

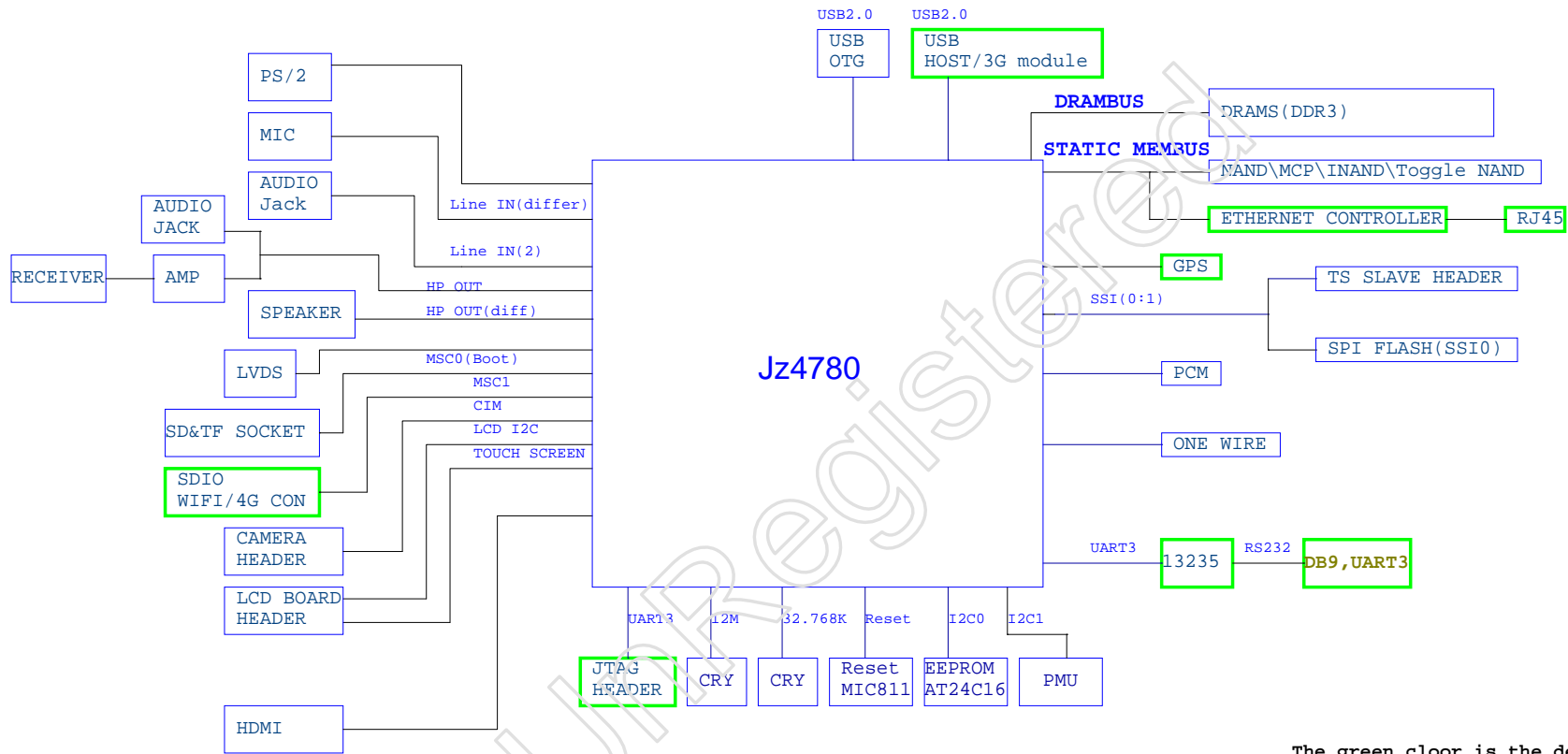


RD4780_GRUS_BOARD

Schematic Revision 1.0

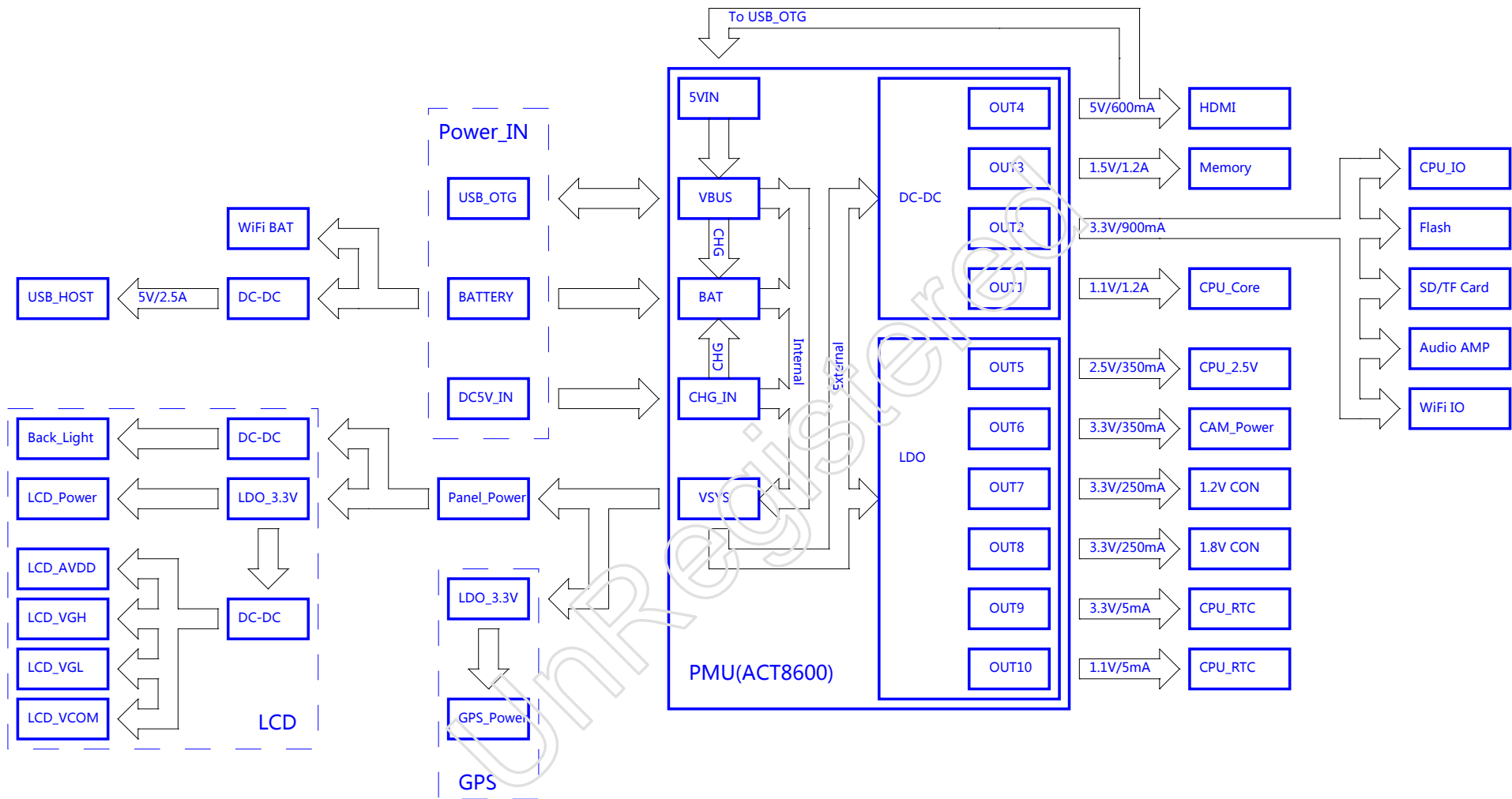
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Nand/Camera	5
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CPU POWER/RESET/SYS CLK/KEY	9
TS/ETH/UART/GPS/JTAG/USB_CON	10
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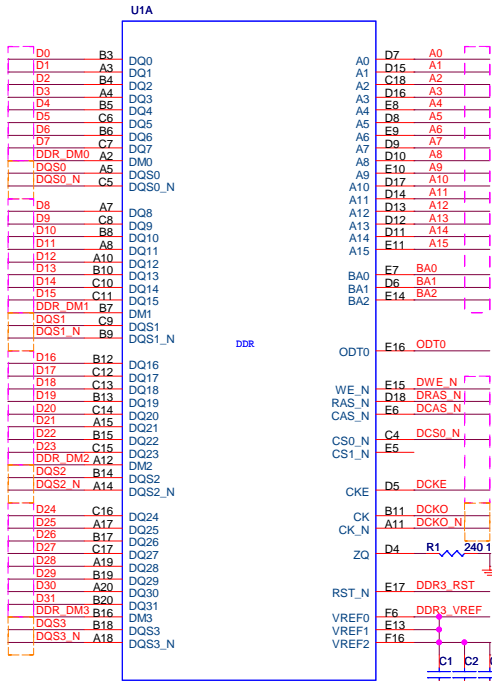
INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD4780_GRUS	
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B	COVER	V1.0
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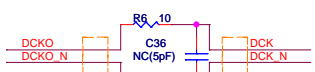
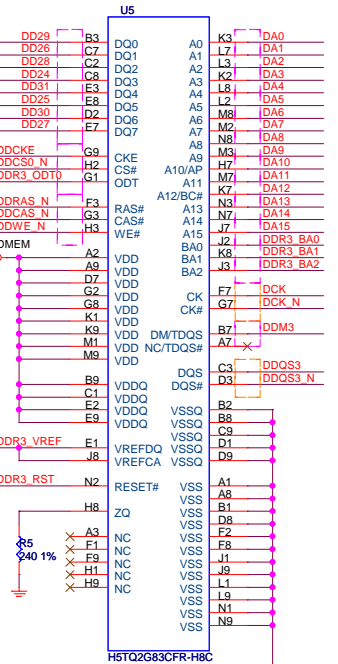
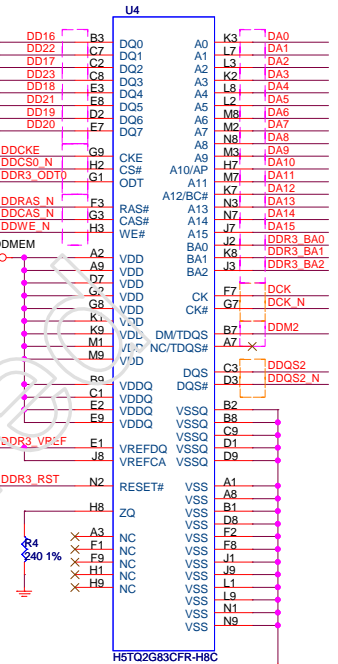
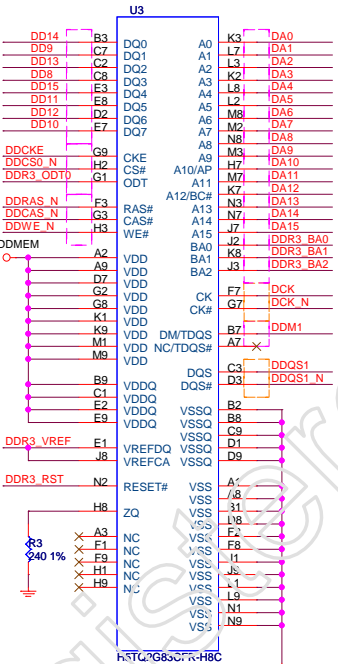
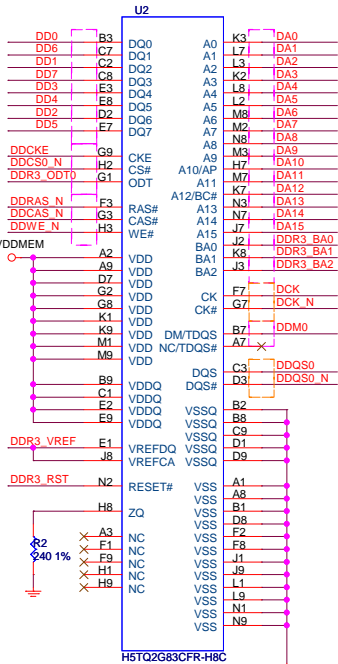
The green color is the debug board

INGENIC SEMICONDUCTOR CO.,LTD			
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A3	SYSTEM ARCHITECTURE	V1.0	
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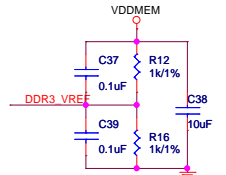




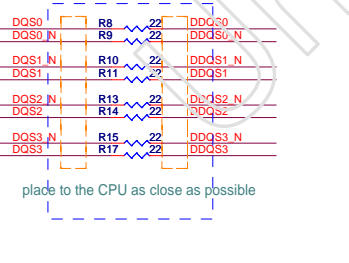
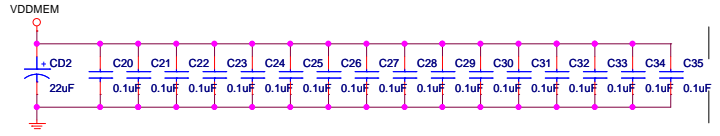
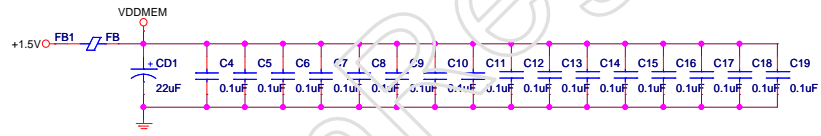
CPU_part_a



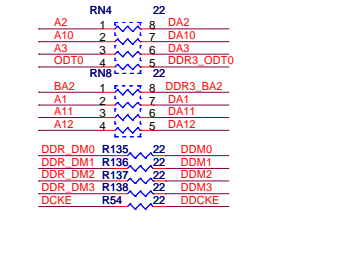
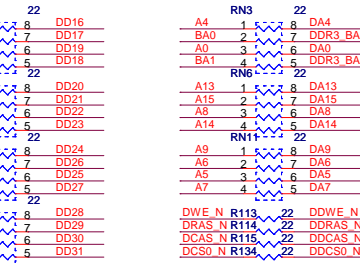
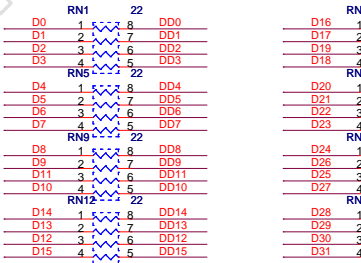
place to the CPU as close as possible



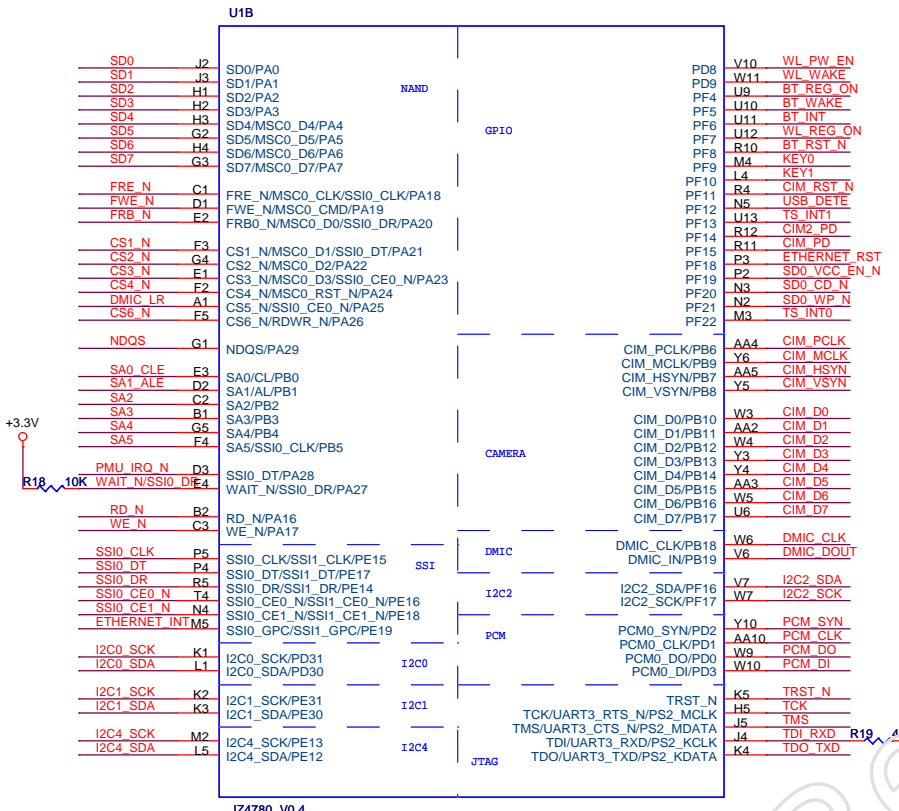
SUGGESTION:
 1. R6 R7 is Differential Clock Termination. place on each side of memory
 2. The traces DDR_VREF is 20 mils wide at least.
 3. R12 and R16 can be adjust to 10K/1k when use DDR



Differential pairs Z0= 100 ohm Equilong BUS Z0= 50 ohm

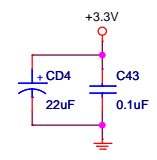
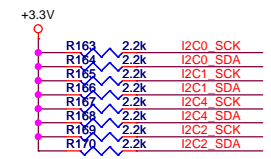
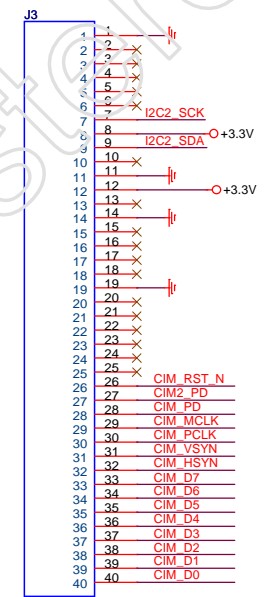
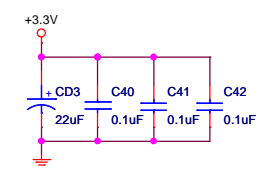
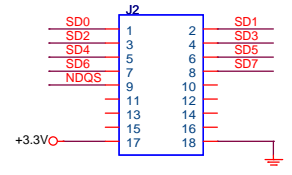
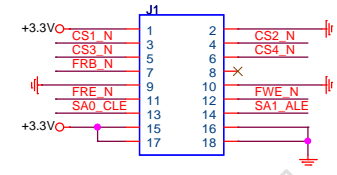


DDR3

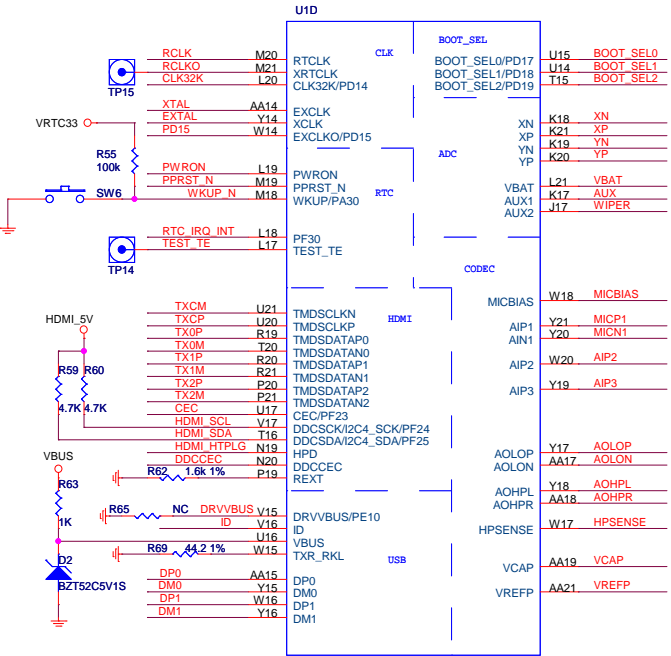


CPU part_b

- | | | |
|--------------|---------------|-----------------|
| BT_RST_N 10 | USB_DETE 11 | SA0_CLE 10 |
| WL_REG_ON 10 | PMU_IRQ_N 7 | SA1_ALE 10 |
| BT_INT 10 | KEY0 9 | SA2 10 |
| WL_PW_EN 10 | KEY1 9 | SA3 10 |
| WL_WAKE 10 | TS_INT0 10 | SA4 10 |
| BT_REG_ON 10 | TS_INT1 10 | SA5 10 |
| BT_WAKE 10 | | |
| PCM_CLK 10 | I2C0_SCK 8 | ETHERNET_INT 10 |
| PCM_SYN 10 | I2C0_SDA 8 | ETHERNET_RST 10 |
| PCM_DI 10 | I2C1_SCK 7 | RD_N 10 |
| PCM_DO 10 | I2C1_SDA 7 | WE_N 10 |
| | I2C2_SCK 10 | CS6_N 10 |
| | I2C2_SDA 10 | SD[0:7] 10 |
| TDO_TXD 10 | I2C4_SCK 9,10 | SD0_CD_N 8 |
| TRST_N 10 | I2C4_SDA 9,10 | SD0_WP_N 8 |
| TCK 10 | I2C4_SDA 9,10 | SD0_VCC_EN_N 8 |
| TMS 10 | | |
| TDL_RXD 10 | SSIO_CE1_N 10 | DMIC_CLK 11 |
| | SSIO_CLK 10 | DMIC_DOUT 11 |
| | SSIO_DT 10 | |
| | SSIO_DR 10 | |
| | SSIO_CE0_N 10 | |



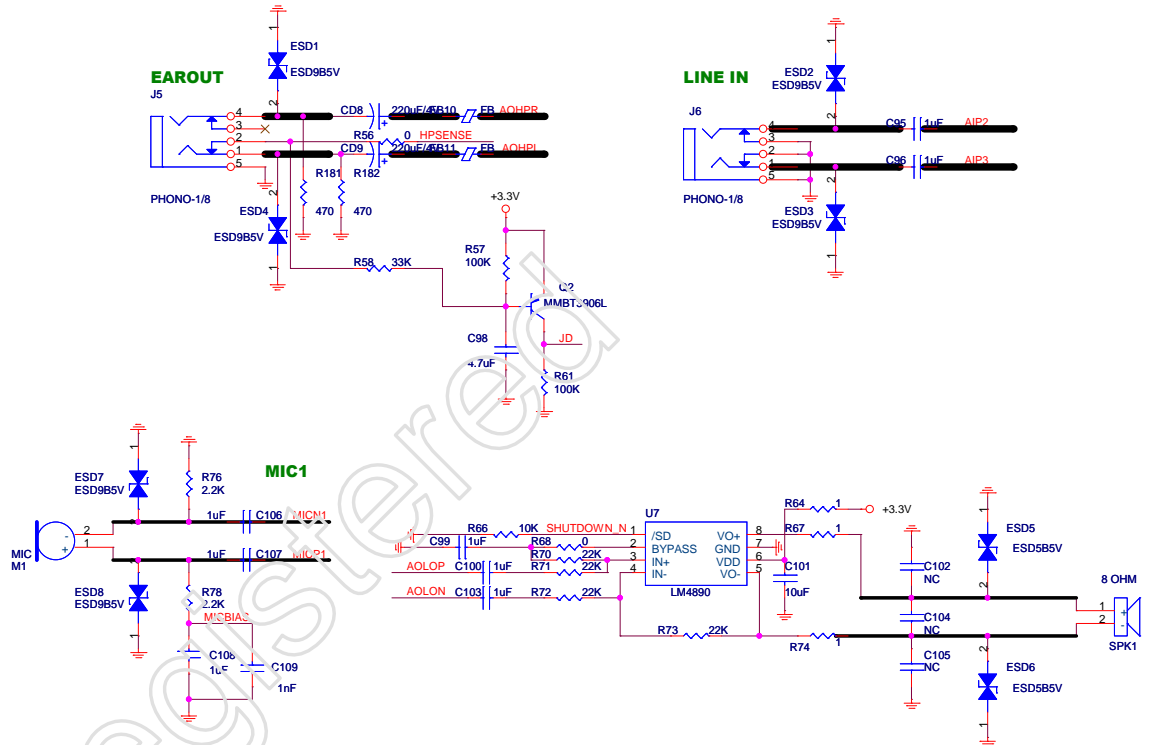
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CPU part_d

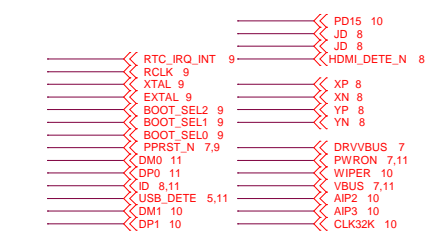
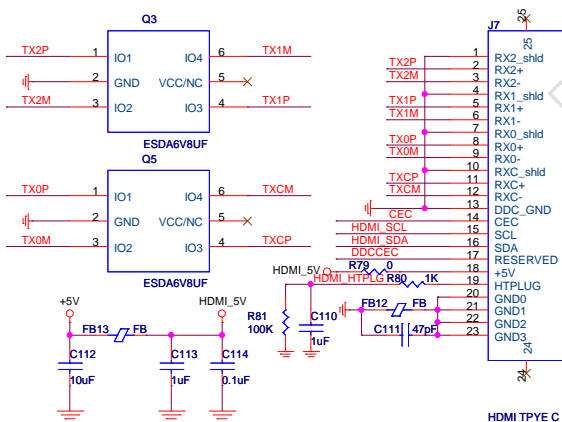
put to CPU pins as close as possible

AUDIO

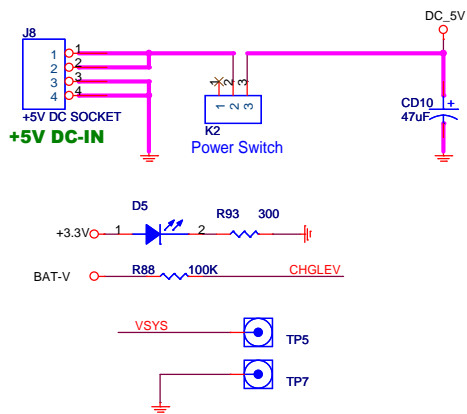


HDMI

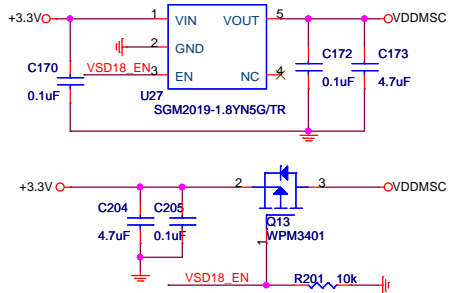
ADC DETECTION



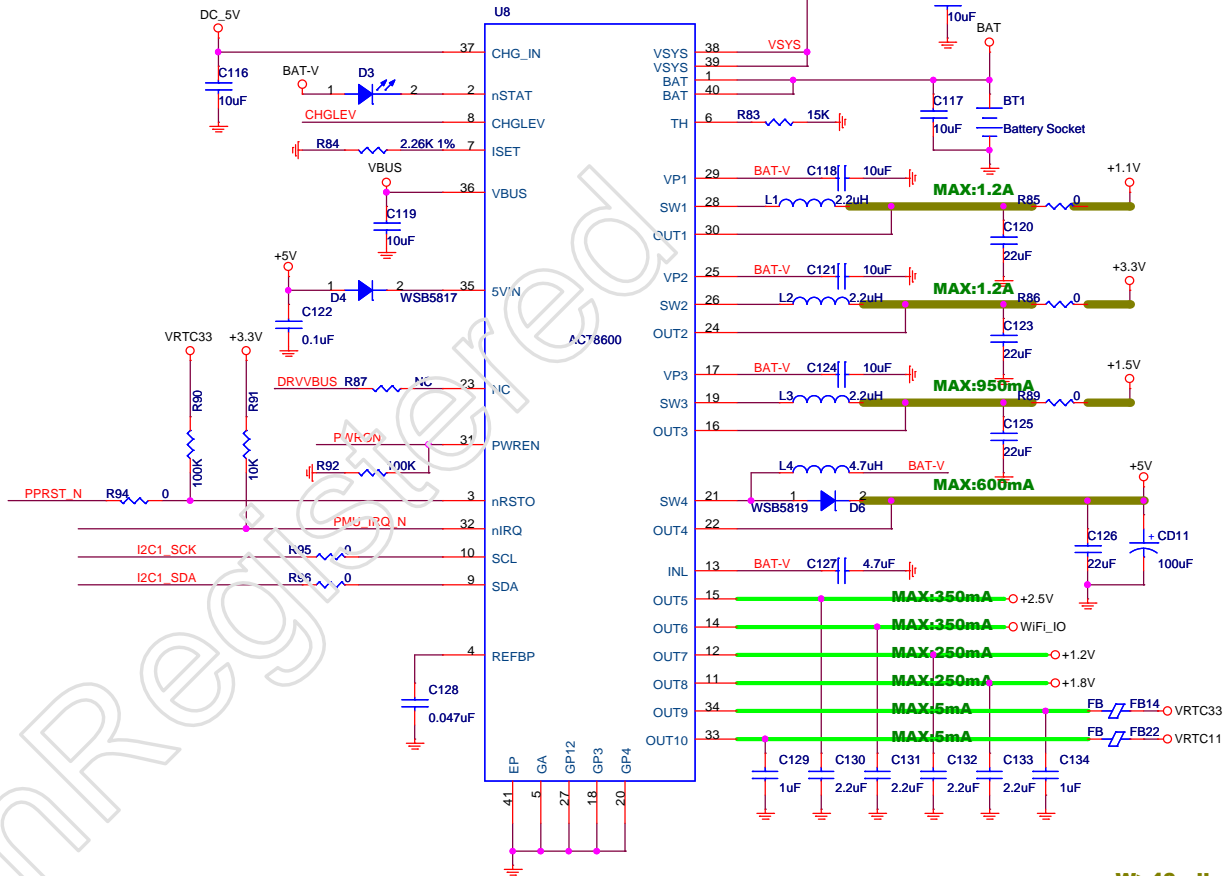
INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD4780_GRUS	
Size	Document Number	Rev
A3	BOOT/AUDIO/HDMI	1.0
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POWER ADAPTER



MSC POWER



PMU

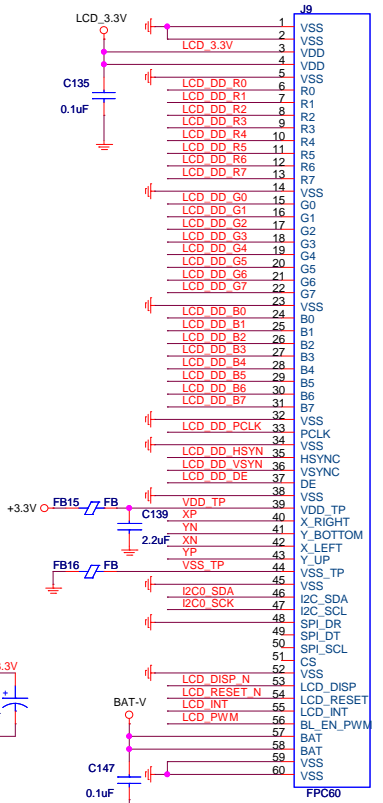
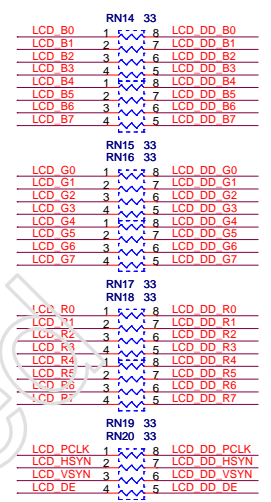
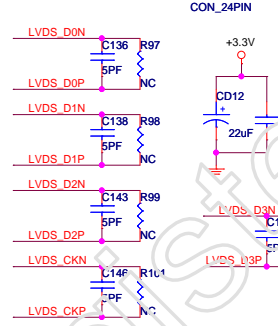
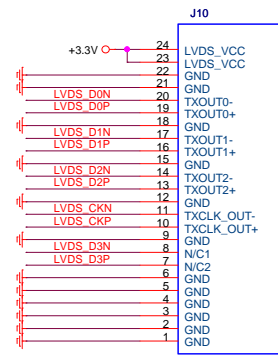
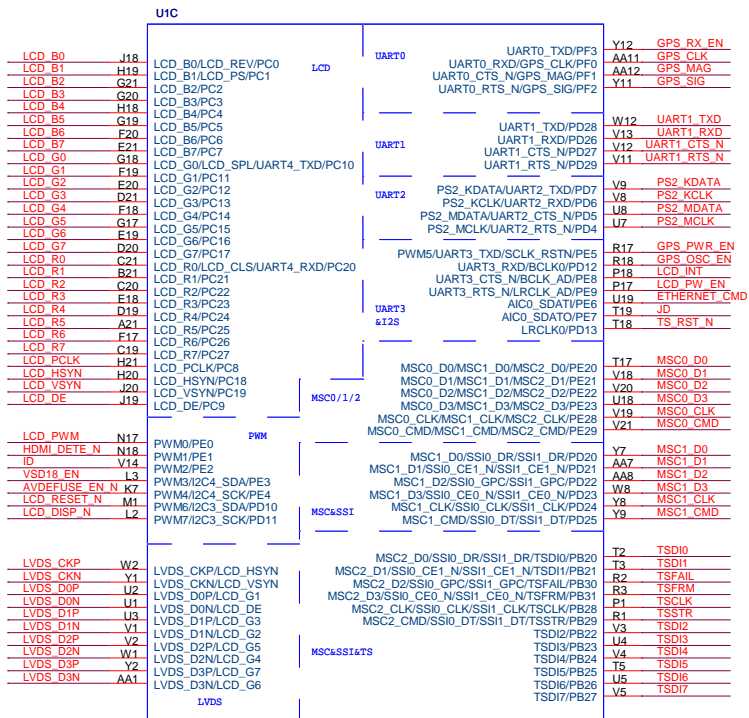
W>40mil

W>20mil



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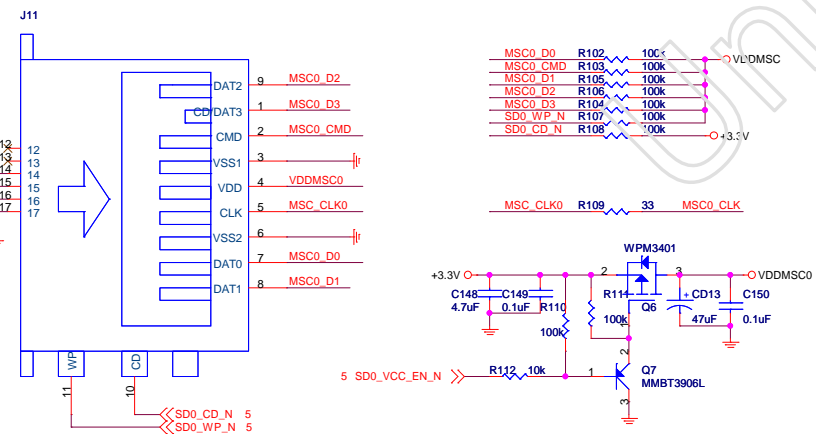
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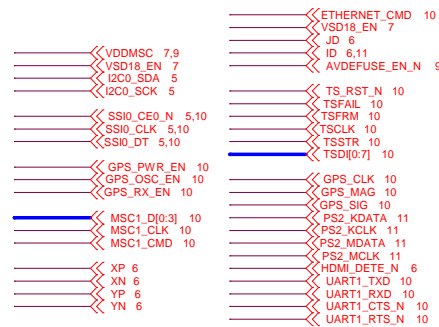
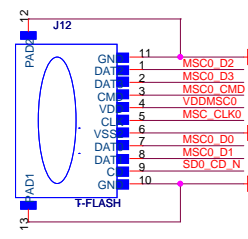
CPU_part_c

LVDS

LCD

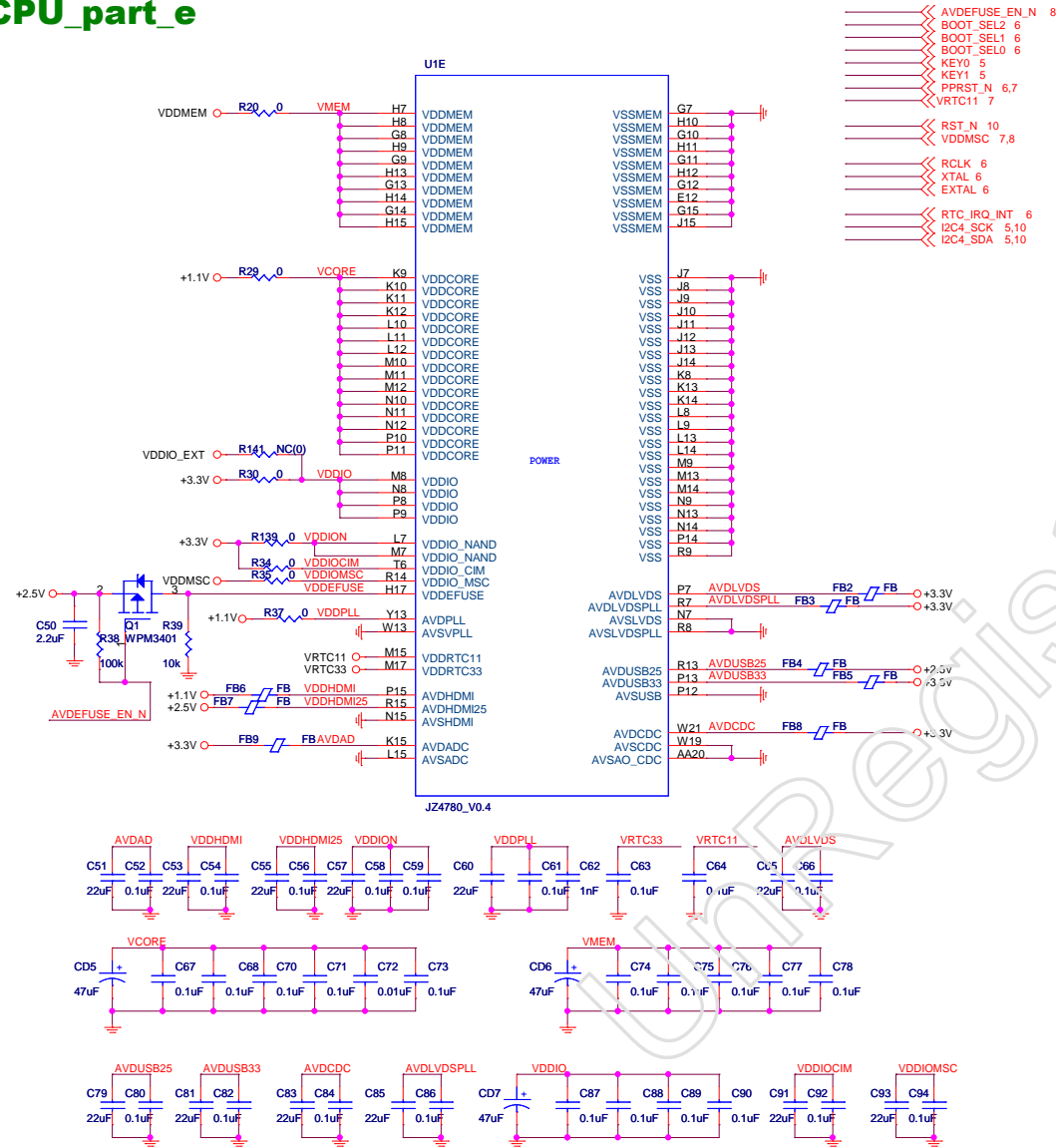


MMC0

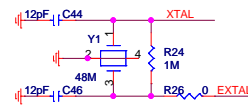


INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD4780_GRUS	
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A3	MMC/LCD/LVDS	1.0
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CPU_part_e

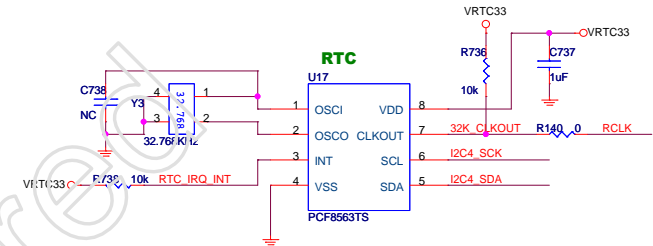


MAIN CLOCK

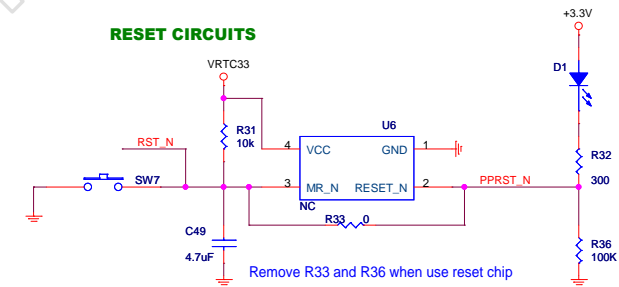


Boot Mode Select

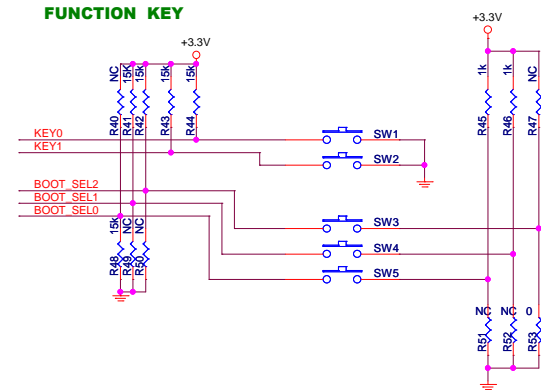
BOOT_SEL[2:1:0]	
111	USB Boot
110	NAND Boot
101	MSC0 Boot
000	SP1 Boot
100	MSC1 Boot
011	eMMC Boot
010	NOR Boot (CS2)



RESET CIRCUITS



FUNCTION KEY

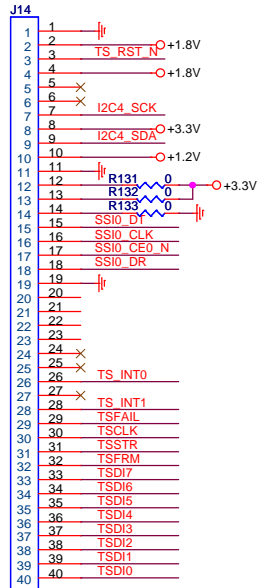


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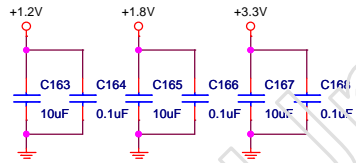
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A3	CPU POWER/RESET/SYS CLK/KEY	1.0
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- WL_REG_ON 5
- BT_INT 5
- WL_PW_EN 5
- WL_WAKE 5
- BT_REG_ON 5
- BT_WAKE 5
- TDO_TXD 5
- TRST_N 5
- TCK 5
- TMS 5
- TDI_RXD 5
- RD_N 5
- WE_N 5
- CS6_N 5
- SD[0:7] 5
- ETHERNET_INT 5
- ETHERNET_RST 5
- ETHERNET_CMD 8
- CS6_N 5
- DM1 6
- DP1 6
- PCM_CLK 5
- PCM_SYN 5
- PCM_DI 5
- PCM_DO 5
- AIP2 6
- AIP3 6
- BT_RST_N 5
- RST_N 9
- GPS_PWR_EN 8
- GPS_OSC_EN 8
- GPS_RX_EN 8
- GPS_CLK 8
- GPS_MAG 8
- GPS_SIG 8
- MSC1_D[0:3] 8
- MSC1_CLK 8
- MSC1_CMD 8
- PMU_IRQ_N 5,7
- CS6_N 5
- UART1_TXD 8
- UART1_RXD 8
- UART1_CTS_N 8
- UART1_RTS_N 8
- SSIO_CE0_N 5
- SSIO_CE1_N 5
- SSIO_CLK 5
- SSIO_DT 5
- SSIO_DR 5
- TS_RST_N 8
- PD15 6
- TS_INT0 5
- TS_INT1 5
- TSFAIL 8
- TSFRM 8
- TSCLK 8
- TSTR 8
- TSDI[0:7] 8
- WIPER 6
- I2C4_SCK 5,9
- I2C4_SDA 5,9
- I2C2_SCK 5
- I2C2_SDA 5
- I2C1_SCK 5,7
- I2C1_SDA 5,7
- SA0_CLE 5
- SA1_ALE 5
- SA2 5
- SA3 5
- SA4 5
- SA5 5
- CLK32K 6

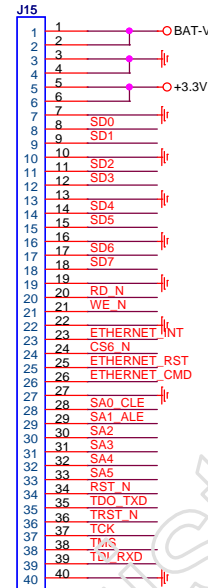
TS Interface Connector



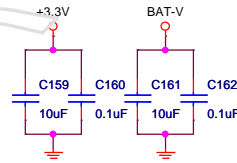
TS INTERFACE



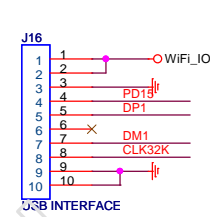
Ethernet & JTAG Interface



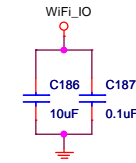
Ethernet & JTAG



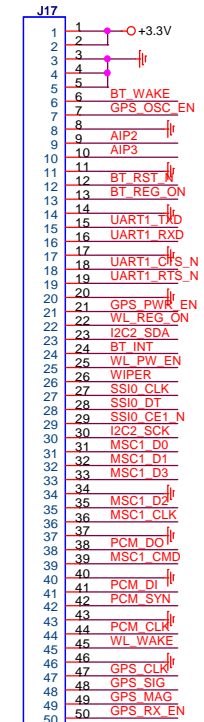
USB Interface



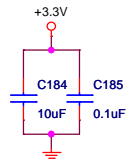
USB INTERFACE



WiFi & GPS Interface

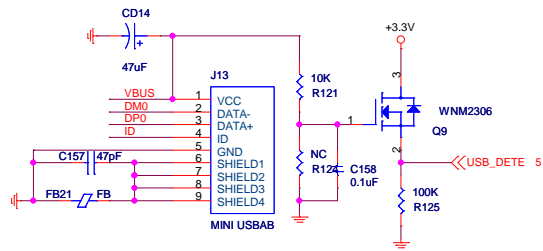


WiFi&GPS

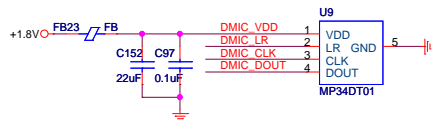


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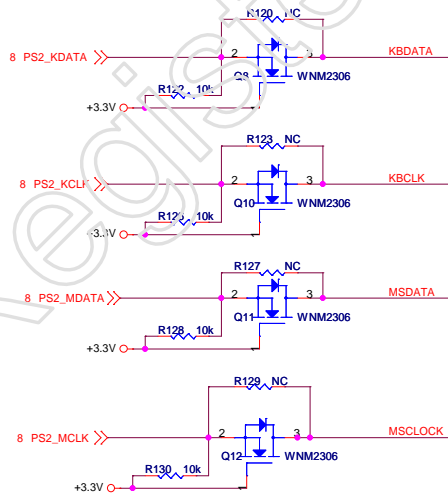
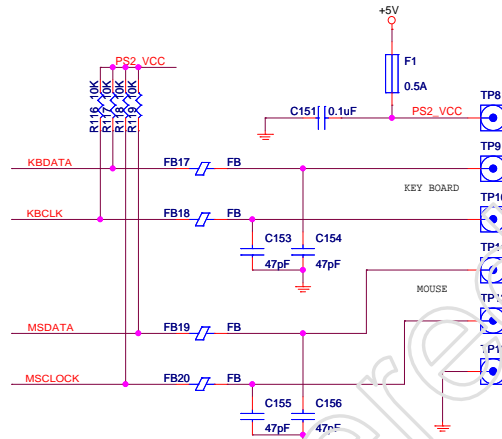
Title		RD4780_GRUS
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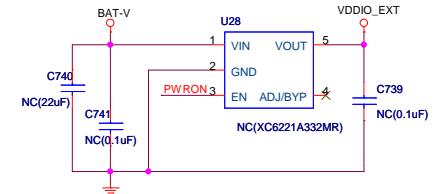
USB2.0_OTG



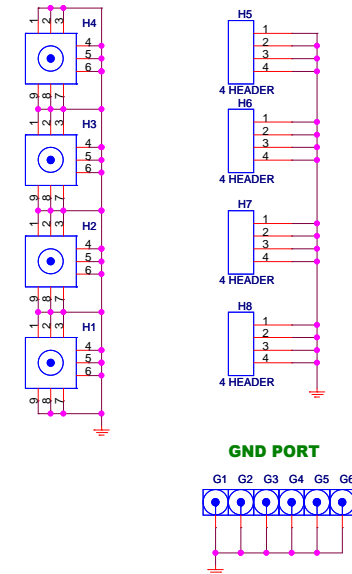
Digital microphone



PS2 PORT



VDDIO_EXT



GND PORT

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Aug 28 2012	Rev1.0	1. First Revision

UnRegistered

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