Ingenic® RD_JZ4775_MENSA Development Board

Hardware Manual

Version: 1.1
Date: 2013.09

北京君正集成电路股份有限公司
Ingenic Semiconductor Co., Ltd.

Ingenic RD_JZ4775_MENSA Development Board

Hardware Manual

Release history

Date	Revision	Change
2013.03	1.0	First release
2013.09	1.1	Change the company address and etc.

Disclaimer

This documentation is provided for use with Ingenic products. No license to Ingenic property rights is granted. Ingenic assumes no liability, provides no warranty either expressed or implied relating to the usage, or intellectual property right infringement except as provided for by Ingenic Terms and Conditions of Sale.

Ingenic products are not designed for and should not be used in any medical or life sustaining or supporting equipment.

All information in this document should be treated as preliminary. Ingenic may make changes to this document without notice. Anyone relying on this documentation should contact Ingenic for the current documentation and errata.

Ingenic Semiconductor Co., Ltd.

Junzheng Bld, Zhongguancun Software Park 2 Dongbeiwang West Road, Haidian District Beijing,China,100193

Tel: 86-10-56345000

Fax: 86-10-56345001

Http: //www.ingenic.cn

Content

1 Overview

JZ4775 is a multimedia application processor, which has a very high performance and low power 32-bit RISC engine. JZ4775 integrates various peripherals for embedded application, such as memory controller, USB1.1 host and USB OTG interface, On-chip audio CODEC, multi-channel SAR-ADC,LCD controller, EPD controller, GMAC controller, CMOS sensor interface, MMC/SD controller, SSI interface, I2C interface, Camera interface, UART, interface, 1-wire, OTP,GPIO, and so on.

The RD_JZ4775_MENSA is a reference design with JZ4775 addressing to consumer electronic equipment that help engineer to quickly develop their own products in hardware and software. This design also provides flexible interface to extend other module.

With this reference design, there have richness development package include Android, Linux, WinCE and Mini OS.

1.1 Functions of RD_JZ4775_MENSA

- CPU: 1.0GHz supports Android, Linux and Mini OS.
- DDR3 SDRAM: H5TQ1G83DFR-H9C x 4, 512MB.
- FLASH: FLASH extended card, TOSHIBA THGBM4G5D1HBAIR 4GB .
- LCD: 800x480 5.0inch TFT with touch panel and support EPD panel.
- Multimedia: Support every multimedia software De/Encoder.
- LVDS interface：LVDS panel
- 7 keys can provide soft power on/off and extended application etc.
- USB1.1 Host / USB OTG interface.
- GMAC : Support 10/100/1000M Ethernet(Default connect to the 10M/100M PHY).
- UART: 2-wire RS232, GPS+GSM module extension.
- Camera interface: Compatible 8-bit ITU656 camera.
- MMC/SD TF extended interface can support SDIO interface.
- Backlight control with PWM.
- Advanced power manager: Lithium battery charge; support RTC alarm and power up; very low power consumption; battery charging status indicator and battery voltage monitor.

1.2 RD_JZ4775_MENSA System Architecture

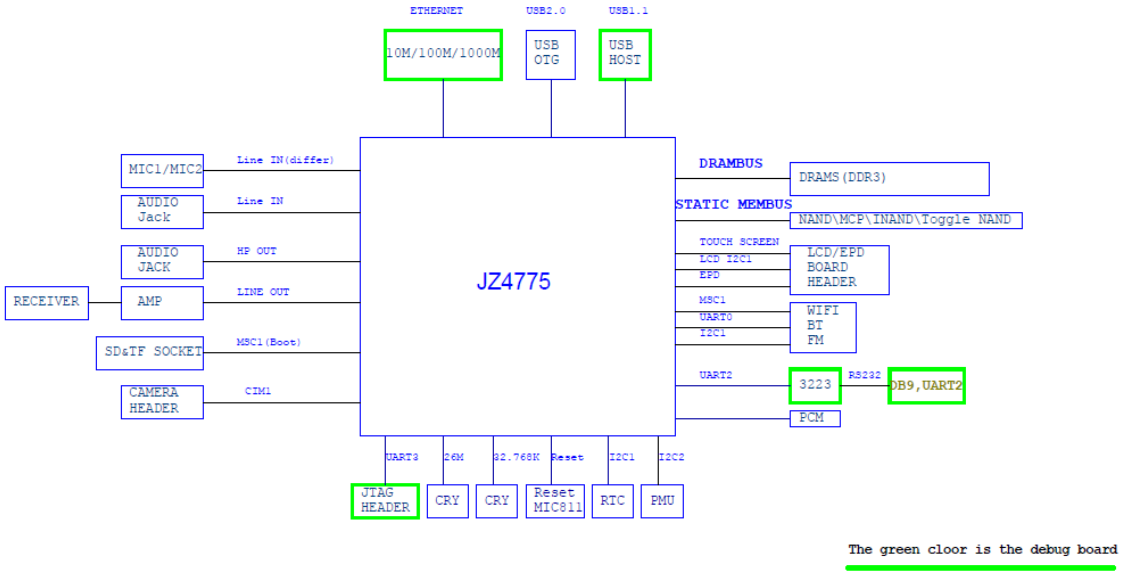

Figure 1-1 RD_JZ4775_MENSA System Architecture

2 Hardware Description

In this section, we describe every hardware module of the board. Please refer to the user's guide of JZ4775 first. For the other components, please refer to relative datasheet. For the details of the board, please refer to RD_JZ4775_MENSA schematic design.

2.1 RD_JZ4775_MENSA board picture

Figure 2-1shows the picture of the main components and connectors.(118mm X 100mm)

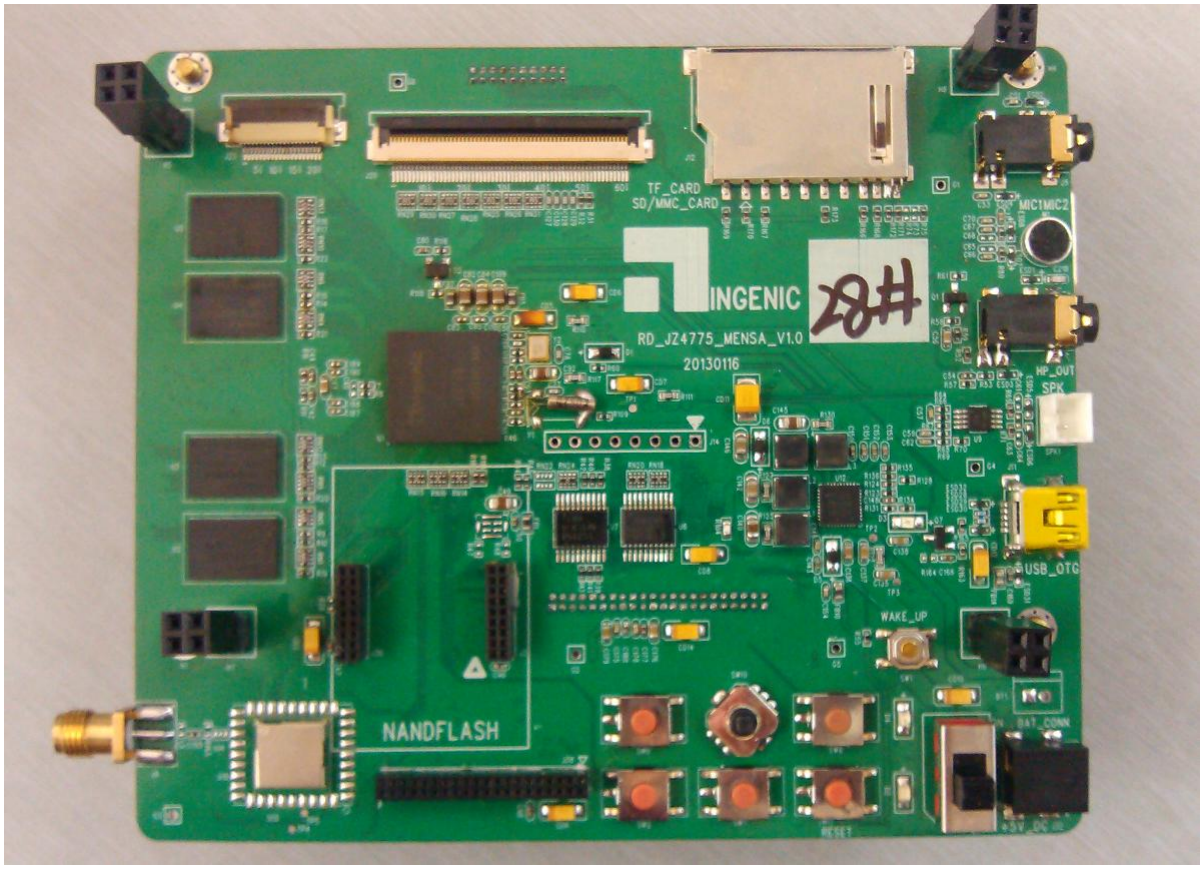

Figure 2-1 RD_JZ4775_MENSA board

2.2 Power

The RD_JZ4775_MENSA board is powered by 5V adapter or USB. K1 is power on/off switch. SW1 is hibernate/wakeup key. It also can be powered by Lithium Battery.

When power is on and system is running, push SW1 for several seconds. It will assert an interrupt to CPU, and CPU will set PW_ON low to power off the board. When long push SW1 again PW_ON is high and power is on (software on/off).

The main power chip PMU (ACT8600) which is power manage unit can support +3.3V, +1.5V and +1.2V. LED-D4 indicates +3.3V power. PMU out9 is RTC power that support +1.8V.

J32 is external power supply jack. It should be connected with 5V-2A DC adapter that power system and charge up battery. Adapter supply current limit is 2A. LED D3 indicates the charge

status when charging. CPU can realize charge state through I2C access PMU's register.

This board also can be powered and charged the battery by USB. Supply current limit is 450mA .The PRI is adapter, USB port and Li battery.

2.3 System Reset

When power on, PMU can provide system reset signal to CPU, extended card and debug card. SW11 is the manual reset button.

2.4 System boot mode

RD_JZ4775_MENSA has six boot modes:

- USB
- Nand Flash
- SPI Flash
- SD/MMC (MSC0, MSC1)
- eMMC

Table 2-1 describes the setting of boot start:

Table 2-1 BOOT SETUP

Hold push key	***Boot From***
SW8	USB Boot
SW8+SW9	Nand Boot
None	MSC0 Boot(default)
SW7+SW9	SPI Boot
SW9	MSC1 Boot
SW7+SW8	eMMC Boot(for special eMMC nand boot)

2.5 SYSTEM MEMORY(DDR3 SDRAM)

RD_JZ4775_MENSA has 4 chips, 32bit bus width, 512MByte DDR3 SDRAM.

2.6 NAND extended card

J30, J31 are iNAND Flash extended slot, default configuration TOSHIBA iNAND THGBM4G5D1HBAIR , 4GB.

2.7 LCD interface and Expansion card

2.7.1 LCD interface definition

J20 is the LCD interface, which can directly connect to LCD Expansion card. RD_JZ4775_MENSA can support serial/parallel interface(ITU656/601), 18/24bit RGB TFT panel; delta RGB TFT panel; smart LCD and STN panel. It also contains I2C and SPI interface for suitable use.

Table 2-2 LCD Interface（J20）Signals Definition

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	+3.3V	4	+3.3V
5	GND	6	LCD_R0/ LCD_CLS
7	LCD_R1	8	LCD_R2
9	LCD_R3	10	LCD_R4
11	LCD_R5	12	LCD_R6
13	LCD_R7	14	GND
15	LCD_G0/LCD_SPL	16	LCD_G1
17	LCD_G2	18	LCD_G3
19	LCD_G4	20	LCD_G5
21	LCD_G6	22	LCD_G7
23	GND	24	LCD_B0/LCD_REV
25	LCD_B1/LCD_PS	26	LCD_B2
27	LCD_B3	28	LCD_B4
29	LCD_B5	30	LCD_B6
31	LCD_B7	32	GND
33	LCD _PCLK	34	GND
35	LCD_HSYNC	36	LCD_VSYNC
37	LCD_DE	38	GND
39	VDD_TP	40	XP
41	YN	42	XN
43	YP	44	VSS_TP
45	GND	46	I2C_SDA
47	I2C_SCK	48	GND
49	SSI1_DT	50	SSI1_CLK
51	SSI1_CE0_N	52	GND
53	LCD_DISP_N	54	LCD_RESET_N
55	LCD_INT	56	PWM4/BL_EN_N
57	BAT-V	58	BAT-V
59	GND	60	GND

There are some special signals: 1-LCD_SPL; 2-LCD_CLS; 3-LCD_PS; 4-LCD_REV. For details please refer to JZ4775 datasheet.

2.7.2 LCD Expansion card

RD4770_PISCES_LCD_BOARD_V1.0 is the LCD expansion card. J1 is the connector with 60 pin FPC to motherboard. J2 is LCD slot which connected BM8766U LCD panel default.

Backlight circuit is RT9293 (U1).Please attend drive current when use other LCD panel(refer to RT9293 datasheet). Adjust R2 can get suitable drive current. Backlight of LCD panel can be adjusted by software of PWM.

2.8 EPD interface

JZ4775 has a EPD controller, support most EPD panel. J20 and J23 are EPD connectors, which can be connect EPD board (RD4760_LEPUS_EPD_V1.0, RD_JZ4775_MENSA_EPD_V1.0 or RD_JZ4775_MENSA_EPD_V1.1 etc.) through 60 pin FPC. J20 is also LCD connector, but can not connect both boards.

Table 2-3 EPD interface (J20) Signals Definition

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	+3.3V	4	+3.3V
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	GND
15	SDCE_[0]	16	SDCE_[1]
17	SDDO[4]	18	SDDO[5]
19	SDDO[6]	20	SDDO[7]
21	NC	22	NC
23	GND	24	GDRL
25	GDSP	26	GDOE
27	SDSHR	28	SDDO[0]
29	SDDO[1]	30	SDDO[2]
31	SDDO[3]	32	GND
33	SDCLK	34	GND
35	SDLE	36	GDCLK
37	SDOE	38	GND
39	NC	40	NC
41	NC	42	NC
43	NC	44	GND
45	GND	46	I2C_SDA
47	I2C_SCK	48	GND
49	NC	50	NC
51	NC	52	GND
53	NC	54	NC
55	NC	56	NC
57	BAT-V	58	BAT-V
59	GND	60	GND

Table 2-4 EPD interface (J23) Signals Definition

Pin Number	Signal	Pin Number	Signal
1	NC	2	GND
3	PWR0	4	PWR1
5	PWR2	6	PWR3
7	PWR4	8	PWR6
9	PWR5	10	PWR7
11	SDCE_L2	12	SDCE_L3
13	SDCE_L4	14	SDCE_L5
15	PWRCOM	16	NC
17	NC	18	NC
19	GND	20	AUX1

2.9 USB Interface

RD_JZ4775_MENSA support USB OTG. There are one MiniAB USB port on main board (J11). It contains insert detect circuit. The USB1.1 host port is on debug board, which can support 500mA current.

2.10 Audio System

2.9.1 Headphone

JZ4775 provides an internal AC97/I2S audio CODEC and 24bits DAC/ADC. User can connect other external CODEC. The audio system use internal CODEC to implement the input and output of audio. J4 is a 3.5mm standard headphone jack. The chip can support up to 16 ohm load.

2.9.2 MIC

M1 is capacitive microphone.

2.9.3 Speaker

SPK1 is audio power connector which can support stereo speaker. 1W output for 8 ohm load.

2.11 WIFI

RD_JZ4775_MENSA integrate WIFI module (IW8101/IW8103/IW8103B can be selected).

2.12 Keypad Interface

There are five keys reserved for extending accessorial application by software control (SW1, SW2, SW7, SW8, SW9).

2.13 MMC/SD TF card

J12 is the MMC/SD card socket for extension memory, supports MMC or SD card. J13 is the TF

card socket. The power on both socket can be turn off by software.

2.14Debug Board Interface

In order to make the system debugging facility, there is a debug board connecting to the main board through head J26 and J27. It provides USB port, JTAG port, UART port (DB9,2-wire RS-232) and 10/100/1000M BASE Ethernet port (RJ45).

2.15System Status LED

There are three LEDs for system status indicator:

- LED D4 indicates the +3.3V power status.
- LED D2 indicates system reset status.
- LED D3 indicates the charge status that light when charging.

2.16CIM interface

J38 is RD_JZ4775_MENSA camera interface can support CMOS and CCD Decoder(CCIR656 data format, RGB/YCbCr color).

Table 2-4 CIM interface (J38) Signals Definition

Pin Number	Signal	Pin Number	Signal
40	CIM_D0	39	CIM_D1
38	CIM_D2	37	CIM_D3
36	CIM_D4	35	CIM_D5
34	CIM_D6	33	CIM_D7
31	CIM_VSYNC	32	CIM_HSYNC
29	CIM_MCLK	30	CIM_PCLK
27	CIM1_PD	28	CIM2_PD
25	NC	26	CIM1_RST_N
23	NC	24	NC
21	NC	22	NC
19	GND	20	NC
17	NC	18	NC
15	NC	16	NC
13	NC	14	GND
11	GND	12	3.3V
9	I2C1_SDA	10	NC
7	I2C1_SCK	8	3.3V
5	NC	6	NC
3	NC	4	NC
1	GND	2	NC

2.17 EFUSE

JZ4775 provide EFUSE function, users can program as needed EFUSE. AVDEFUSE pin should be kept 0V except during programming. Maximum accumulative time for AVDEFUSE pin

exposed under 2.5V should be less than 1 sec. For detail, please refer to JZ4775 datasheet.

3 Quick start RD_JZ4775_MENSA board

When you get the RD_JZ4775_MENSA board, it has been initialized with Linux system. Before power on the board, please do the following step:

- Connecting the debug board;
- Connecting serial port – UART to a host PC as console，the configuration is 57600-8N1;
- Connecting a battery to BT1, external DC power adapter (5V-2A) or USB port;

Keys introduction：

- SW1: system power on/off and wakeup manual. Long pushing will turn on the board, once again will turn it off. When in sleep mode, long pushing will wake up the system.
- SW11： system reset manual.

Start Linux system:

After power on the board, there will be output on the console via serial port and LCD panel. After a moment, the demo application will be launched, you will go into a rich and colorful multimedia world.

4 Appendix: GPIO Definition

in Number	Default Port Name	Name for Real Size	Direction	Active	Function
K1	CIM1_D2/SD10/PG12	DMIC_LR	Output	Low	DMIC right/left selection
W8	MSC2_D1/PB21	PMU_IRQ_N	Input	LOW	PMU interrupt
J1	CIM1_D0/SD8/PG10	WLAN_PW_EN	Output	High	WIFI Power Enable
N2	CIM1_PCLK/PG6	WL_WAKE	Output	High	WIFI Wake Up
H1	CIM1_D1/SD9/PG11	BT_REG_ON	Output	High	BT REG ON
P1	CIM1_HSYN/PG7	BT_WAKE	Output	High	BT Wake Up
M2	CIM1_MCLK/PG9	BT_INT	Input	High	BT interrupt
J2	CIM1_D3/SD11/PG13	WL_REG_ON	Output	High	WL REG ON
N1	CIM1_VSYN/PG8	BT_RST_N	Output	Low	BT Reset
M3	WAIT_N/SSI0_DR/PA27	CIM_RST_N	Output	Low	CIM Reset
K5	RD_N/PA16	USB_DETE	Input	High	USB detect
R2	CIM0_CLK/PB6	CIM2_PD	Output	High	Camera2 power down
R2	CIM0_CLK/PB6	CIM1_PD	Output	High	Camera1 power down
T1	CIM0_HSYN/PB7	PHY_RESET_N	Output	High	ETHERNET reset
M6	SA3/PB3	SD0_VCC_EN	Output	High	SD Power enable
K3	SA2/PB2	SD0_CD_N	Input	Low	SD CD detect
T8	DRVVBUS/PE10	SD0_WP_N	Input	Low	SD Write protect
Y9	MSC2_D3/PB31	RTC_IRQ_INT	Input	Low	RTC Interrupt
M17	PWM1/PE1	LCD_PWM	Output	High	LCD PWM
Y8	MSC2_D0/PB20	EPD_SIG_CTRL_N	Output	Low	EPD signal control
M5	SA5/SSI0_CLK/PB5	ID	Input	Low	USB OTG ID Interrupt
M19	PWM2/PE2	AVDEFUSE_EN_N	Output	Low	AVDEFUSE ENABLE
AA10	MSC2_CLK/PB28	LCD_RESET_N	Output	Low	TP WAKE
AA9	MSC2_D2/PB30	LCD_DISP_N	Output	Low	LCD DISPLAY
W9	MSC2_CMD/PB29	LCD_INT	Input	Low	TP INTRRUPT
K6	WE_N/PA17	JD	Input	High	AUDIO INPUT DETECT