

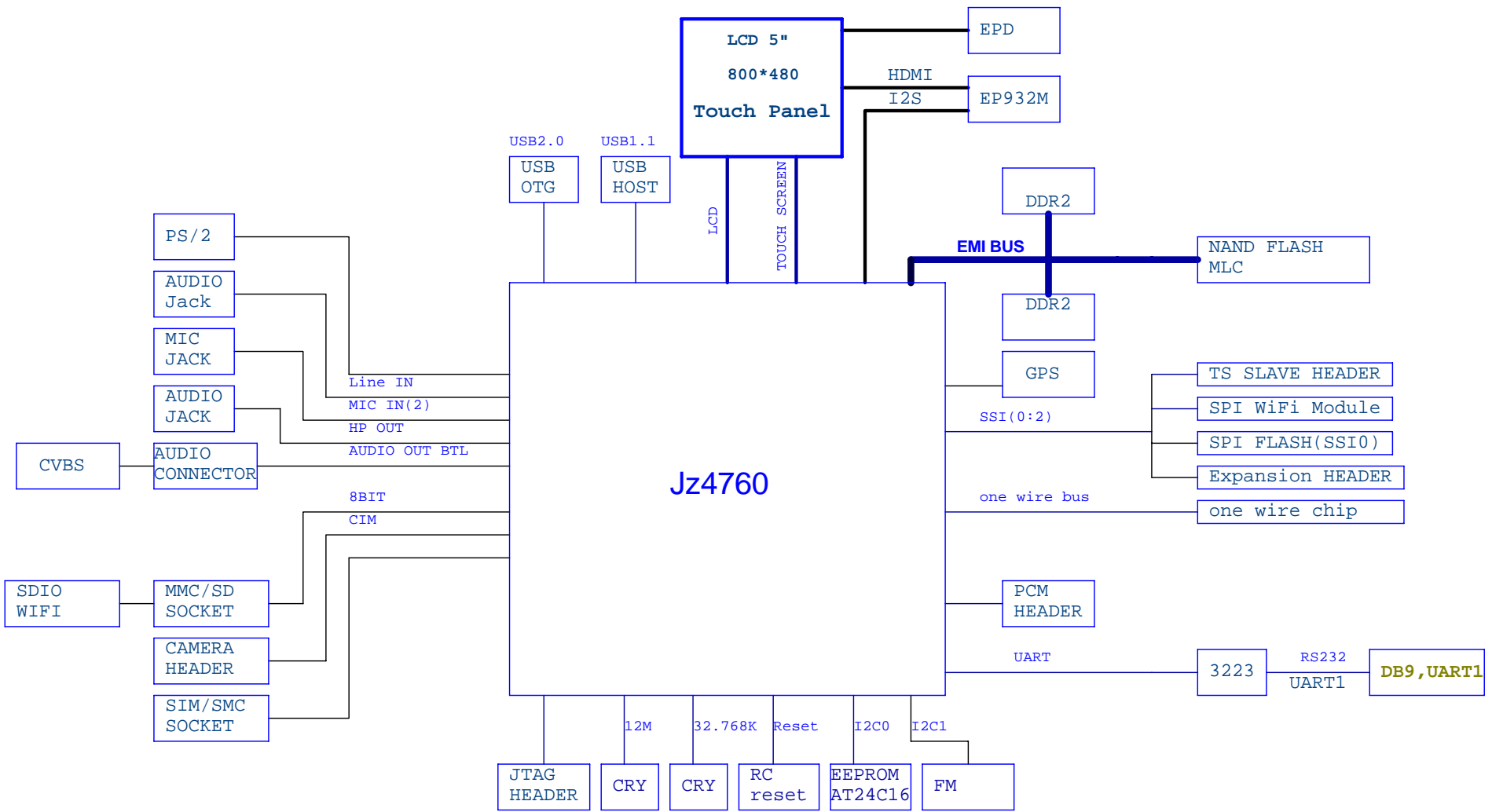


RD4760_LEPUS BOARD

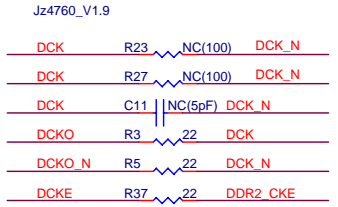
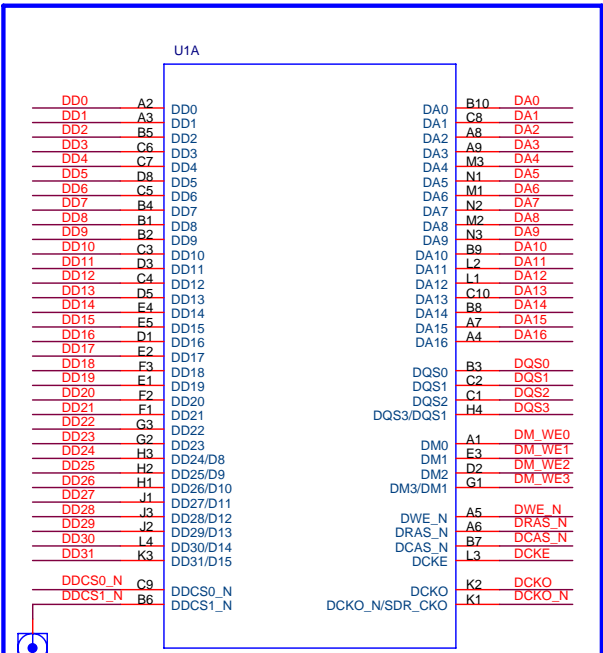
Schematic Revision 1.3.1

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B	COVER	1.3.1
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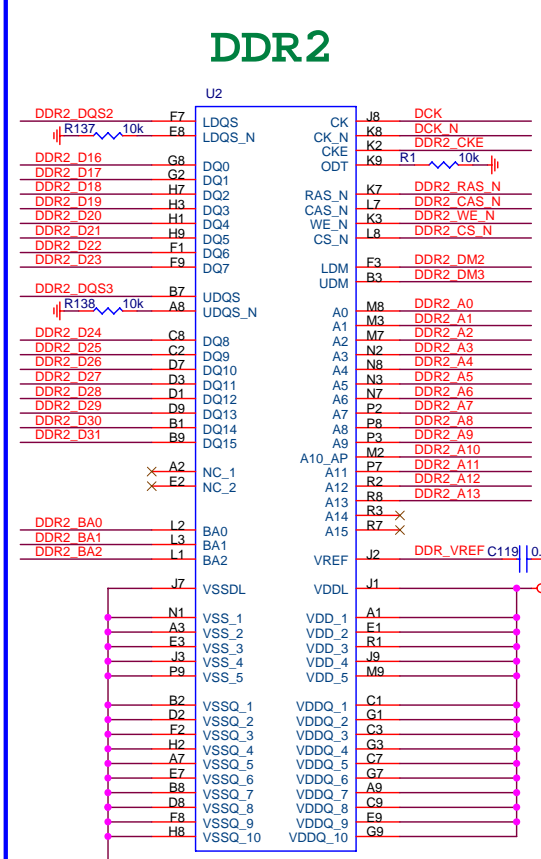
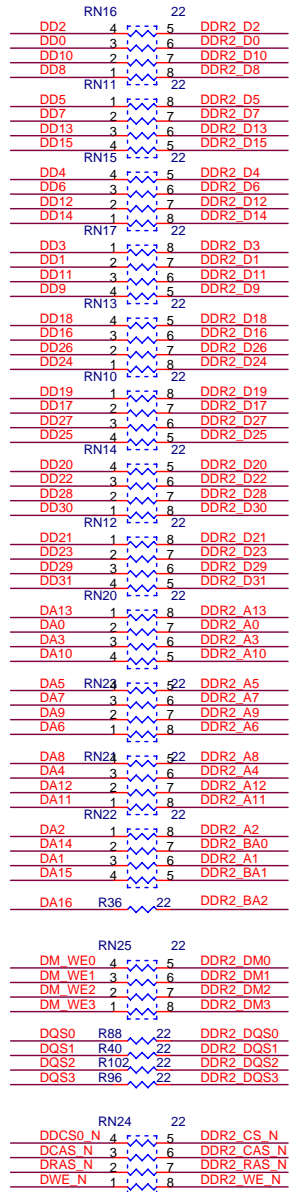


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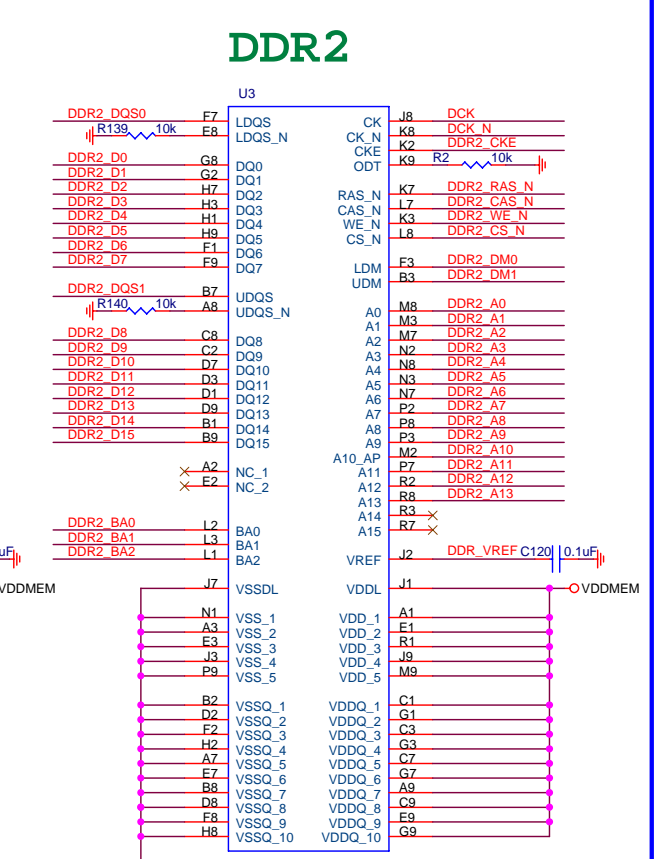
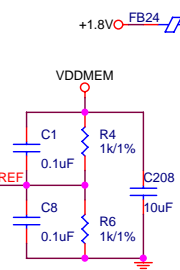
SUGGESTION:

- R23 R27 is Differential Clock Termination. place on each side of memory
- The trance DDR_VREF is 20 mils wide at least.

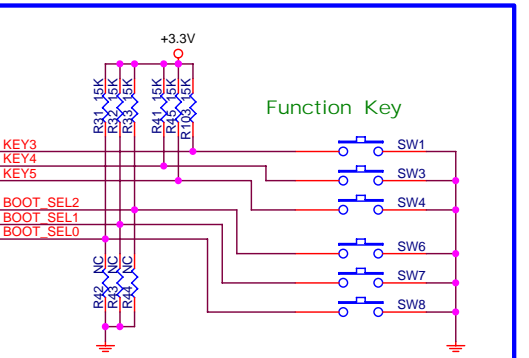
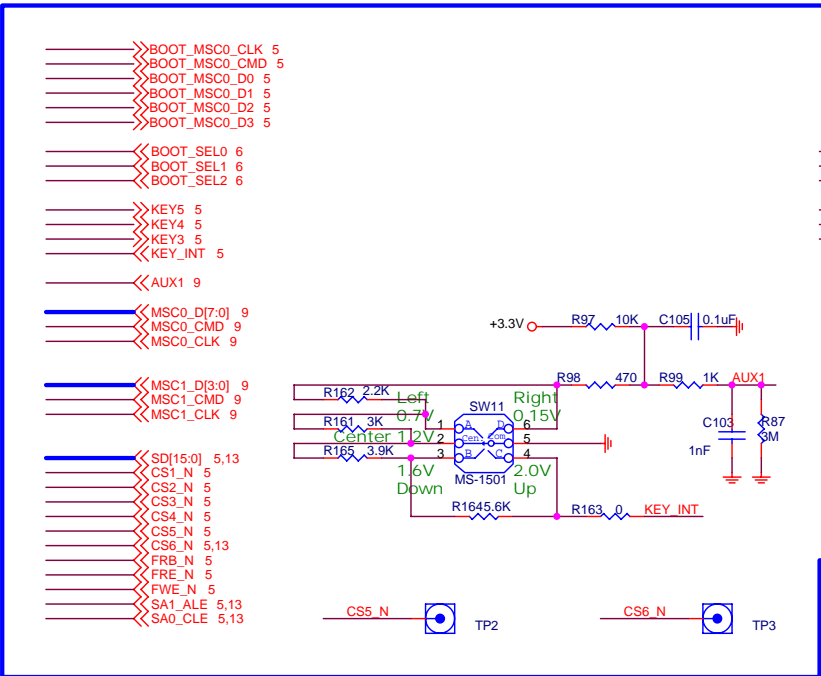
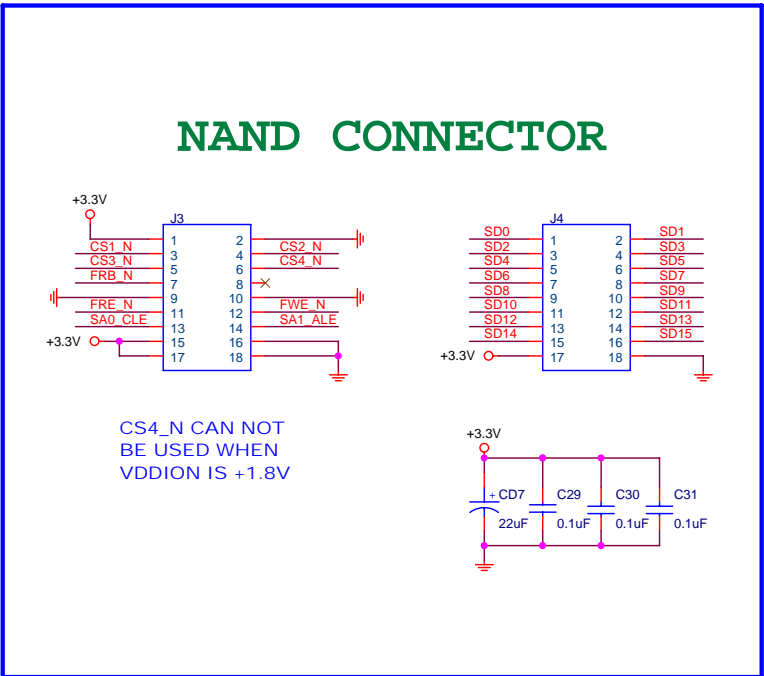
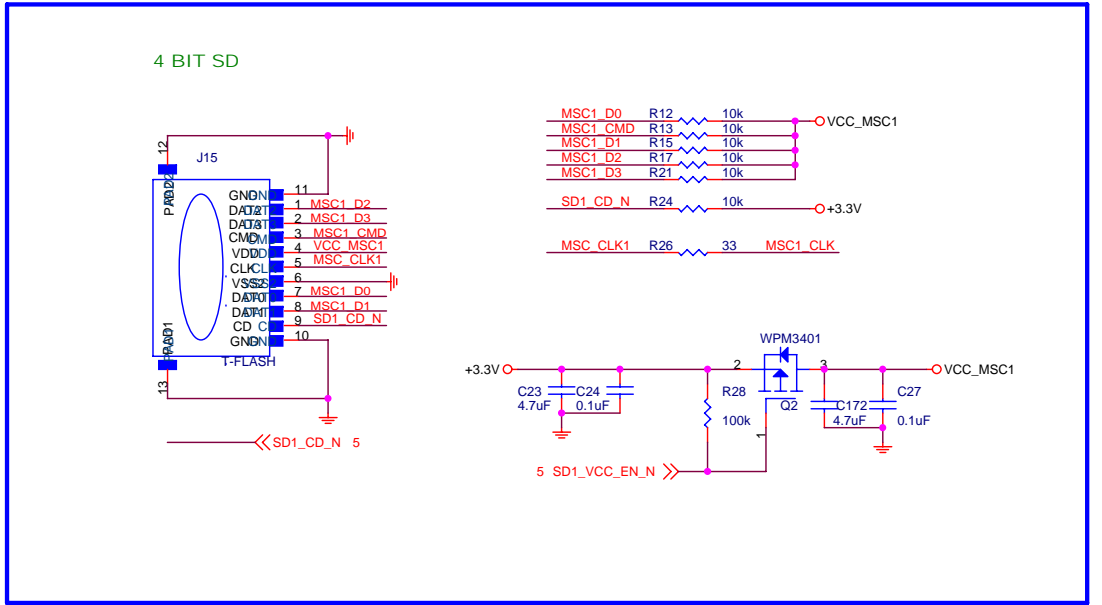
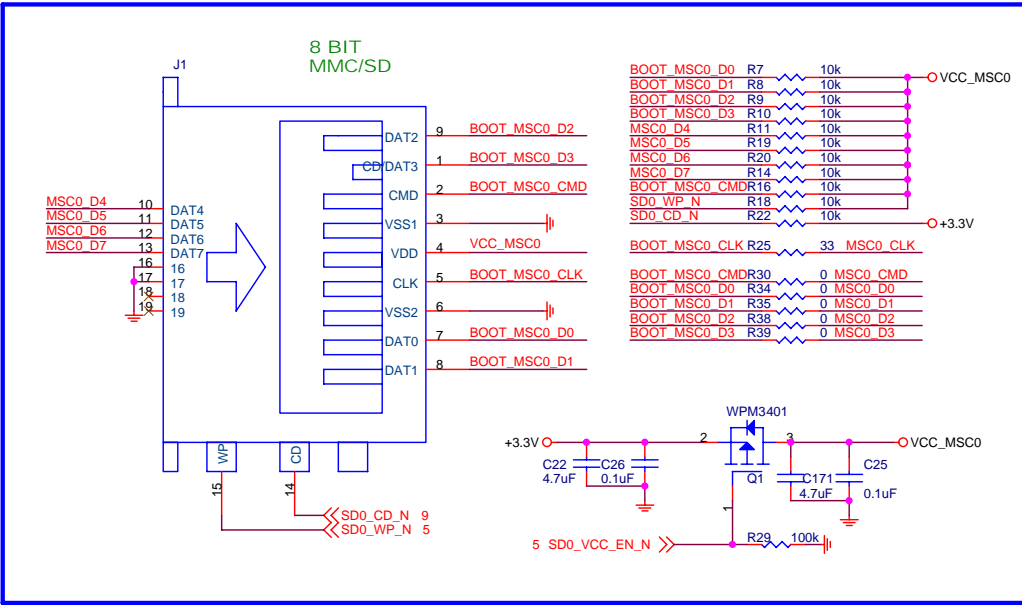


4 R4 and R6 can be adjust to 10K/1Ω when use mDDR

6 DDR_VREF >> DDR_VREF

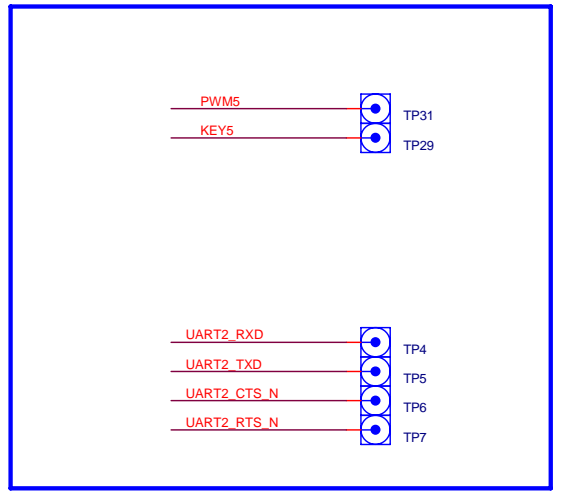
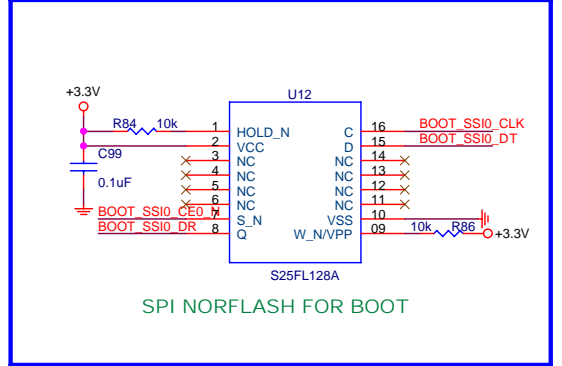
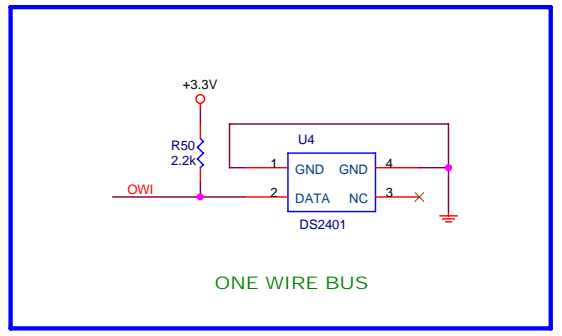
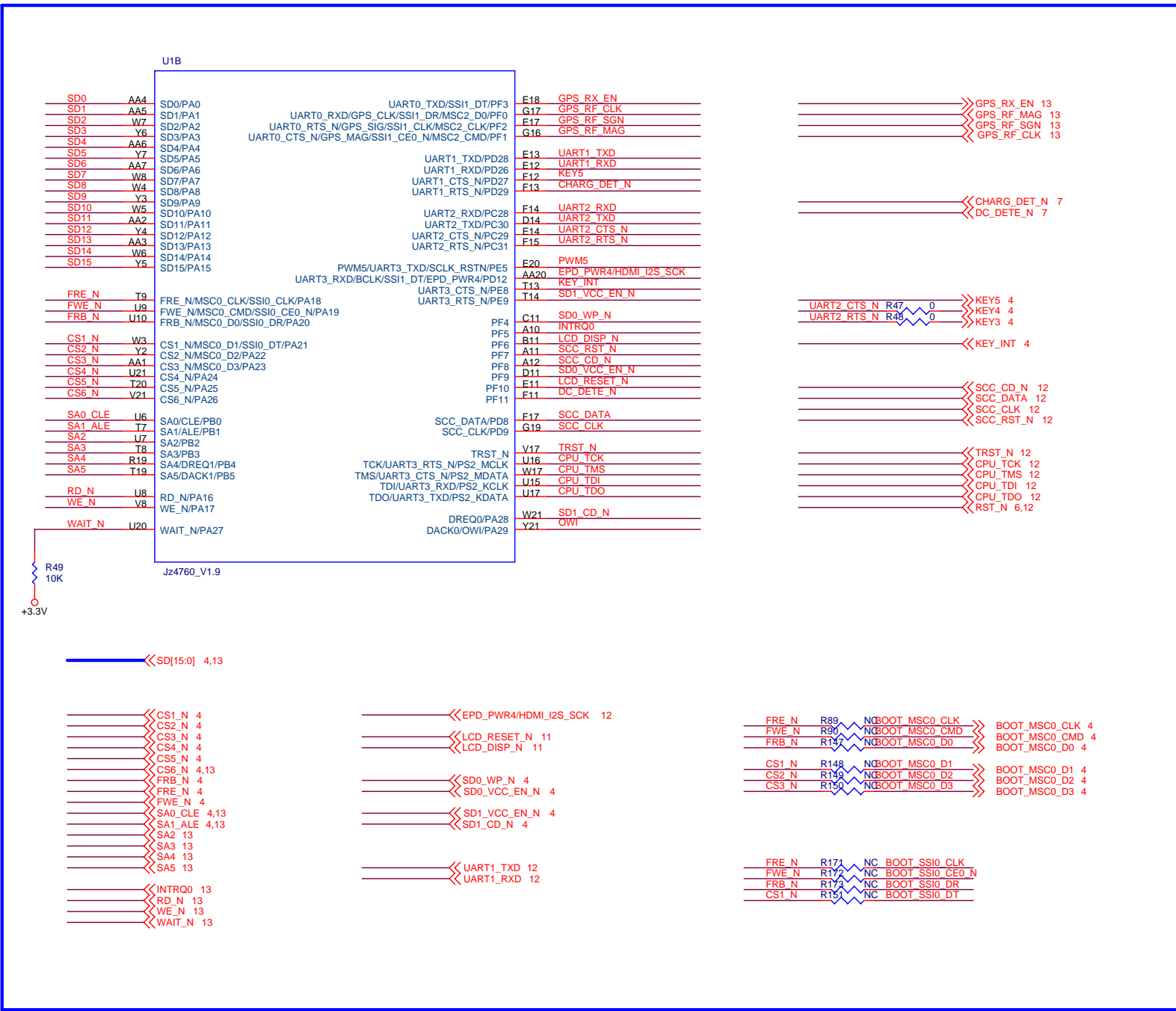


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Boot Mode Select

BOOT_SEL[2:1:0]	Setting
100	Boot from SD Card at MMC0
111	Boot from NAND flash at CS1 default setting
110	Boot from USB device
101	Boot from SPI NORFLASH

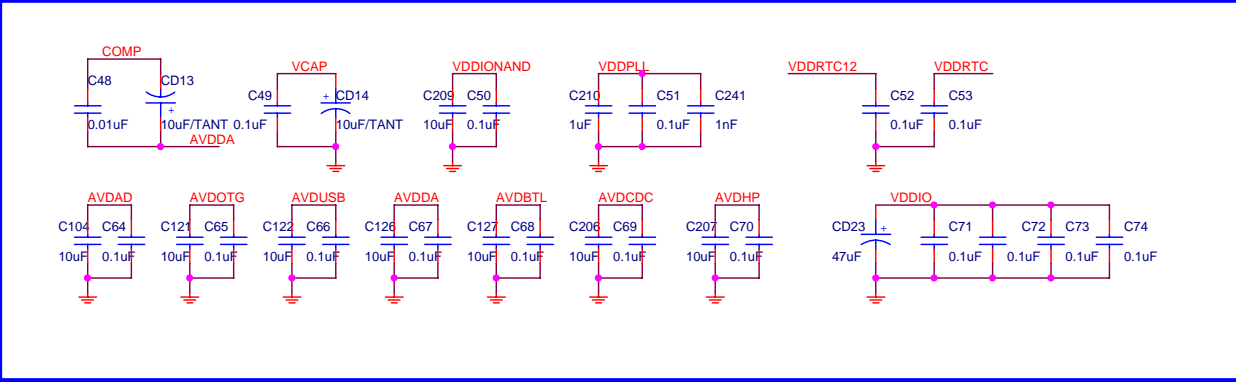
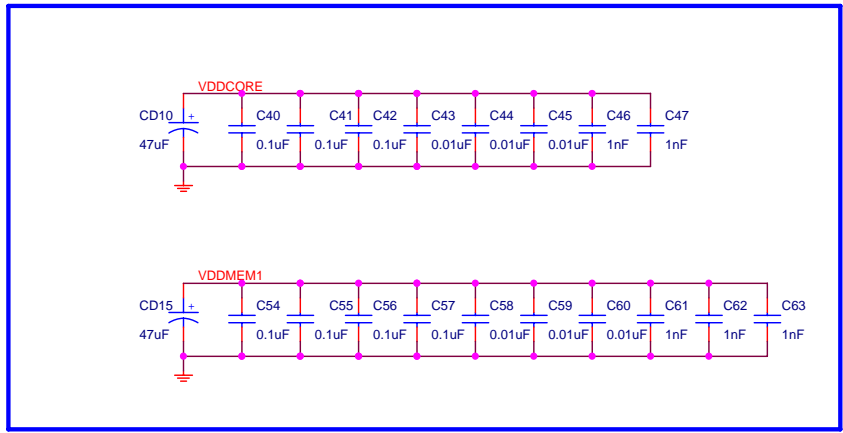
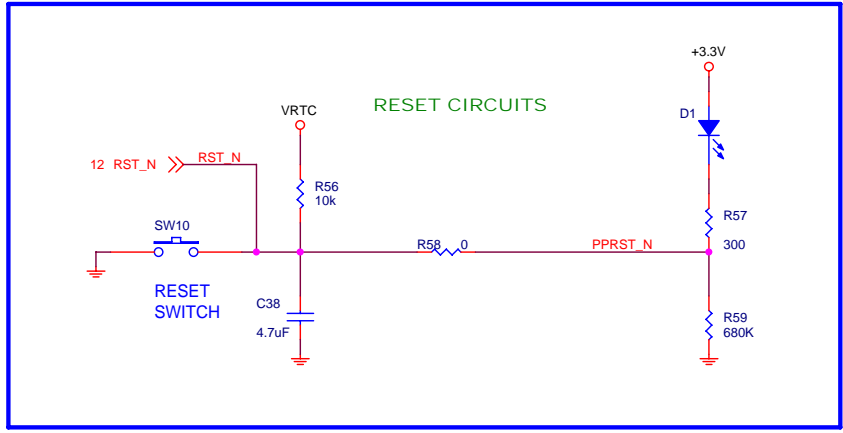
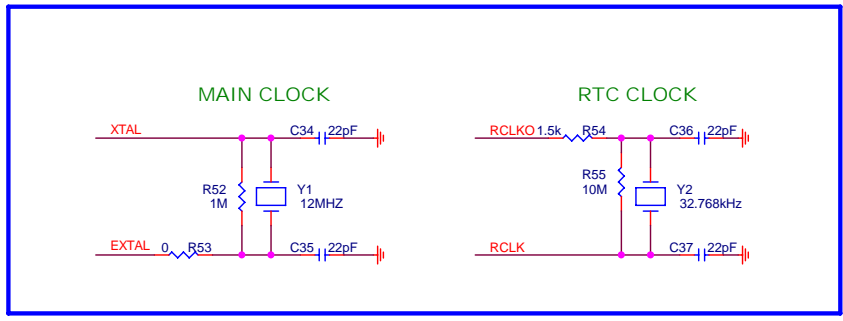
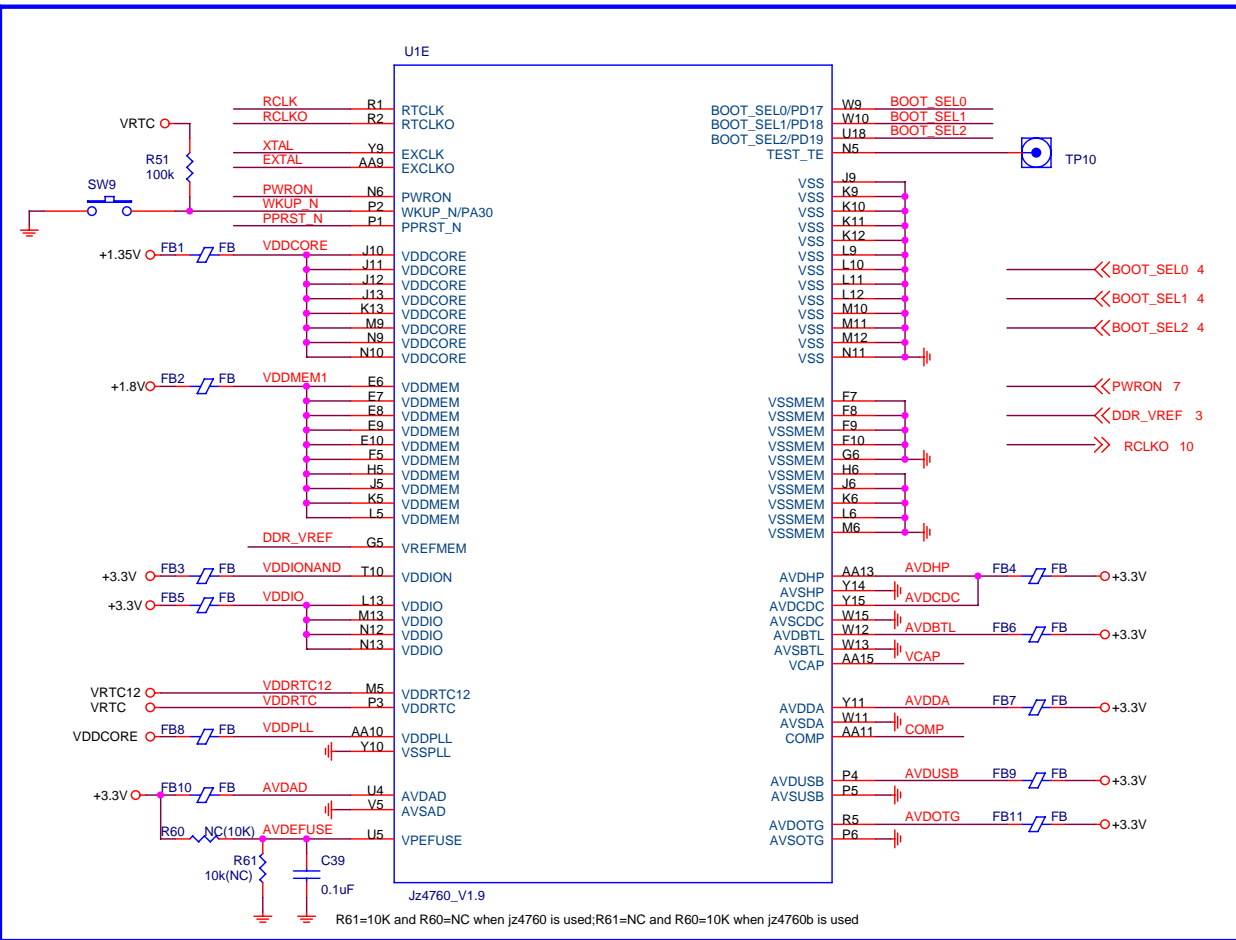


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B	UART/OWI/SPINOR	1.3.1	
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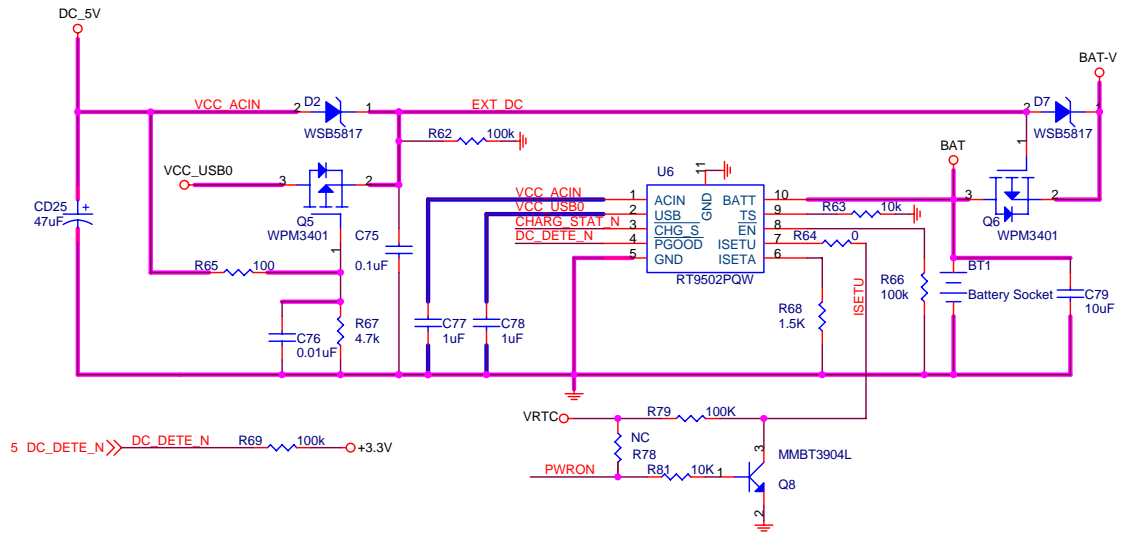
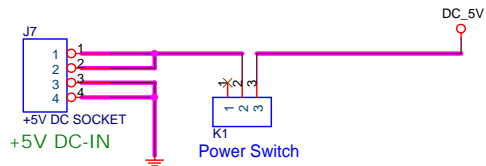
SD[15:0] 4,13

- << CS1_N 4
- << CS2_N 4
- << CS3_N 4
- << CS4_N 4
- << CS5_N 4
- << CS6_N 4,13
- << FRB_N 4
- << FWE_N 4
- << FWE_N 4
- << SA0_CLE 4,13
- << SA1_ALE 4,13
- << SA2 13
- << SA3 13
- << SA4 13
- << SA5 13
- << INTRQ0 13
- << RD_N 13
- << WE_N 13
- << WAIT_N 13
- << EPD_PWR4/HDMI_I2S_SCK 12
- << LCD_RESET_N 11
- << LCD_DISP_N 11
- << SD0_WP_N 4
- << SD0_VCC_EN_N 4
- << SD1_VCC_EN_N 4
- << SD1_CD_N 4
- << UART1_TXD 12
- << UART1_RXD 12
- << NGBOOT_MSC0_CLK
- << NGBOOT_MSC0_CMD
- << NGBOOT_MSC0_D0
- << NGBOOT_MSC0_D1
- << NGBOOT_MSC0_D2
- << NGBOOT_MSC0_D3
- << NC_BOOT_SSI0_CLK
- << NC_BOOT_SSI0_CE0_N
- << NC_BOOT_SSI0_DR
- << NC_BOOT_SSI0_DT
- << BOOT_MSC0_CLK 4
- << BOOT_MSC0_CMD 4
- << BOOT_MSC0_D0 4
- << BOOT_MSC0_D1 4
- << BOOT_MSC0_D2 4
- << BOOT_MSC0_D3 4

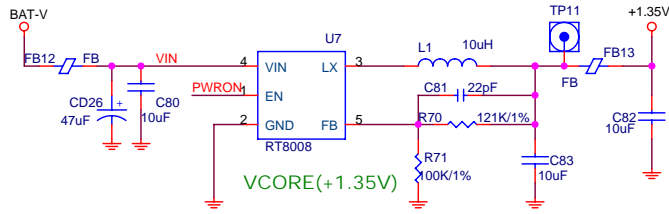
- << KEY5 4
- << KEY4 4
- << KEY3 4
- << KEY_INT 4
- << TRST_N 12
- << CPU_TCK 12
- << CPU_TMS 12
- << CPU_TDI 12
- << CPU_TDO 12
- << RST_N 6,12
- << SCC_CD_N 12
- << SCC_DATA 12
- << SCC_CLK 12
- << SCC_RST_N 12
- << SD0_WP_N
- << LCD_DISP_N
- << SCC_RST_N
- << A12 SCC_CD_N
- << D11 SD0_VCC_EN_N
- << E11 LCD_RESET_N
- << F11 DC_DETE_N
- << F17 SCC_DATA
- << G19 SCC_CLK
- << V17 TRST_N
- << U16 CPU_TCK
- << W17 CPU_TMS
- << U15 CPU_TDI
- << U17 CPU_TDO
- << W21 SD1_CD_N
- << Y21 OWI
- << GPS_RX_EN 13
- << GPS_RF_CLK 13
- << GPS_RF_SGN 13
- << GPS_RF_MAG 13
- << GPS_RF_CLK 13
- << UART1_TXD
- << UART1_RXD
- << KEYS
- << CHARG_DET_N 7
- << DC_DETE_N 7
- << PWM5
- << EPD_PWR4/HDMI_I2S_SCK
- << KEY_INT
- << SD1_VCC_EN_N
- << C11 SD0_WP_N
- << A10 INTRQ0
- << B11 LCD_DISP_N
- << P16 SCC_RST_N
- << P17 A12 SCC_CD_N
- << P18 D11 SD0_VCC_EN_N
- << P19 E11 LCD_RESET_N
- << P10 F11 DC_DETE_N
- << P11 F17 SCC_DATA
- << P11 G19 SCC_CLK
- << P17 TRST_N
- << U16 CPU_TCK
- << W17 CPU_TMS
- << U15 CPU_TDI
- << U17 CPU_TDO
- << W21 SD1_CD_N
- << Y21 OWI



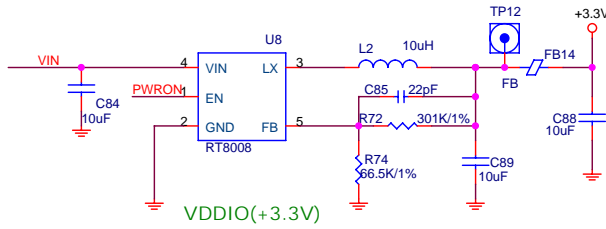
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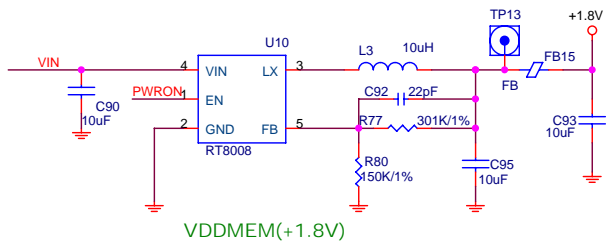
Power Input Charge Circuit



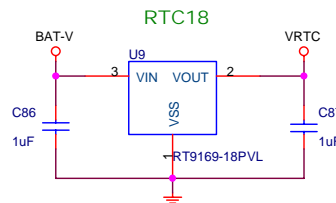
VCORE(+1.35V)



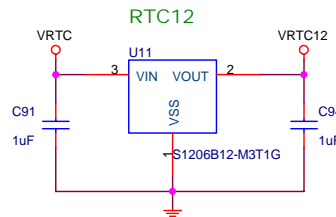
VDDIO(+3.3V)



VDDMEM(+1.8V)

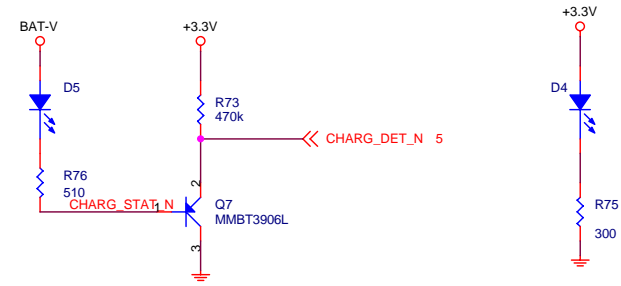


RTC18



RTC12

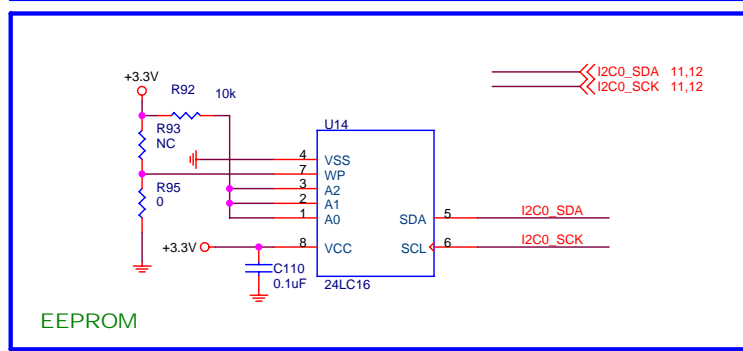
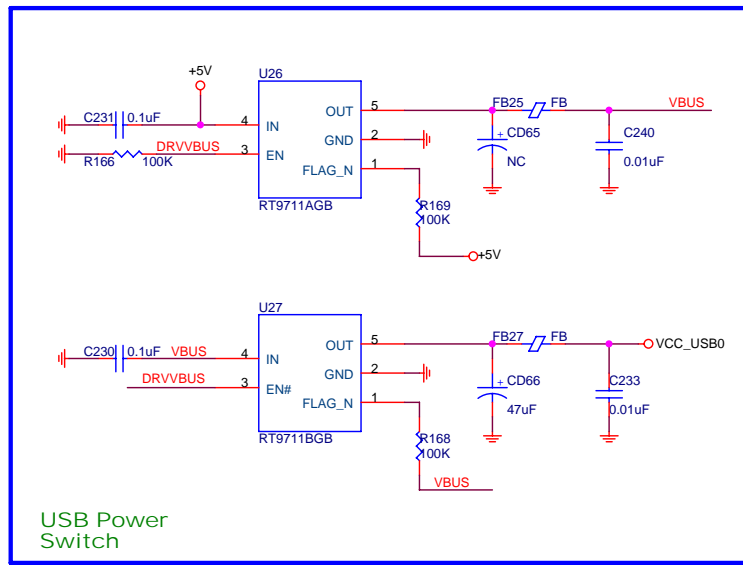
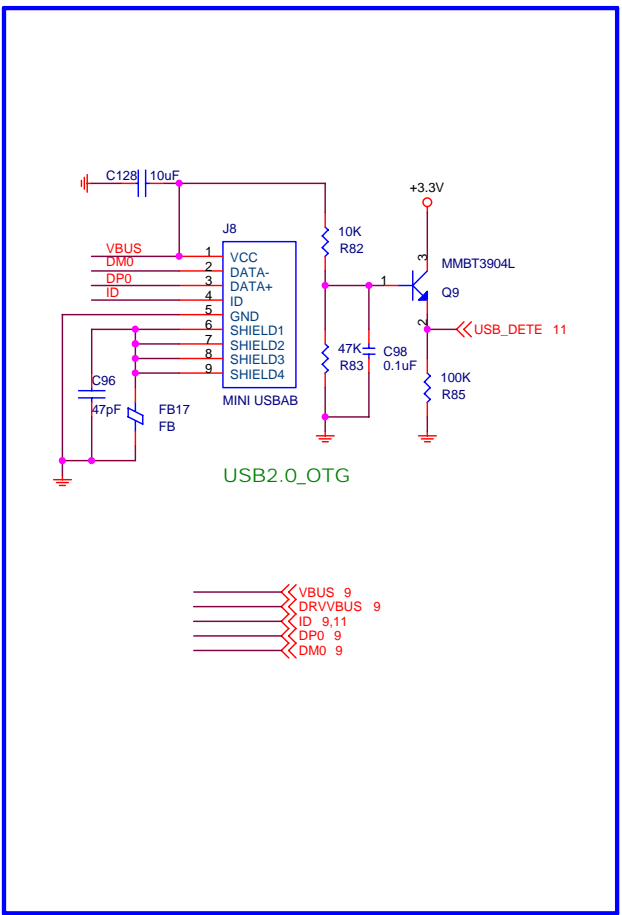
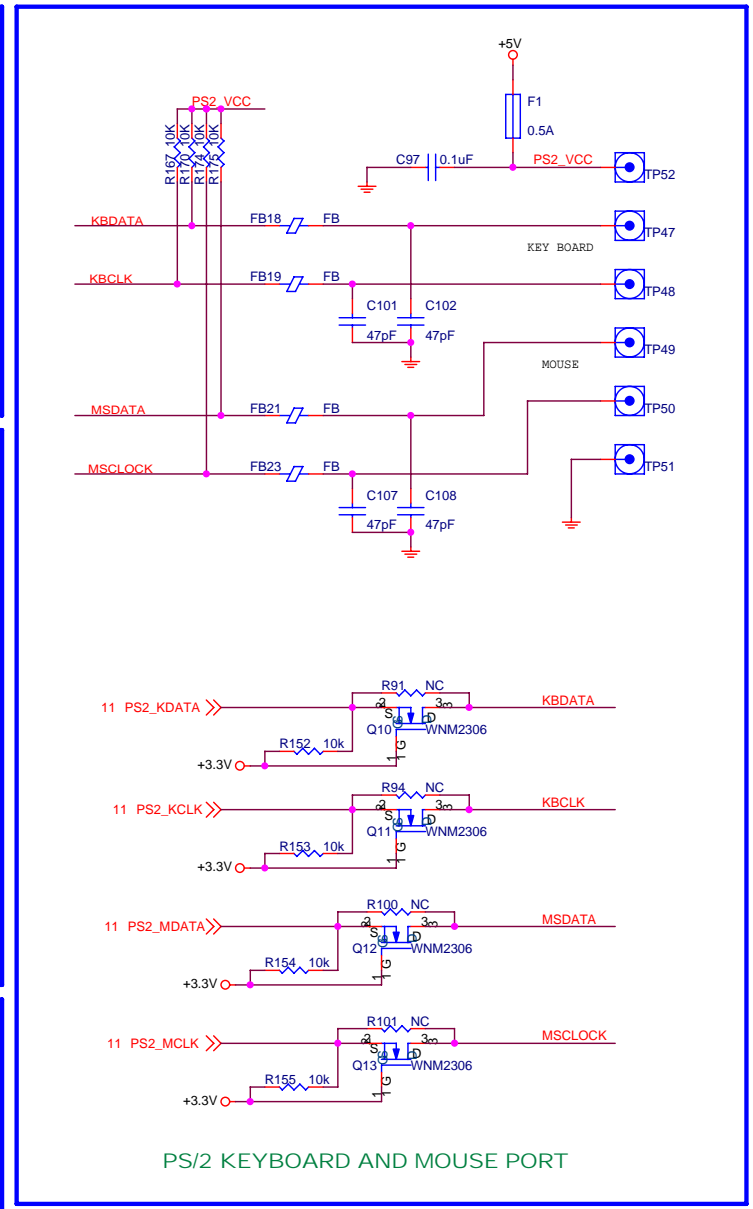
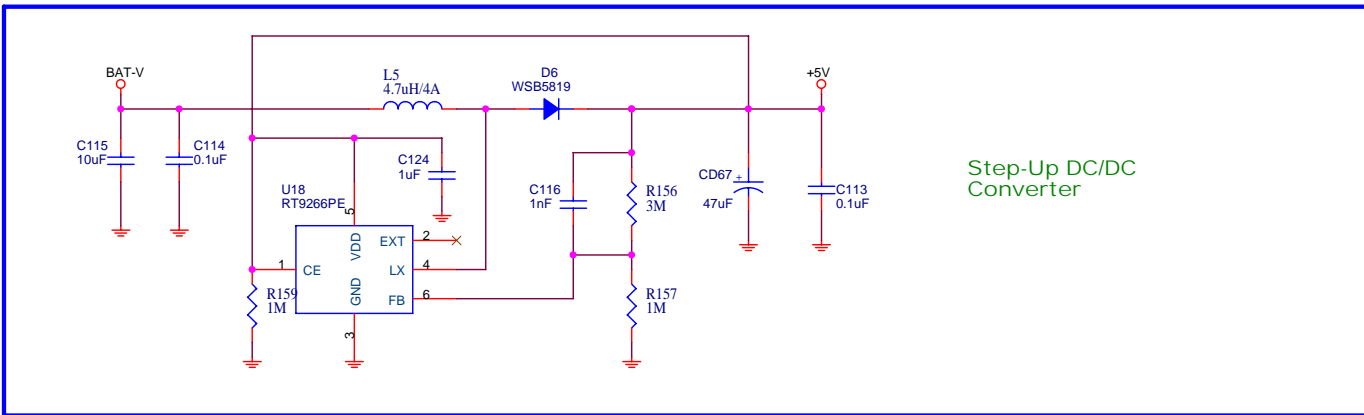
VRTC



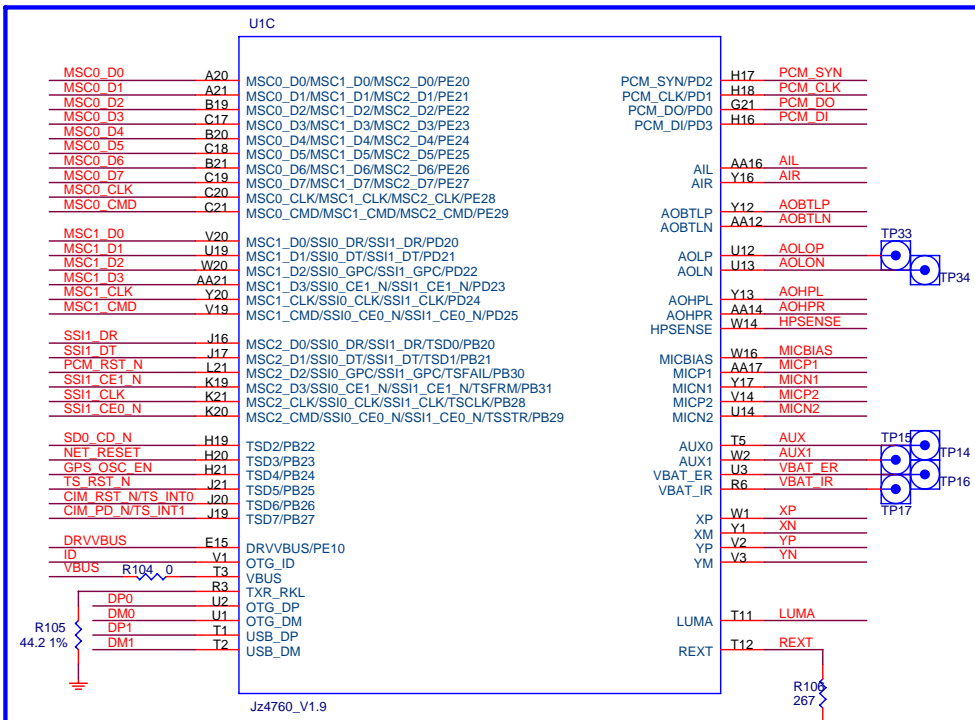
Power Supply & Charge state Indicators

INGENIC SEMICONDUCTOR CO.,LTD

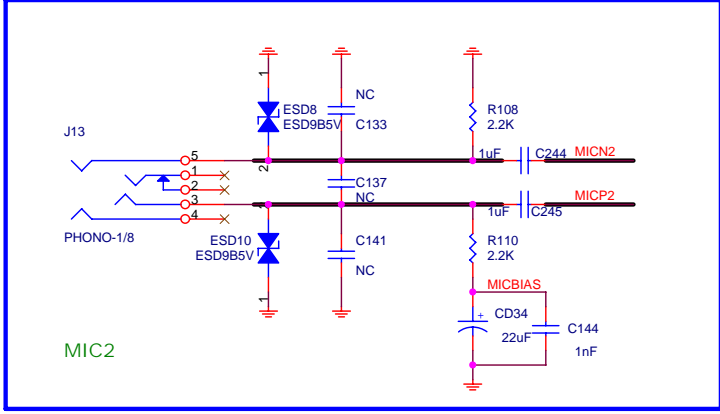
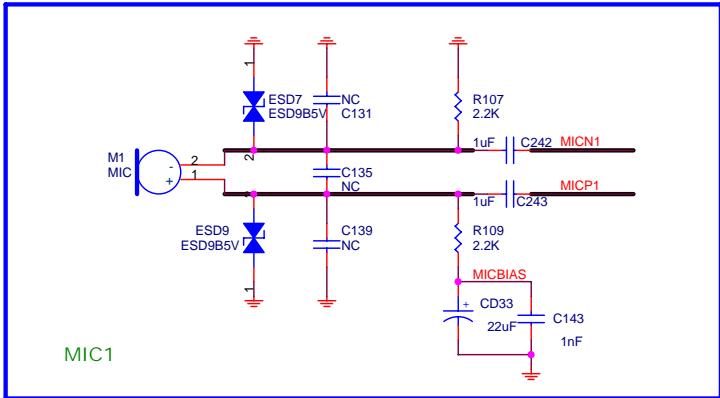
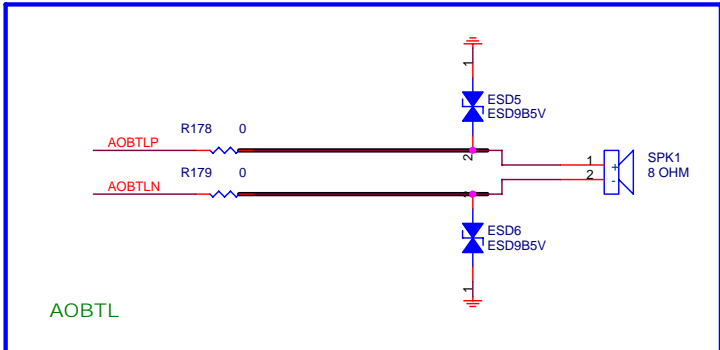
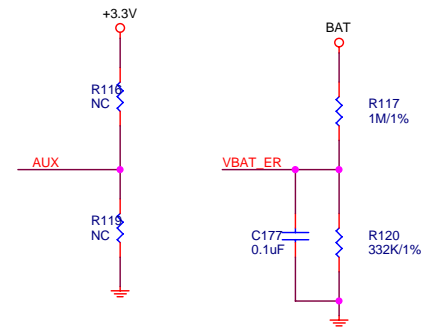
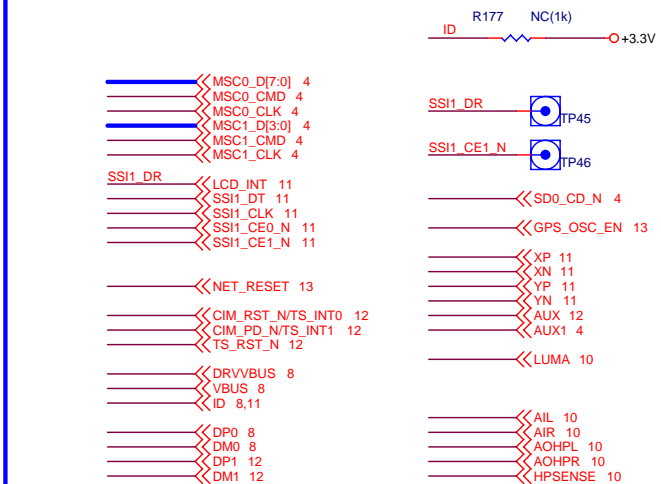
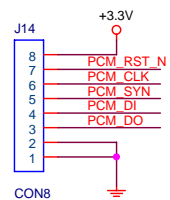
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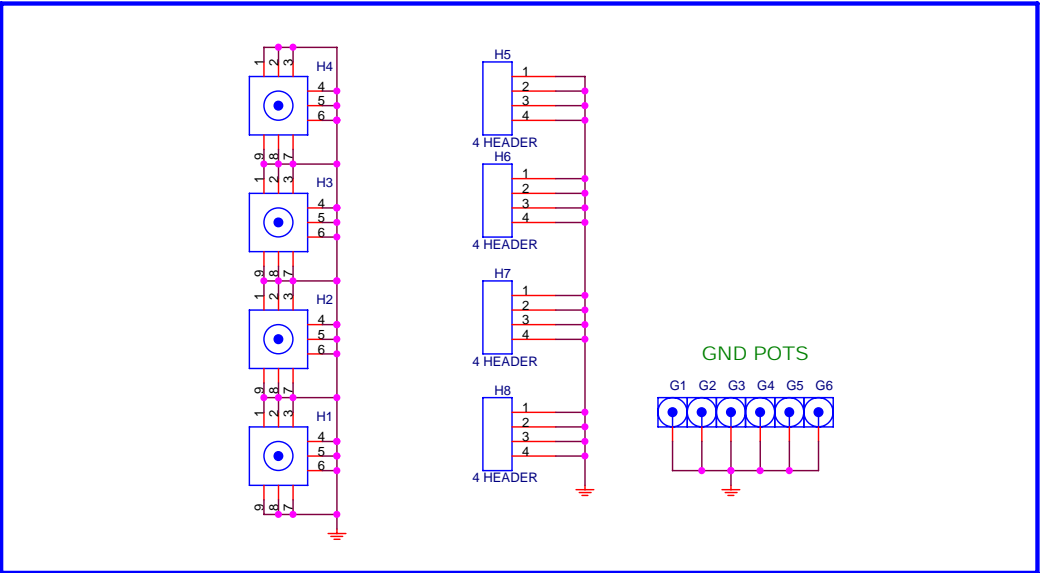
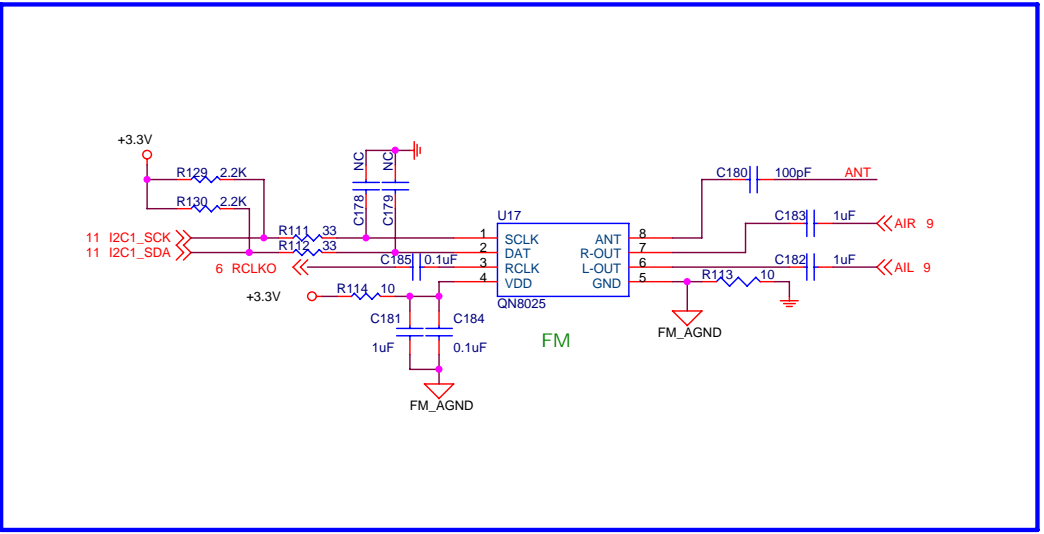
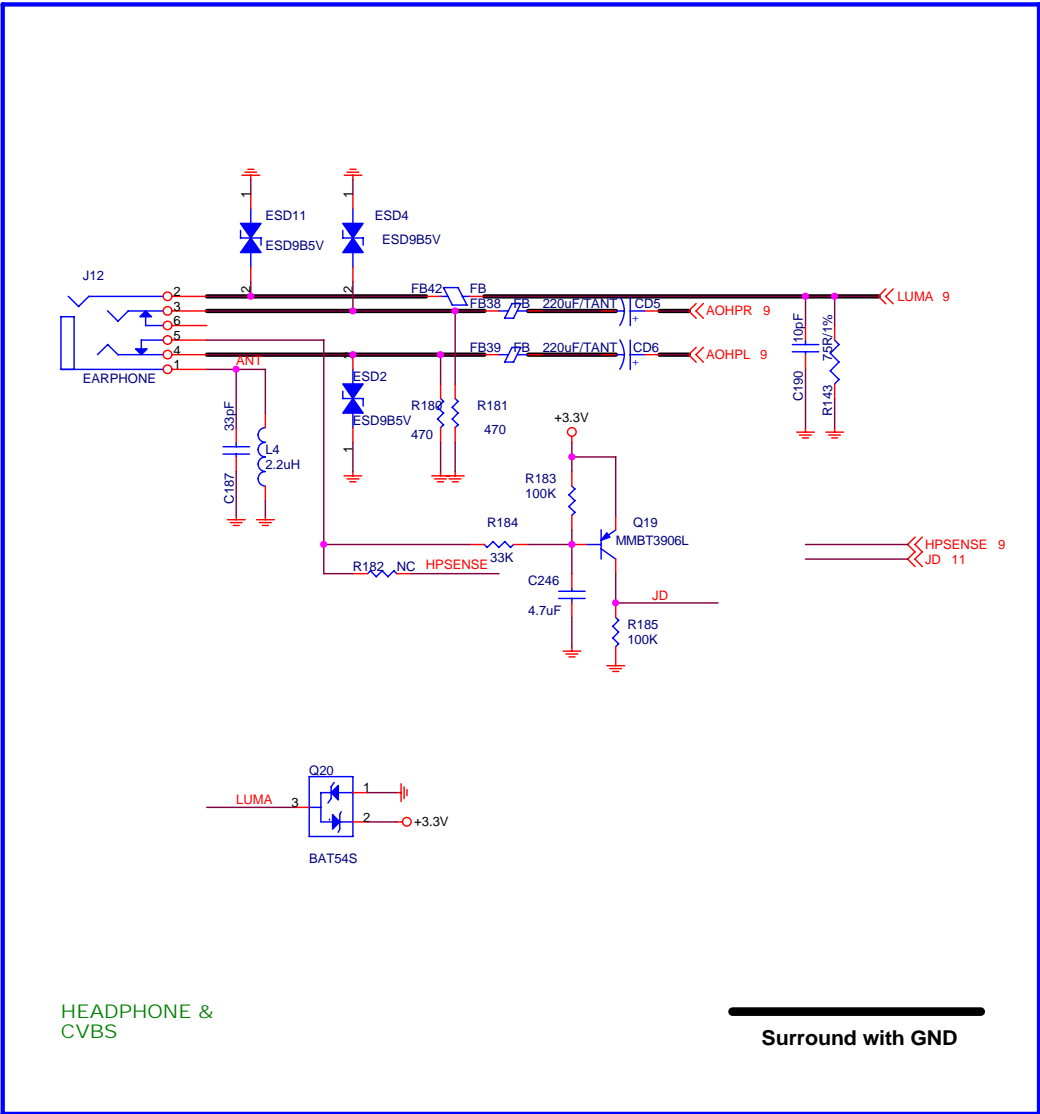
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B	USB OTG/EEPROM/PS2	1.3.1
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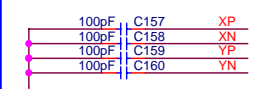
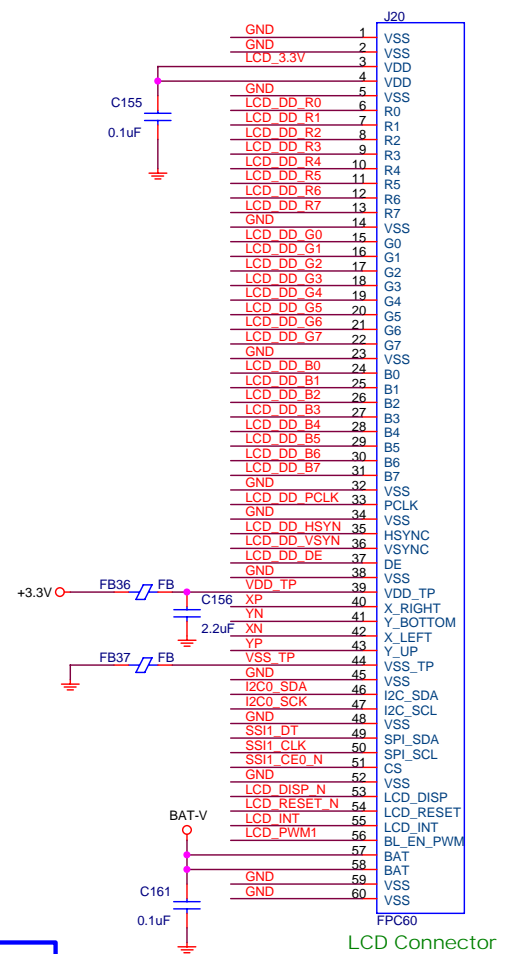
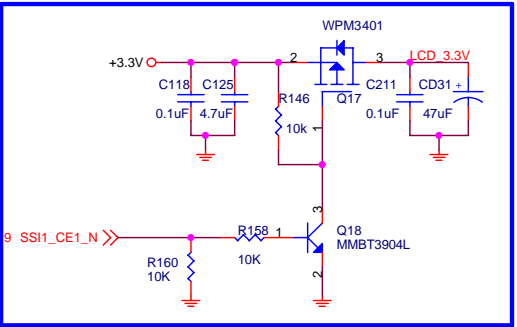
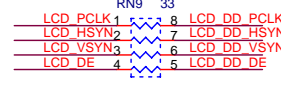
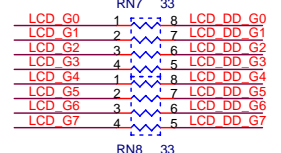
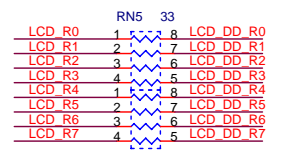
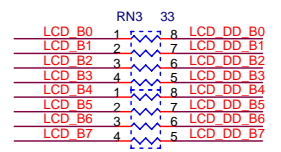
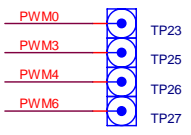
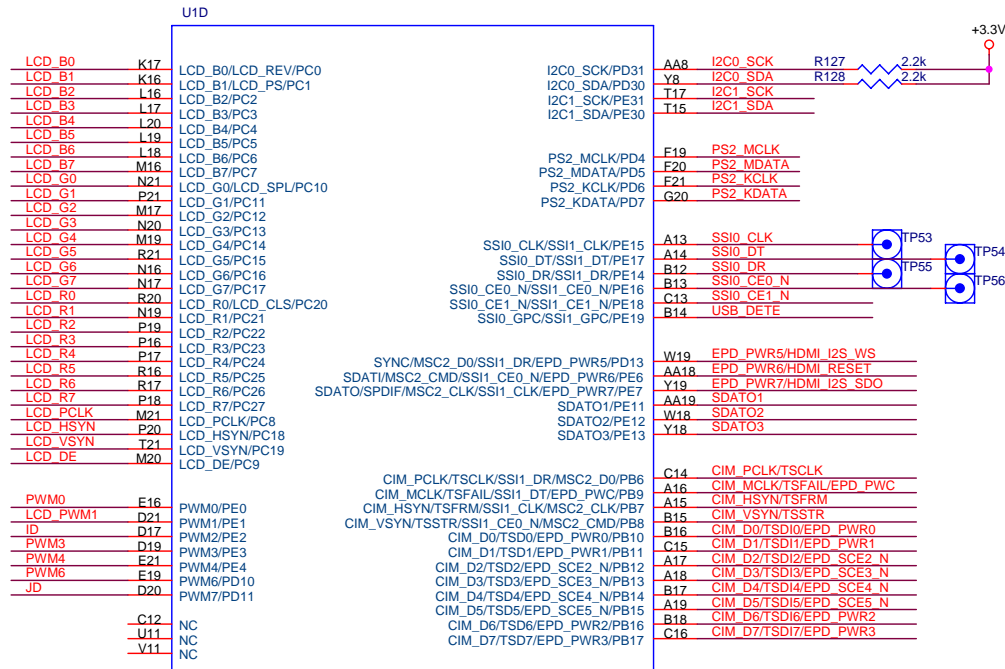
PCM CODEC CONNECT



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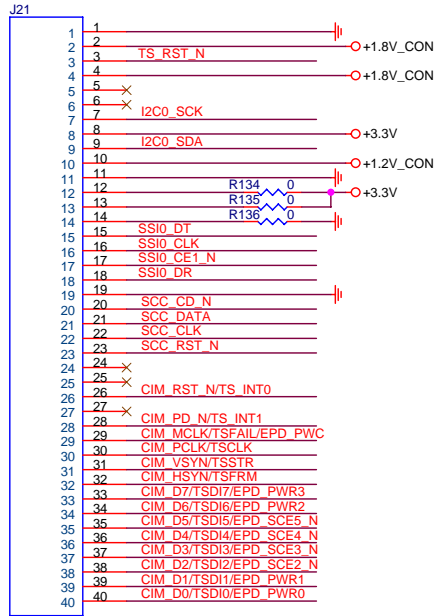
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Title: RD4760_LEPUS

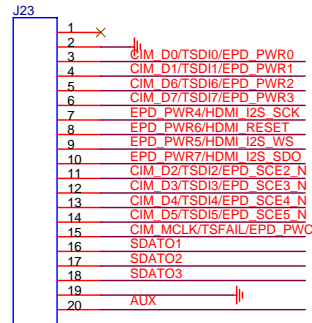
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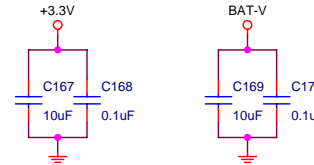
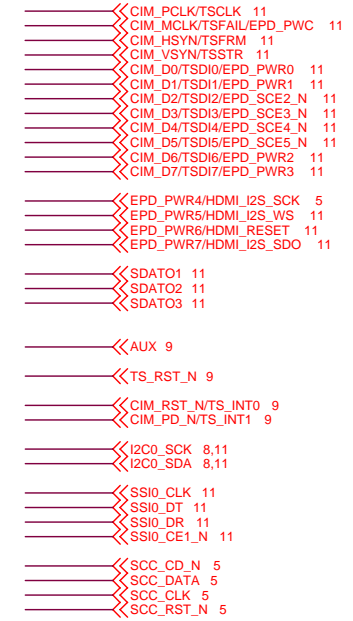
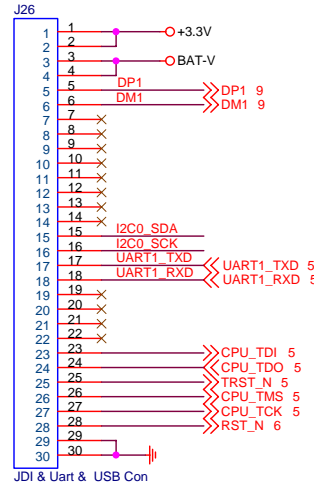
TS/Camera Interface Connector



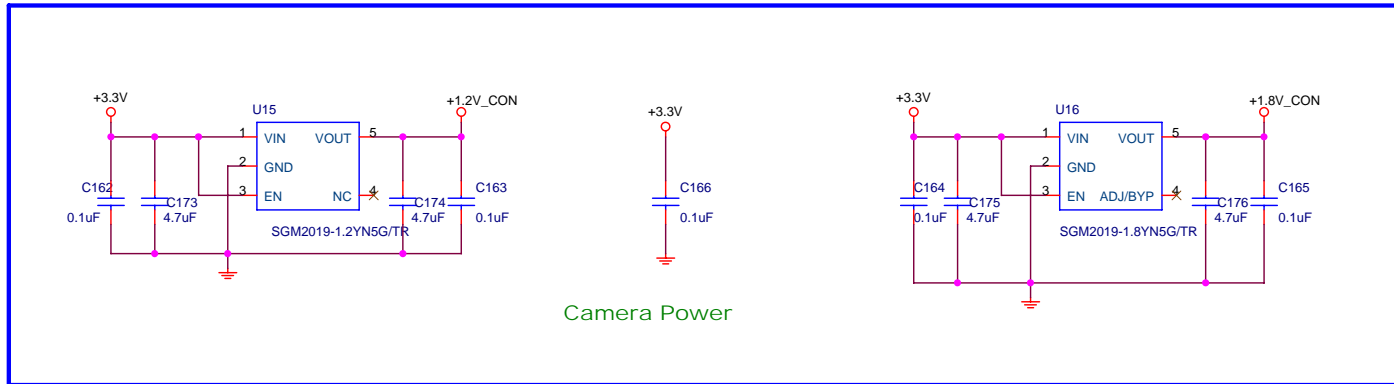
EPD/HDMI Connector



JDI & Uart & USB HOST

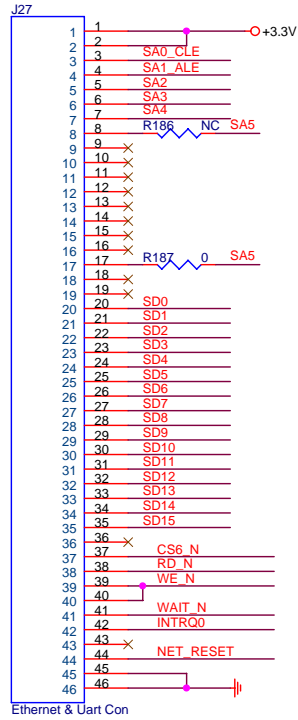


Camera Power

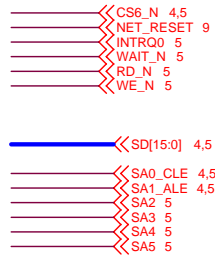


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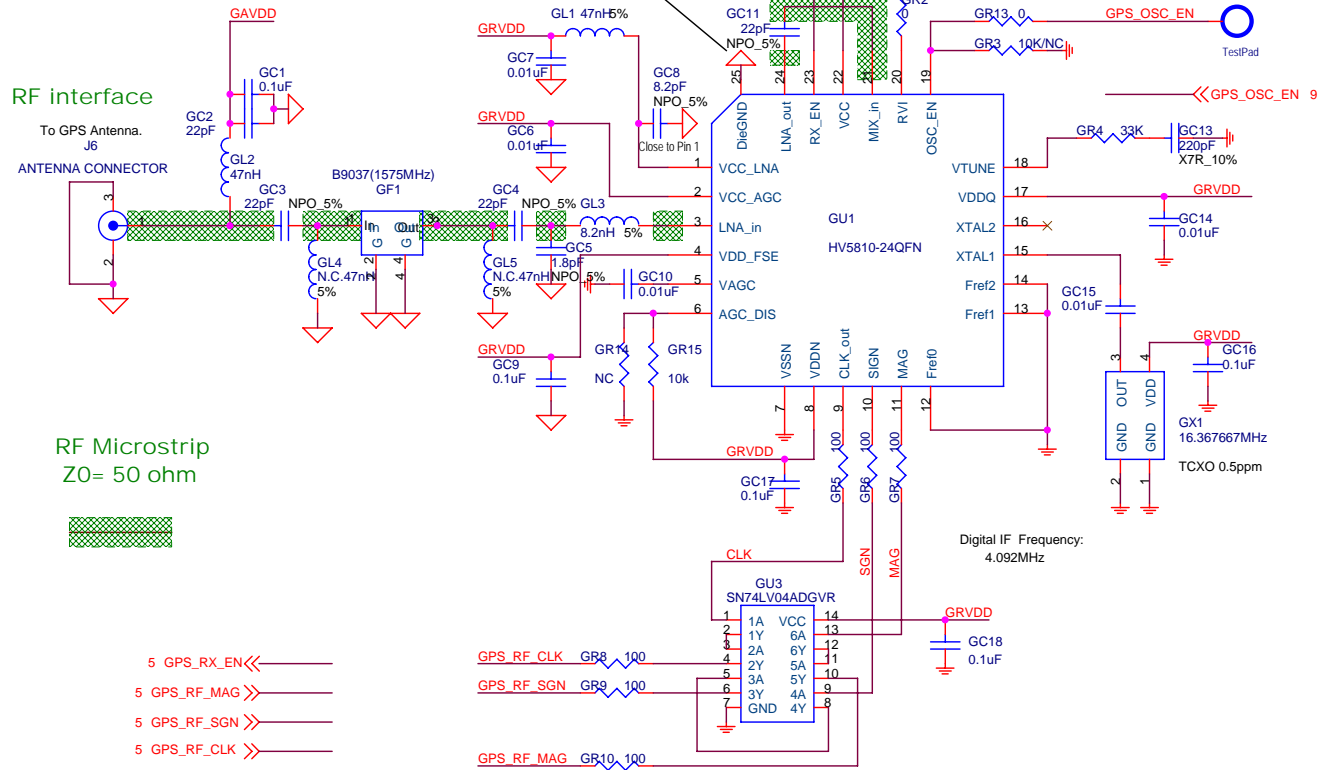


Ethernet



GPS RF Receiver core
Must be placed into RF shielding case

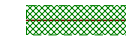
For good grounding, put 9 vias under RF IC die ground pad Pin25.



Operation Mode Description:

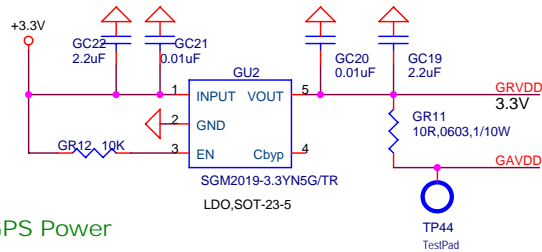
RX_EN	OSC_EN	Mode
0	0	All stand by
0	1	Oscillator only
1	0	Full active (external reference)
1	1	Full active (internal oscillator)

RF Microstrip
Z0= 50 ohm



Digital IF Frequency:
4.092MHz

GPS Power



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Data

Revision

Change

Data	Revision	Change
Apr.20 2010	Rev1.0	1. First released Revision
May.21 2010	Rev1.1	<ol style="list-style-type: none"> 1. Change jz4760_V1.6 to jz4760_V1.8 2. Remove reset chip IMP811 on PAGE6 3. Delete net name PWM0 on PAGE7 4. Change VRTC chip U9 from RT9169-33PVL to RT9169-18PVL on PAGE7 5. Change pullup signal on net CHARG_STAT_N from VRTC33 to BAT-V on PAGE7 6. Change U27 from RT9179AGB to RT9179BGB and controll is DRVVBUS on PAGE8 7. Add 1Kohm ID pullup resistance to +3.3V on PAGE9 8. Add C242~C245 for MIC1,MIC2 on PAGE9 9. Adjust C131~C142 to NC on PAGE9 10. Remove U19,R176,C117 on PAGE8 11. Change 8bit and 4bit SD/MMC card pullup resistance to 10Kohm on PAGE4 12. Change left and right channel of J12 on PAGE10 13. Change C204,C205 to R178,R179 on PAGE9 14. Remove C198~C203 on PAGE9 15. Remove C132,C136,C140 on PAGE9 16. Remove C134,C138,C142 on PAGE9 17. Change C193,C194 to R180,R181 on PAGE10 18. Change C143,C144 from 0.1uF to 1nF on PAGE10 19. Add GR14,GR15 for GU1 on PAGE14
Jun.24 2010	Rev1.1.1	<ol style="list-style-type: none"> 1. Change R23 R27 to NC on PAGE3 2. Change net on SW11 from aux to aux1 on PAGE4 3. Change GF1 to BF9037 on PAGE14 4. Add insert detection net JD and adjust net HPSENSE on PAGE10 5. Adjust c43~c45 c58~c60 to 0.01uF and c46~c47 c61~c63 to 1nF on PAGE6
Jul.15 2010	Rev1.1.2	<ol style="list-style-type: none"> 1. Change jz4760_V1.8 to jz4760_V1.9 2. Delete net CHROMA_U and CHROMA_V on PAGE 10 3. Delete VGA output circuit
Jul.23 2010	Rev1.2	<ol style="list-style-type: none"> 1. Change D6 from MBR0520 to WSB5819 on PAGE08 2. Adjust LUMA output to AUDIO JACK 12 and delete J24 on PAGE10 3. Add insert detection circuit on PAGE10
Oct.29 2010	Rev1.2.1	<ol style="list-style-type: none"> 1. Adjust R59 to 680K,R117 to 1M,R120 to 332K and R78,R93 to NC for power loose on PGAE6 and PAGE9
Nov.5 2010	Rev1.3	<ol style="list-style-type: none"> 1. Delete two test point TP8 TP9 and add SA0 SA4 and SA5 for ethernet test on PAGE5 2. Add R186,R187 for ethernet test on PAGE13 and adjust R70 to 121K on PAGE7
Dec.15 2010	Rev1.3.1	<ol style="list-style-type: none"> 1. Adjust R29 to 100K ohm on PAGE04 2. Adjust +1.2V to +1.35V on PAGE06 and PAGE07 3. Adjust DDR2 module name to H5PS1G63EFR-G7C on PAGE03 4. Add note of AVDEFUSE on PAGE06 5. Adjust C11 to NC and add note for mDDR on PAGE03 6. Adjust U11 to S1206B on PAGE07

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B	REVISION HISTORY	1.3.1
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