

# Ingenic<sup>®</sup> JZ4760

## Board Design Guide

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北京君正集成电路股份有限公司  
Ingenic Semiconductor Co., Ltd.

# Ingenic JZ4760

## Board Design Guide

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July. 2010	1.0	First release
Nov.2010	1.1	1. Change the pin's name of LCD 2. Increase the notes for use AUX0 3. Increase OTP EFUSE

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## Content

1	Overview .....	1
1.1	Introduction .....	1
1.2	Reference Platform .....	2
2	Platform Stack-Up and Placement .....	3
2.1	General Design Considerations .....	3
2.2	Nominal 6-Layer Board Stack-Up .....	3
2.3	PCB Technology Considerations .....	4
3	Static Memory Interface Design Guidelines .....	6
3.1	Overview .....	6
3.2	Boot Memory .....	6
3.3	NAND Flash Connection .....	7
4	DDR2 SDRAM .....	8
4.1	Overview .....	8
4.2	Connection to two 1Gb x 16 DDR2 SDRAM device .....	8
4.3	Layout Guideline .....	8
5	Audio Design Guidelines .....	11
5.1	Overview .....	11
5.2	Audio Power .....	11
5.3	Headphone Out .....	12
5.4	Mic In and Line In .....	13
5.5	Speaker .....	14
5.6	Layout Guideline .....	14
6	Video Design Guidelines .....	16
6.1	Overview .....	16
6.2	Video Power .....	16
6.3	TV Out .....	17
7	USB and OTG Design Guidelines .....	18
7.1	USB Overview .....	18
7.1.1	USB Power .....	18
7.2	OTG Overview .....	18
7.2.1	OTG Power .....	18
7.3	The following are general guidelines for the USB and OTG interface: .....	20
8	LCD .....	22

9	Camera.....	24
10	PS/2 and Keyboard .....	25
10.1	Overview.....	25
11	SAR A/D Controller.....	26
11.1	Overview.....	26
11.2	Touch Screen.....	26
11.3	Battery Voltage Measurement.....	27
12	OTP EFUSE .....	28
12.1	Overview.....	28
13	Ethernet Design Guidelines.....	29
13.1	Overview.....	29
13.2	JZ4760 Ethernet Controller Connection.....	29
14	RTC .....	30
14.1	Overview.....	30
14.2	RTC Clock .....	30
14.3	Power Control.....	30
15	Miscellaneous Peripheral Design Guidelines .....	32
15.1	SSI Design Guideline .....	32
15.2	UART/IrDA.....	33
15.2.1	UART Implementation.....	33
15.2.2	IrDA Implementation .....	33
15.3	I2C Bus.....	34
15.4	PWM.....	34
15.5	GPIO.....	35
15.6	JTAG/Debug Port .....	35
16	Platform Clock Guidelines .....	36
17	Platform Power Guidelines .....	37
17.1	Overview.....	37
17.2	Power Delivery and Decoupling .....	37

# 1 Overview

JZ4760 is a multimedia application processor designed by INGENIC®, which targeting for multimedia rich and mobile devices like Smart phone, PMP, mobile digital TV and GPS. This SOC introduces innovative dual-core architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit/8-bit/12-bit/16-bit/24-bit ECC MLC/TLC NAND flash memory for cost sensitive applications. JZ4760 also integrates DDR ( including DDR, DDR2 and Mobile DDR) memory controller, LCD controller, Audio Codec, multi-channel SAR-ADC, AC97/I2S controller, Camera controller, PCM interface, TV encoder, TS interface, MMC/SD/SDIO host controller, high speed SPI, I2C, One-wire, PS2 interface, USB1.1 Host, USB OTG, UART, IrDA, GPIO and so on.

## 1.1 Introduction

This design guide provides recommendations for system designs based on the JZ4760 processor. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor.

The design guidelines in this document are used to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** Items based on INGENIC's simulations and lab experience to date are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by INGENIC. They should be used as an example, but may not be applicable to particular designs.

**Note:** In this manual, processor means the JZ4760 processor if not specified.

The guidelines recommended in this manual are based on experience and simulation work completed by INGENIC while developing systems with JZ4760. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

## 1.2 Reference Platform

Figure 1-1 shows the JZ4760 Development Board Architecture.

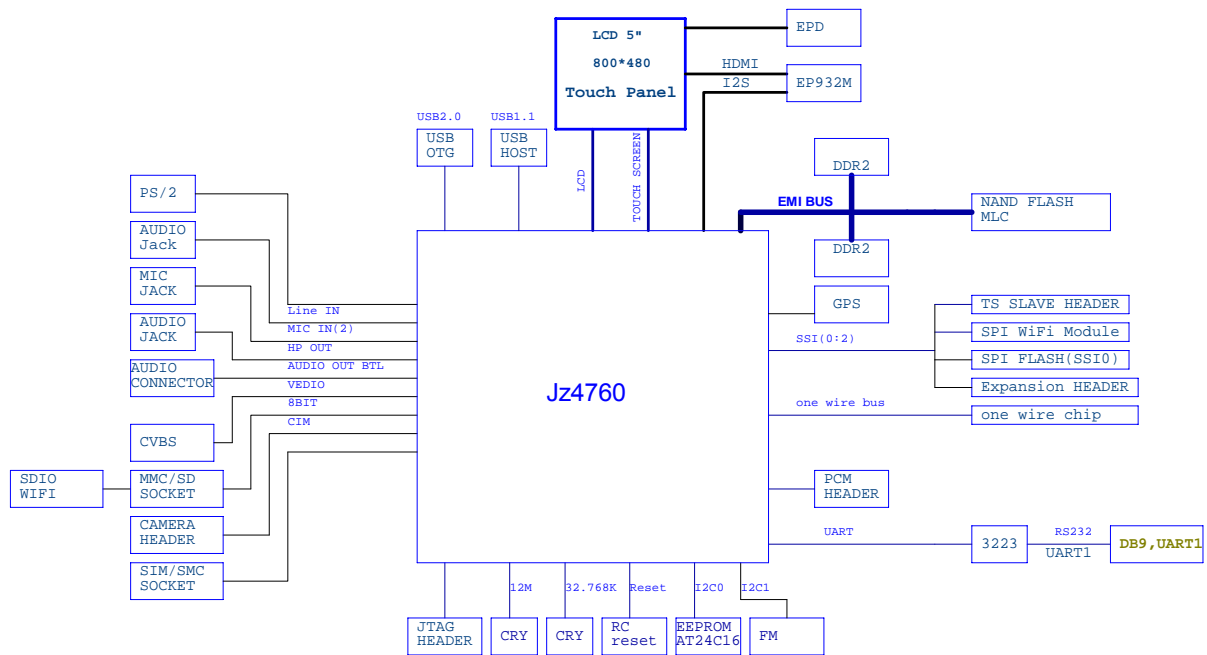


Figure 1-1 JZ4760 Development Board Architecture

## 2 Platform Stack-Up and Placement

In this section, an example of a JZ4760 platform component placement and stack-up is presented for a PMP product.

### 2.1 General Design Considerations

This section describes motherboard layout and routing guidelines for JZ4760 platforms. This section does not describe the function of any bus, or the layout guidelines for an add-in device. If the guidelines listed in this manual are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e.,  $50\Omega \pm 10\%$ ) is the nominal trace impedance for a 4-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time. Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 2-1.

### 2.2 Nominal 6-Layer Board Stack-Up

The JZ4760 platform requires a board stack-up yielding a target board impedance of  $50 \Omega \pm 10\%$ . Recommendations in this design guide are based on the following a 6-layer board stack-up:

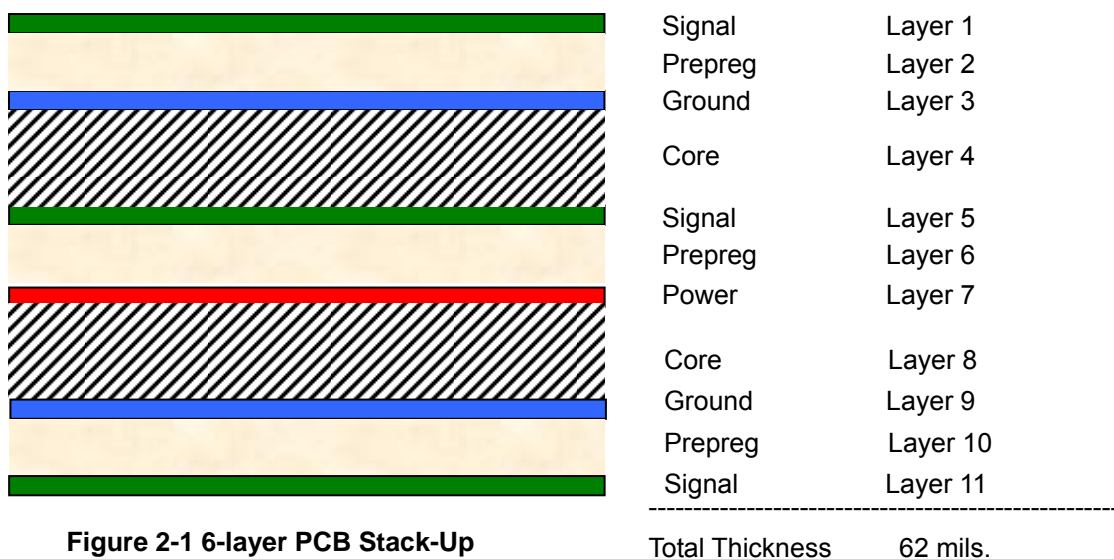


Figure 2-1 6-layer PCB Stack-Up

Table 2-1 PCB Parameter

Description	Nominal Value	Tolerance	Comments
Board Impedance Z0	50Ω	± 10%	With nominal 4 mil trace width
Dielectric Thickness	4.3 mils	± 0.5 mils	1 x 2116 Pre-Preg
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	4.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Soldermask Er	4.0	± 0.5	@ 100 MHz
Soldermask Thickness	1.0 mils	± 0.5 mils	From top of trace

### 2.3 PCB Technology Considerations

The following recommendation aids in the design of a JZ4760 based platform. Simulations and reference platform are based on the following technology, and we recommend that designers adhere to these guidelines.

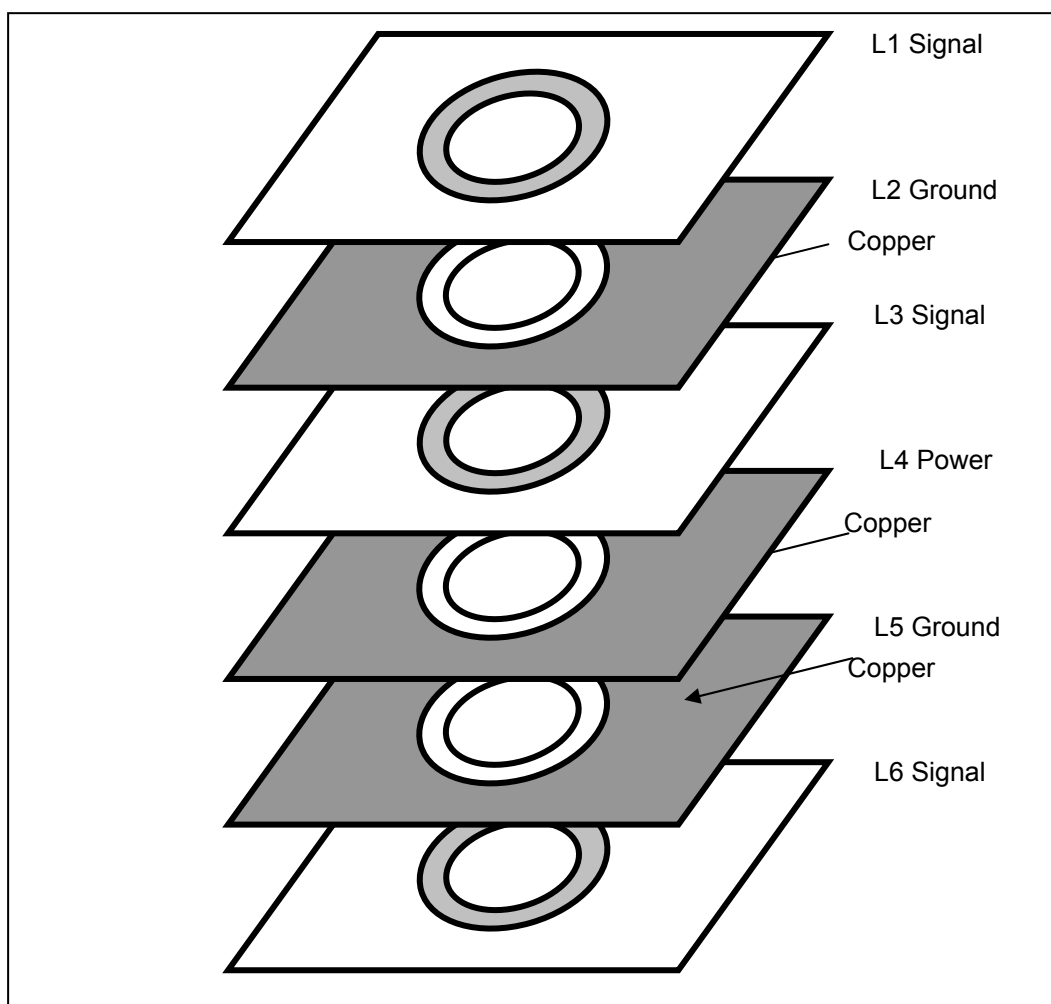


Figure 2-2 PCB Technologies – Stack-Up



**Table 2-2 PCB Parameter for Vias**

<b>Number of Layers</b>	
Stack Up	6 Layer
Cu Thickness	0.5 oz Outer (before plating); 1 oz inner
Final Board Thickness	62 mils (- 5mils / +8mils)
Material	Fiberglass made of FR4
<b>Signal and Power Via Stack</b>	
Via Pad	13 mils
Via Anti-Pad	20 mils
Via Finished Hole	6 mils

## 3 Static Memory Interface Design Guidelines

### 3.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of memory and bus interfaces. It enables the connection of static memory, NAND flash memory, etc., to this processor.

This section is the design guidelines for the external memory interface.

The static memory controller provides a glueless interface to ROM, Burst ROM, NOR Flash and NAND Flash. It supports 6 chips selection CS6 ~1# and each bank can be configured separately. JZ4760 supports most types of NAND flashes, including SLC and MLC/TLC, 8-bit and 16-bit bus width, 512B, 2KB page size. It also support boot from NAND flash. The data bus width for each chip select region may be programmed to be 8-bit, 16-bit.

### 3.2 Boot Memory

BOOT\_SEL[2:0] pins define the boot time configurations as listed in the following table.

**Table 3-1 Boot Configuration**

BOOT_SEL[2]	BOOT_SEL[1]	BOOT_SEL[0]	Description
1	0	0	Boot from SD card: MSC0
1	0	1	Boot from SPI (SPI0/CE0)
1	1	0	Boot from USB with EXCLK = 12MHz
1	1	1	Boot from NAND flash at CS1
0	0	0	Boot from USB with EXCLK = 13MHz
0	0	1	Boot from USB with EXCLK = 26MHz
0	1	0	Boot from USB with EXCLK = 19.2MHz
0	1	1	Boot from NOR flash at CS4

### 3.3 NAND Flash Connection

It supports on CS[6:1], sharing with static memory bank4~bank1.

The following Figure 3-1 is an example of 8-bit NAND Flash Interconnection, Figure3-2 is an example of 16-bit NAND Flash Interconnection.

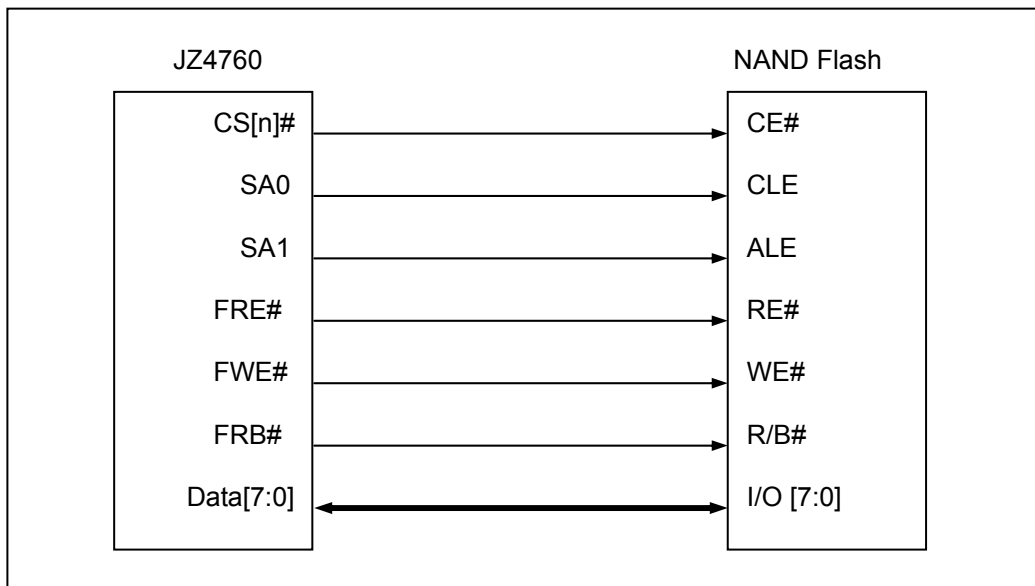


Figure 3-1 8-bit NAND Flash Interconnection Example

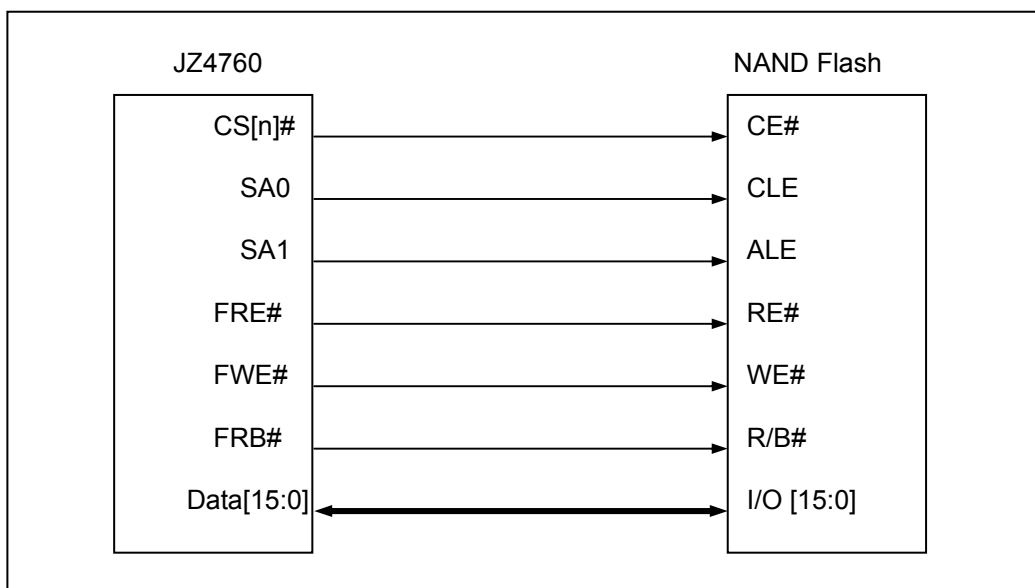


Figure 3-2 16-bit NAND Flash Interconnection Example

## 4 DDR2 SDRAM

### 4.1 Overview

JZ4760 contain a DDR Controller which is a general IP that provide an interface to DDR2, DDR, mobile DDR memory. The following figures give examples on the connection to external DDR2 SDRAM devices.

### 4.2 Connection to two 1Gb x 16 DDR2 SDRAM device

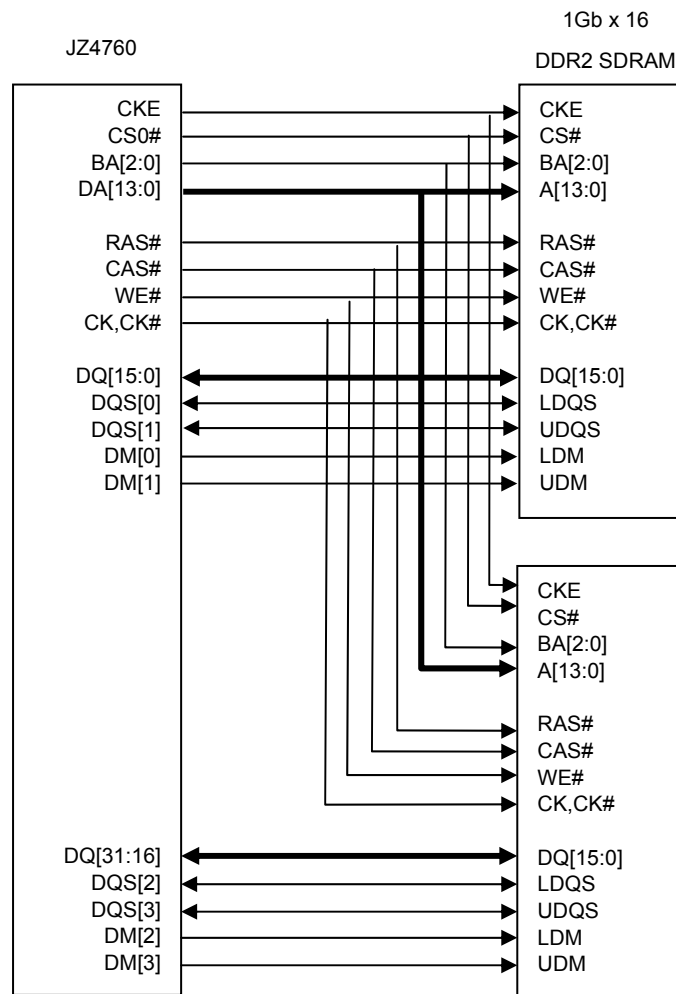


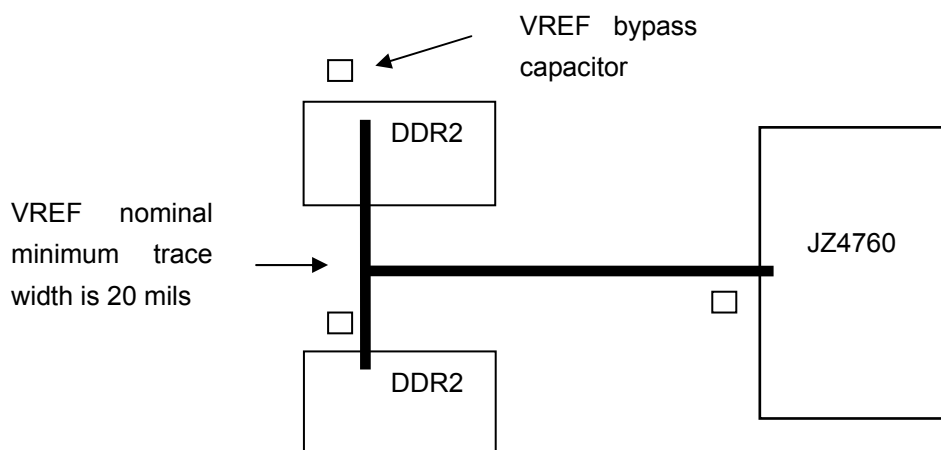
Figure 4-1 Two 16-bit DDR2 Interconnection Example

### 4.3 Layout Guideline

In the classical high-speed flow, to ensure the maximum performance of the DDR2, we should observe the following guidelines. The questions we should be noticed are: Flight time delay and skew, Signal integrity and impedance matching, Crosstalk, Power supply bypassing.

The basic recommendations are as follows:

- The minimum Stack-up required six layer stack. There must have a ground layer to separated two signal layers. Just as describes in Figure 2-2.
- The fundamental high-speed PCB issues are flight time delay and skew. Controlling the maximum placement of components. All of the shorter nets in a clock domain must be match the longest one. Therefore, flight time delay and skew are controlled by the matching of the trace.
- Signal integrity refers to controlling overshoot, ring back, and transition edges. These issues are caused by the mismatch of impedance. Trace impedance is governed by the trace width as well as the thickness and dielectric constant of the PCB insulating materials (usually FR-4). So you should keep the impedance average in a trace, be sure the bending and via as little as possible.
- Crosstalk is fundamentally controlled by the PCB stack-up and minimum trace spacing. The best approach to avoiding a crosstalk problem is to ensure all the signals have high-quality signal return paths and to spread the signal out. Each signal layer should have a nearby full ground plane to provide the shortest return current path. The other aspect of crosstalk control is signal separation, we should keep  $3W$  space between two signals ( $W$  is the width of trace). This method can reduce the crosstalk.
- Precise power supply bypassing is important for high-speed PCB. Control the power supply high-frequency impedance means controlling power supply inductance. Power supply high-frequency impedance is beaten down by many small capacitors connected between the power and ground plane. Using many capacitors, rather than a large one, will reduce the inductance. The inductance of a capacitor is dependant on its size. The capacitor need to be placed very close to the device they are bypassing.
- VREF is used as a reference by the input buffers of the DDR2 memories. It is recommended to be  $1/2$  of the DDR2 power supply voltage and should be created using a resistive divider as shown in the schematic. Other methods are not recommended. Figure 4-2 shows the layout guidelines for VREF.



**Figure 4-2 VREF Routing and Topology**

- The region of the PCB used for DDR2 circuitry must be isolated from other signals. Region should be encompass all DDR2 circuitry and varies signals depending on placement.

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Non-DDR2 signals should not be routed on the DDR2 signal layer with in the DDR2 keep out region. No breaks should be allowed in the reference ground layers in the region. In addition, the +1.8V power plane should cover the entire keep out region.

- Bypassing capacitors should be close to the devices, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

## 5 Audio Design Guidelines

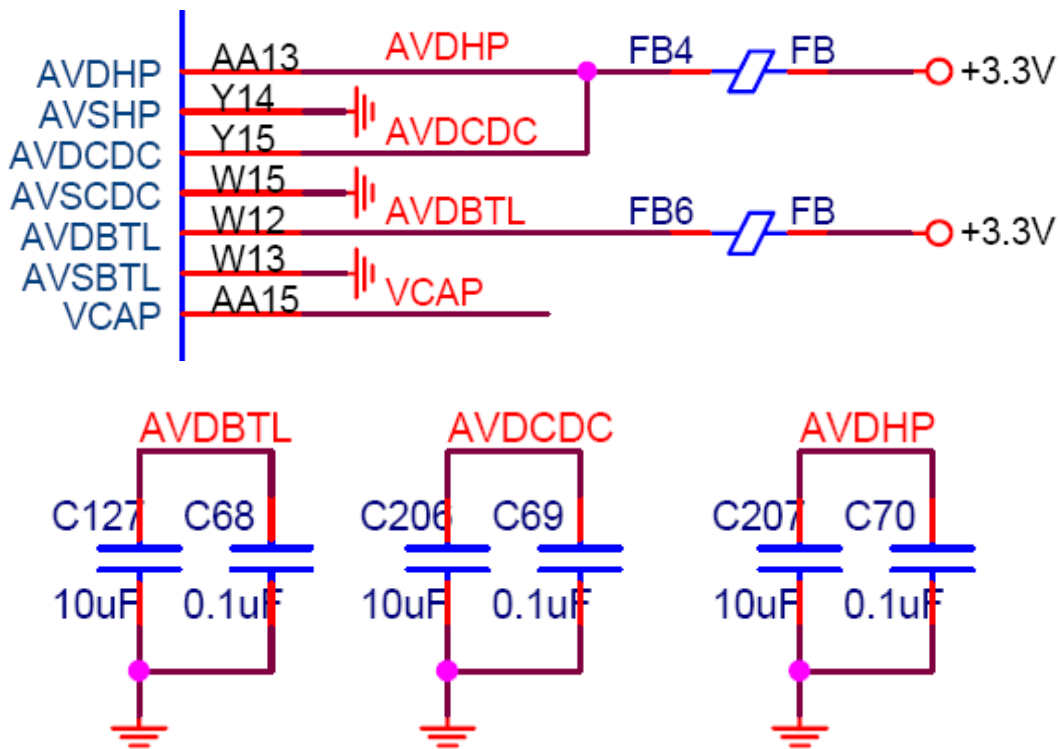
### 5.1 Overview

The AIC(AC'97 and I2S Controller) included in this processor. The AIC supports the Audio Codec '97 Component Specification 2.3 for AC-link format and I2S or IIS (for inter-IC sound), a protocol defined by Philips Semiconductor. Both normal I2S and the MSB-justified I2S formats are supported by AIC.

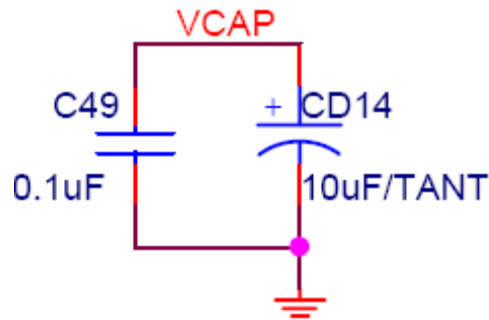
### 5.2 Audio Power

AVDHP, AVDCDC and AVDBTL should be connected to a cleaned +3.3V power.

For a correct working, it is required to connect two decoupling capacitor (10 $\mu$ F and 100nF ceramic) between the pins AVDCDC and AVSCDC.



An electrolytic capacitor more than 10 $\mu$ F tantalum and a 100nF ceramic capacitor should be attached from VCAP to AVSCDC to eliminate the effects of high frequency noise.

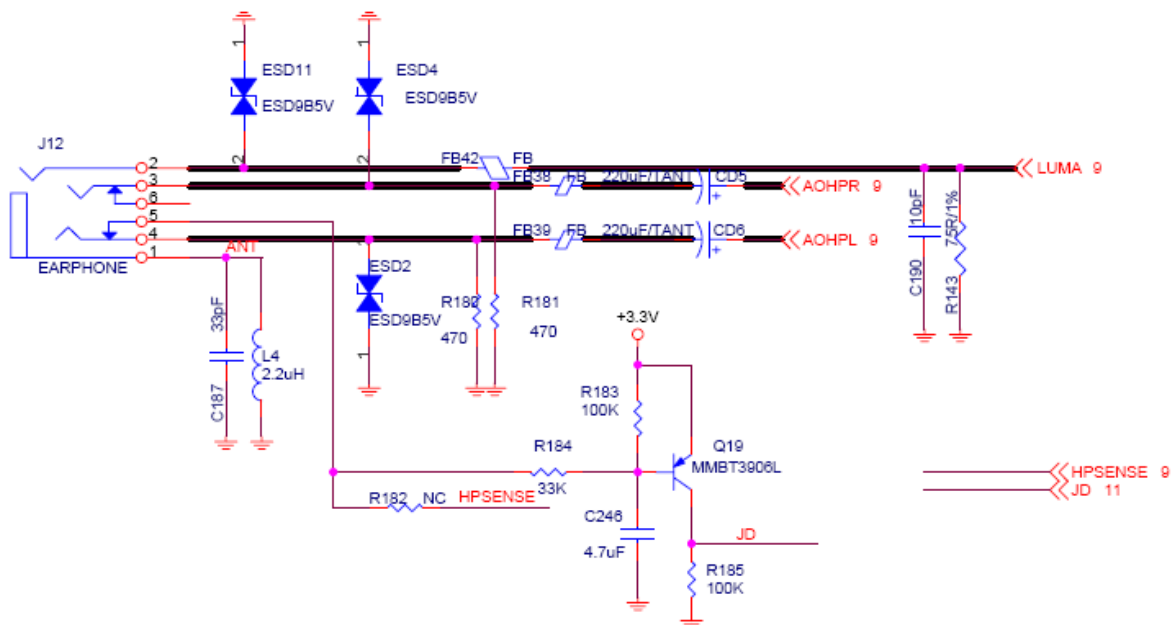


### 5.3 Headphone Out

The AOHPL and AOHPR pins should use two coupling capacitors to block the dc offset voltage. These capacitor can be large (from 33 $\mu$ F to 1000 $\mu$ F). They have the additional limiting of the low-frequency performance of the system. This effect is due to the high pass filter created by the coupling capacitor and the speaker impedance.

For a 220 $\mu$ F coupling capacitor and a 32Ohm speaker, frequencies below 23Hz are attenuated. The ESD2, ESD4 and ESD11 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. The device provides protection for contact discharges to greater than +/-15KV.

The ANT pin is used as an antenna of FM module.



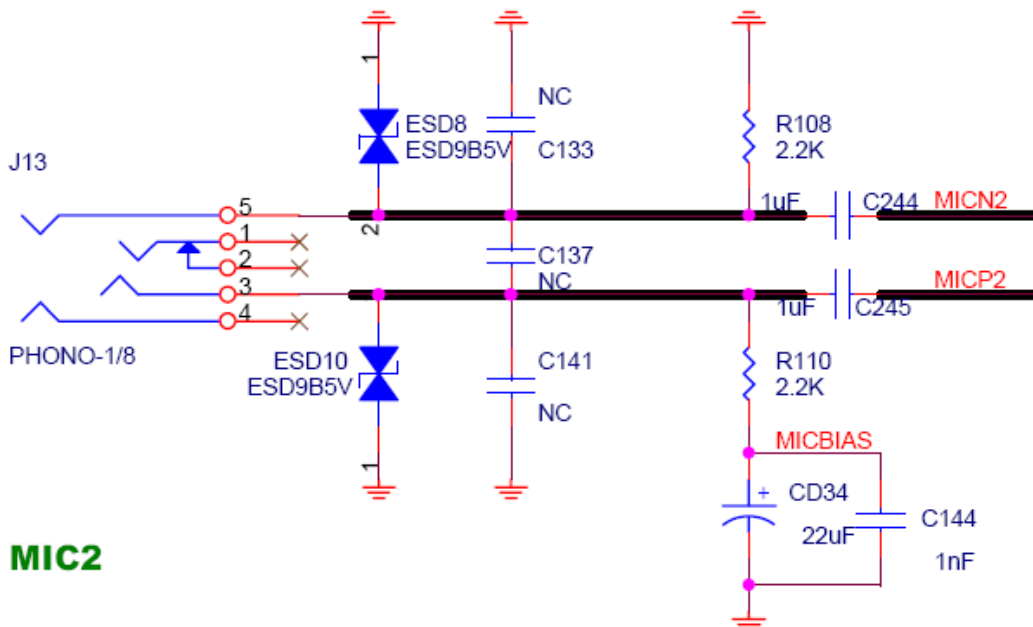
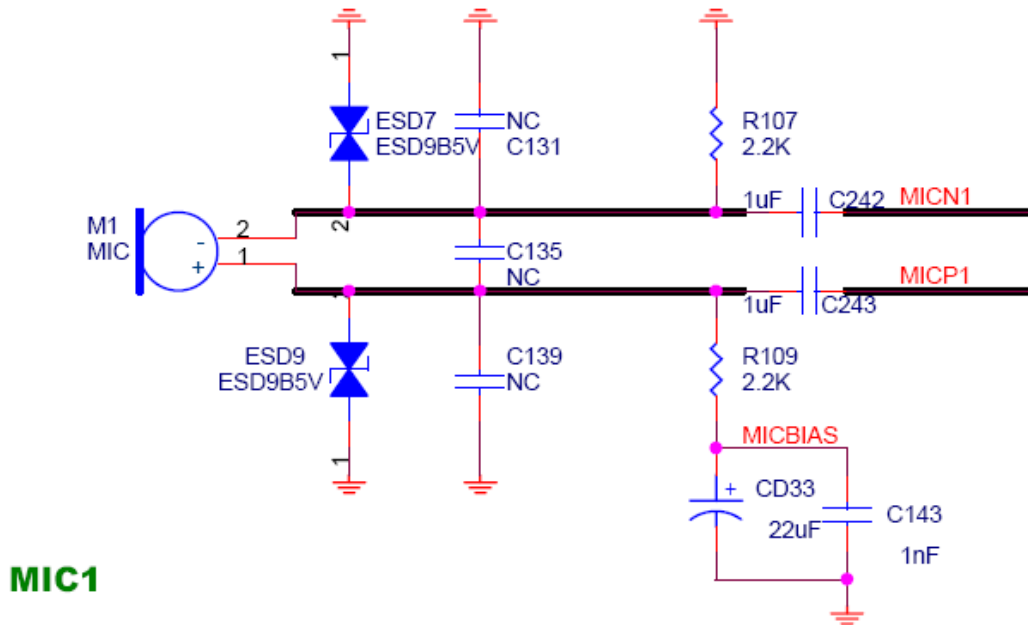
HPSENSE and JD are used to implement the insert test. When the jack is inserted, the value of HPSENSE or JD will be high. Otherwise, HPSENSE and JD will be low.



## 5.4 Mic In and Line In

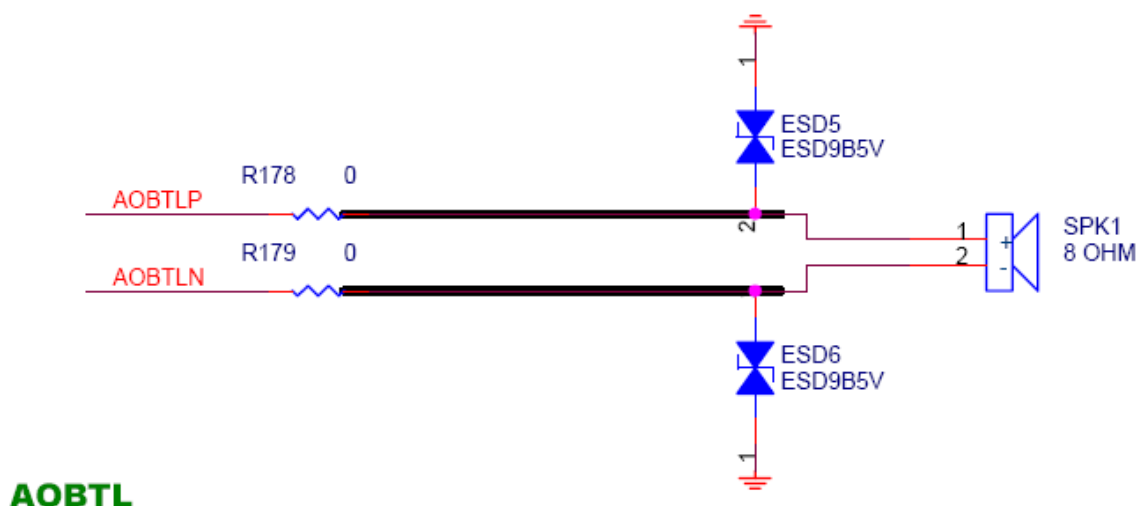
Specific value of resistor (R107, R108, R109, R110, commonly from 2.2kOhm to 4.7kOhm) and  $V_{MICBIAS}$  (usually from 1V to 2V or more) depends on the selected EC (Electret Condenser) microphone.

The 1nf decoupling capacitance removes high frequency noise of the chip.



## 5.5 Speaker

The ESD5 and ESD6 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. The device provides protection for contact discharges to greater than +/-15KV.



## 5.6 Layout Guideline

To ensure the maximum performance of the Audio, proper component placement and routing techniques are required. These techniques include properly isolating associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must not cross the ground split in the area

where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

## 6 Video Design Guidelines

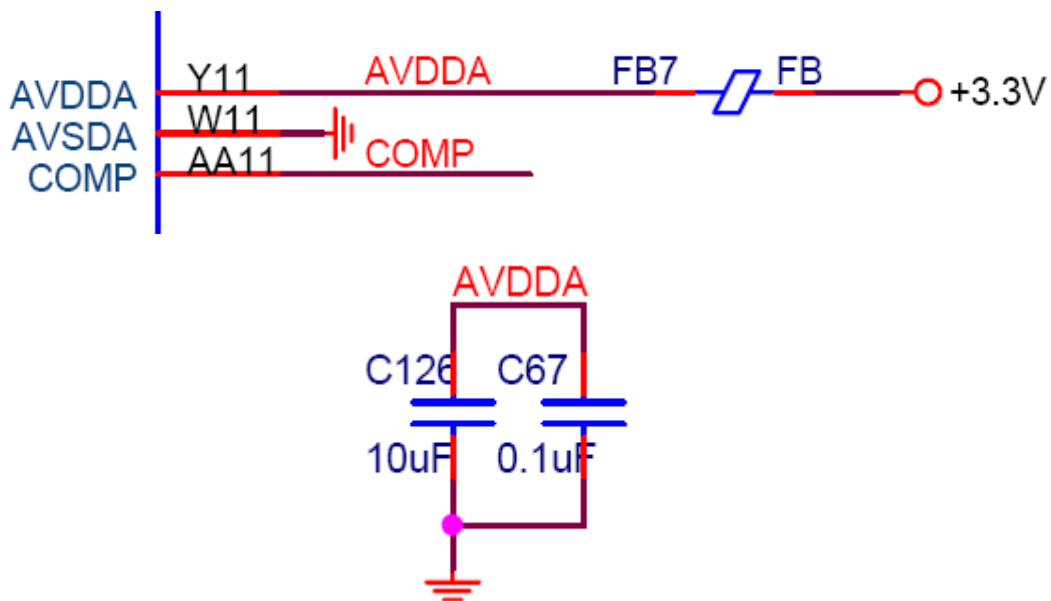
### 6.1 Overview

The TV Encoder enables the data for LCD panel showing in TV screen.

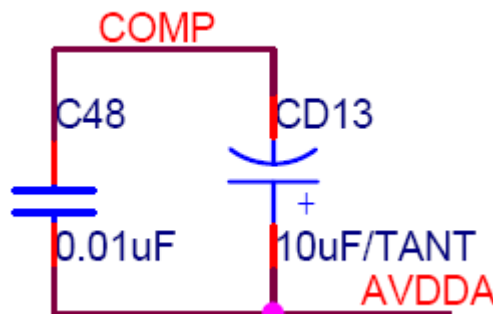
### 6.2 Video Power

AVDDA should be connected to a cleaned +3.3V power.

For a correct working, it is required to connect two decoupling capacitor (10 $\mu$ F and 100nF ceramic) between the pins AVDDA and AVSDA.

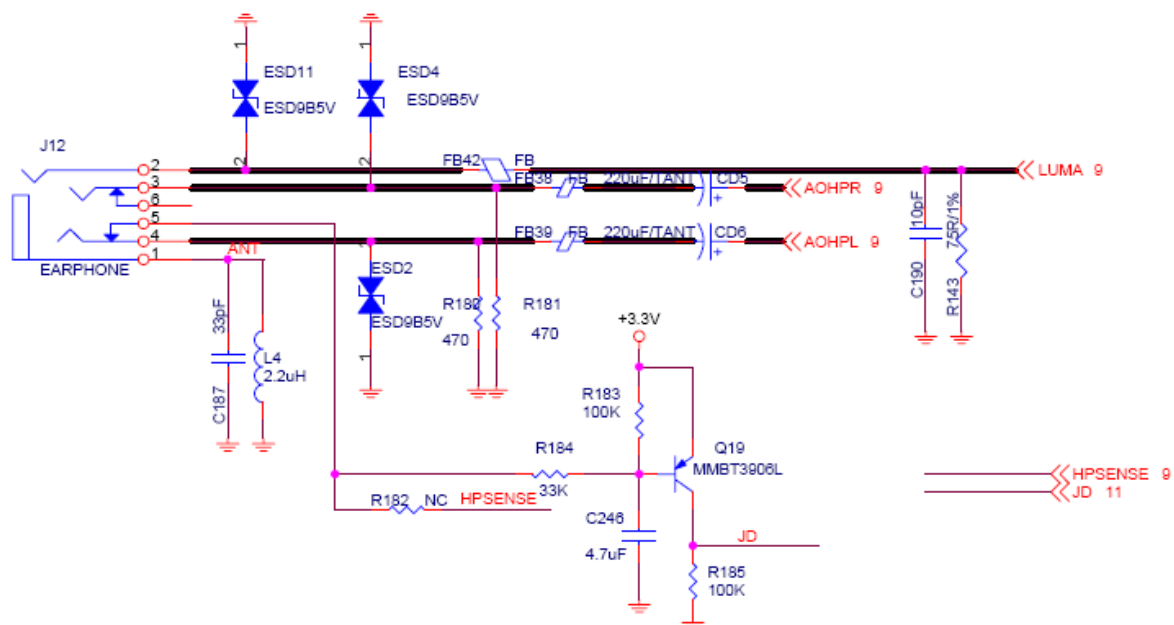


A tantalum capacitor more than 10 $\mu$ F and a 10nF ceramic capacitor should be attached from COMP to AVDDA externally.



### 6.3 TV Out

It is required a 75 Ohm 1% pull-down resistors for matching, a Ferrite Bead and a 10pF ceramic capacitor for filtering.



## 7 USB and OTG Design Guidelines

### 7.1 USB Overview

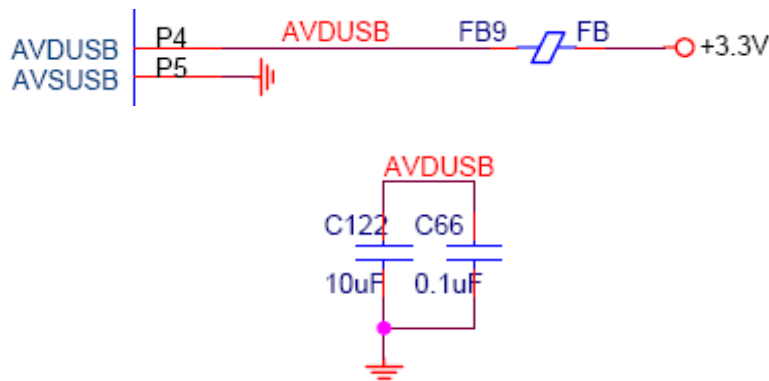
JZ4760 integrates USB Host Controller (UHC) which is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.

Familiarity with the Universal Serial Bus Specification, Revision 1.1 and the OHCI specification are necessary to fully understand the material.

It supports both low-speed and high-speed USB devices.

#### 7.1.1 USB Power

For a correct working, it is required to connect two decoupling capacitor (10 $\mu$ F and 100nF ceramic) between the pins AVDUSB and AVSUSB.



### 7.2 OTG Overview

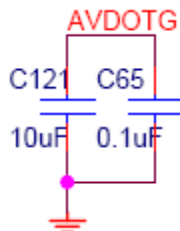
The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can play the role of both host and device.

JZ4760 also integrates and USB 2.0 OTG interface, which compliant with USB protocol Revision 2.0 OTG. It supports low-speed (1.5 Mbps), full-speed (12 Mbps) and high speed (480 Mbps). High speed and full speed supported for device role and high speed, full speed and low speed supported for host role.

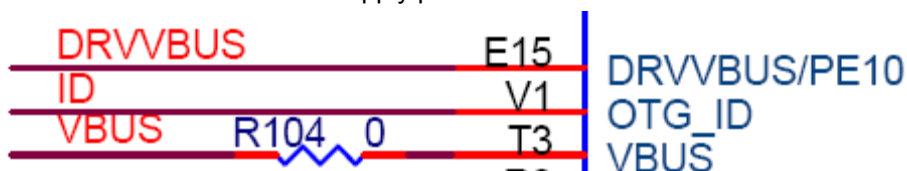
#### 7.2.1 OTG Power

The power of AVDOTG is support for the USB OTG analog power. It is required to connect two decoupling capacitor (10 $\mu$ F and 100nF ceramic) between the pins AVDOTG and AVSOTG.





And we should have a pin of VBUS supply power OTG, it have to connect to an external charge. The DRVVBUS is used to control whether to supply power for OTG.



To enable the OTG, the circuit should monitor the VBUS pin and can supply voltage for this pin and we also need ID pin. Figure 7-1 shows the classic design for OTG function.

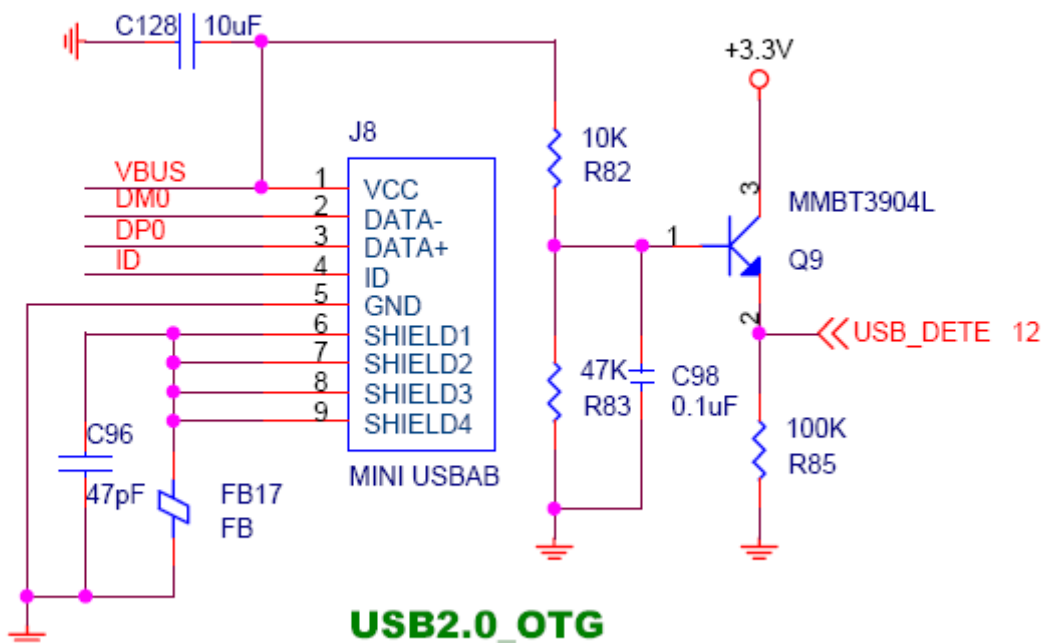
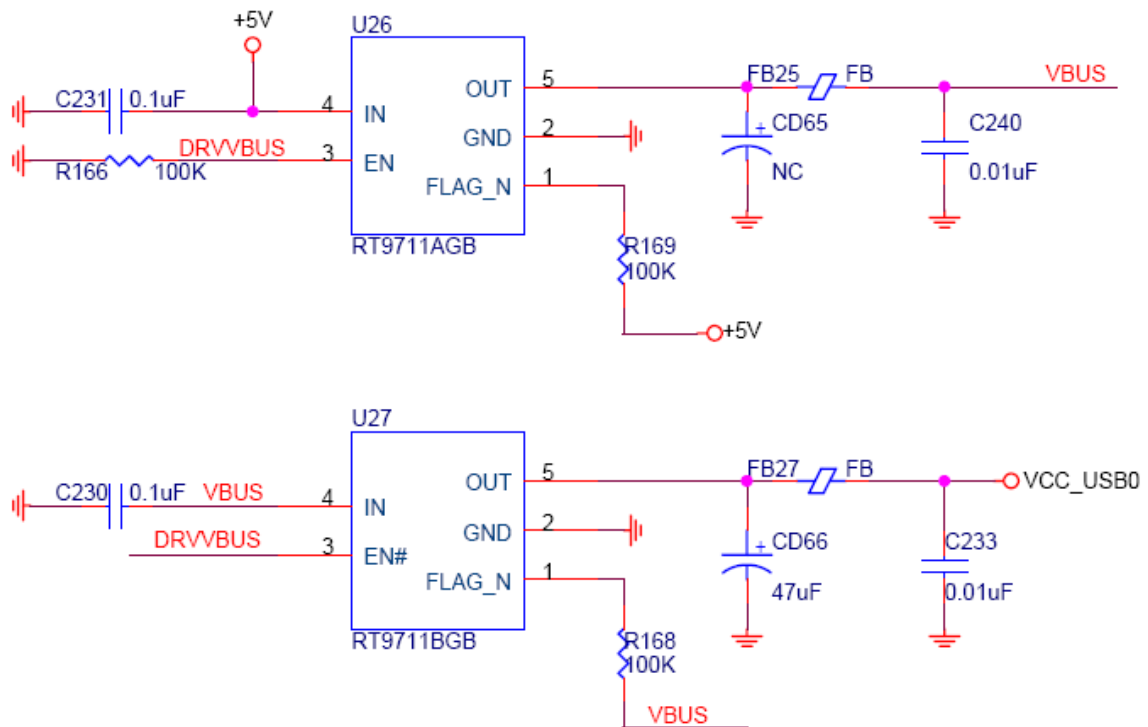


Figure 7-1 Classic Design for USB 2.0 OTG

To achieve this function, we should have circuit to control whether supply voltage for VBUS or not. So we need a power switch circuit to achieve this target. Figure 7-2 shows the power switch circuit, and DRVVBUS controlled by the processor. Via the state of USB\_DETE and ID pins, the processor can complete this task.



## USB Power Switch

Figure 7-2 USB Power Switch for USB 2.0 OTG

### 7.3 The following are general guidelines for the USB and OTG interface:

- Unused USB ports should be terminated with 15 k $\Omega$  pull-down resistors on both DP1/DM1 data lines.
- 15  $\Omega$  series resistors should be placed as close as possible to the JZ4760. These series resistors provide source termination of the reflected signal.
- 47-pF caps must be placed as close as possible to the JZ4760 as well as on the processor side of the series resistors on the USB data lines (DP1, DM1). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 k $\Omega$   $\pm$  5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (DP1, DM1). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the DP and DM signals should be 45  $\Omega$  (to ground) for each USB signal DP or DM. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 7-3 7-4. The impedance is 90  $\Omega$  between the differential signal pairs DP and DM, to match the 90  $\Omega$  USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90  $\Omega$  is the series impedance of both wires, which results in an individual wire presenting 45  $\Omega$  impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals'. (i.e., hand-routing preferred). The



DP/DM signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the DP/DM signal pair to adjacent signal traces will help to prevent cross-talk. The DP/DM signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

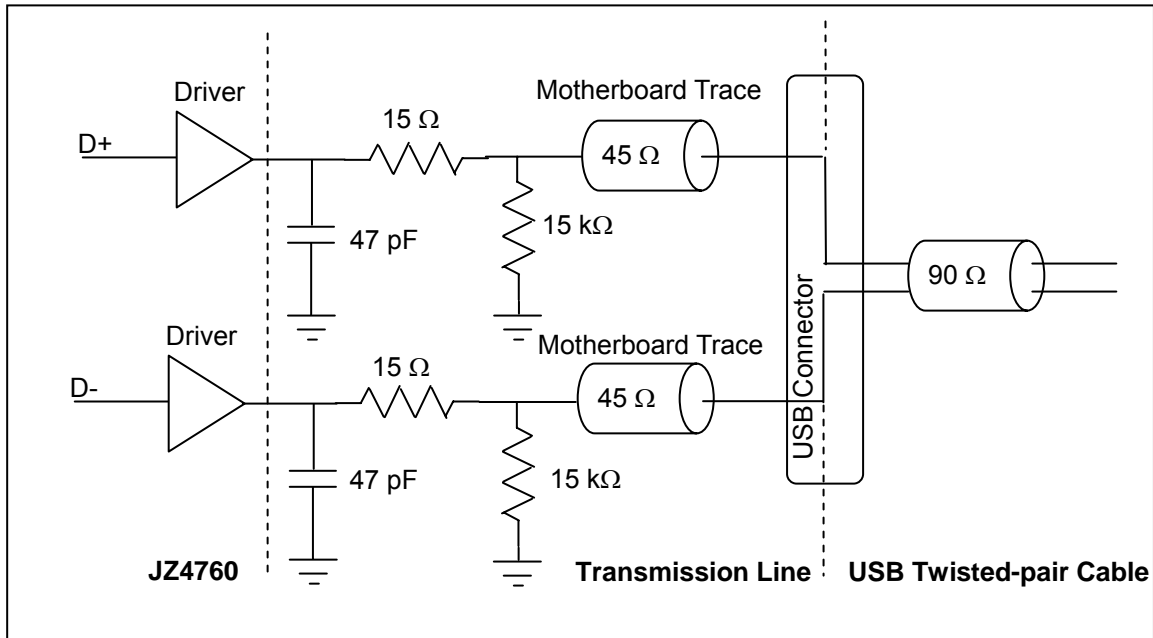


Figure 7-3 Recommend USB Host Schematic

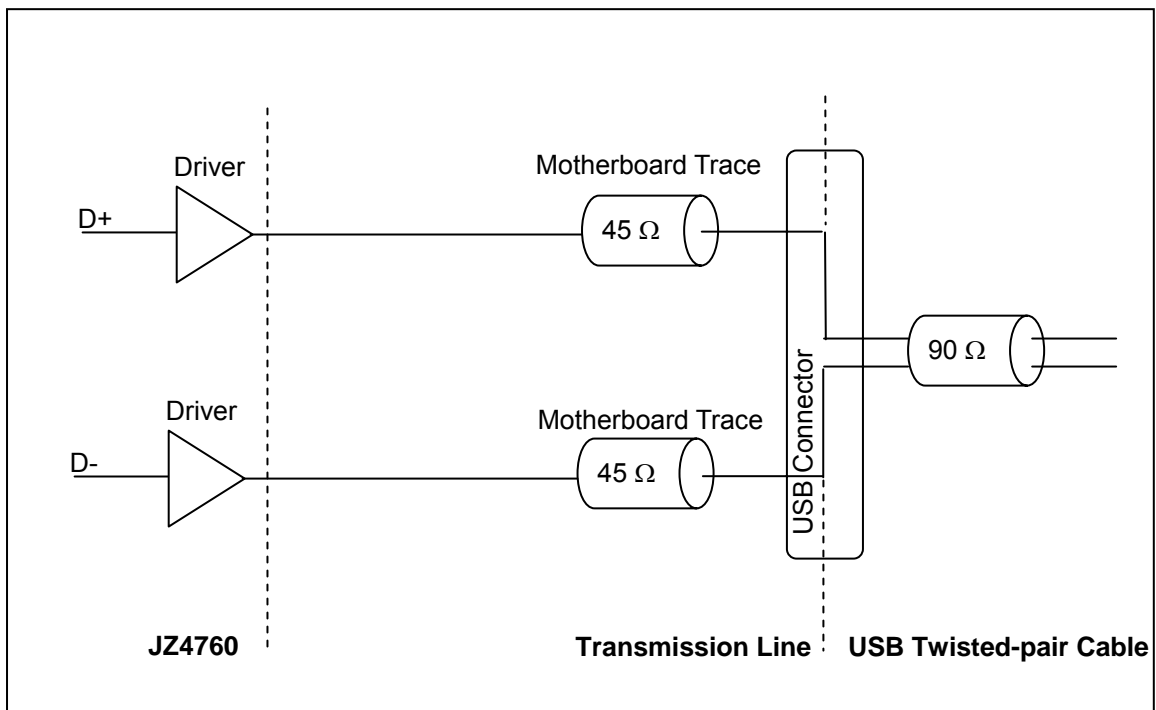


Figure 7-4 Recommend USB Device Schematic

## 8 LCD

The JZ4760 integrated LCD controller, which has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller. Temporal dithering (frame rate modulation) is supported for STN LCD panels.

NOTE: The LCD controller can provide high driven strength, so you should use resistance of 33 ohm connect to the signal, and the resistance of clock needed maybe not the same together with the different screen.

**Table 8-1 TFT Pin Mapping**

JZ4760 Pin	8-bit Serial RGB	18-bit Parallel RGB	24-bit Parallel RGB	Smart LCD Serial	Smart LCD Parallel
LCD_PCLK/SLCD_CLK	CLK	CLK	CLK		CLK
LCD_HSYNC/SLCD_RS	HSYNC	HSYNC	HSYNC	RS	RS
LCD_VSYNC/SLCD_CS	VSYNC	VSYNC	VSYNC	CS	CS
LCD_R7		R5	R7		D17
LCD_R6		R4	R6		D16
LCD_R5		R3	R5	D15	D15
LCD_R4		R2	R4	D14	D14
LCD_R3		R1	R3	D13	D13
LCD_R2		R0	R2	D12	D12
LCD_G7		G5	G7	D11	D11
LCD_G6		G4	G6	D10	D10
LCD_G5		G3	G5	D9	D9
LCD_G4		G2	G4	D8	D8
LCD_G3	R7/G7/B7	G1	G3	D7	D7
LCD_G2	R6/G6/B6	G0	G2	D6	D6
LCD_B7	R5/G5/B5	B5	B7	D5	D5
LCD_B6	R4/G4/B4	B4	B6	D4	D4
LCD_B5	R3/G3/B3	B3	B5	D3	D3
LCD_B4	R2/G2/B2	B2	B4	D2	D2
LCD_B3	R1/G1/B1	B1	B3	D1	D1
LCD_B2	R0/G0/B0	B0	B2	D0	D0
LCD_DE	DE	DE	DE		
LCD_R1			R1		

---

LCD_CLS/LCD_R0			R0		
LCD_G1			G1		
LCD_SPL/LCD_G0			G0		
LCD_PS/LCD_B1			B1		
LCD_REV/LCD_B0			B0		

## 9 Camera

The CIM (Camera Interface Module) of JZ4760 connects to a CMOS or CCD type image sensor. The CIM source the digital image stream through a common 8-bit parallel common digital protocol. The CIM can directly connect to external CMOS image sensors and ITU656 standard video decoders.

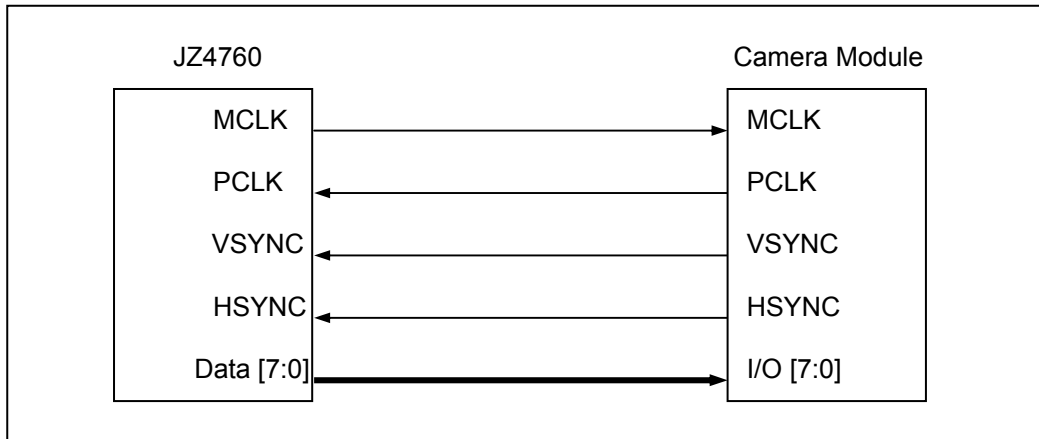


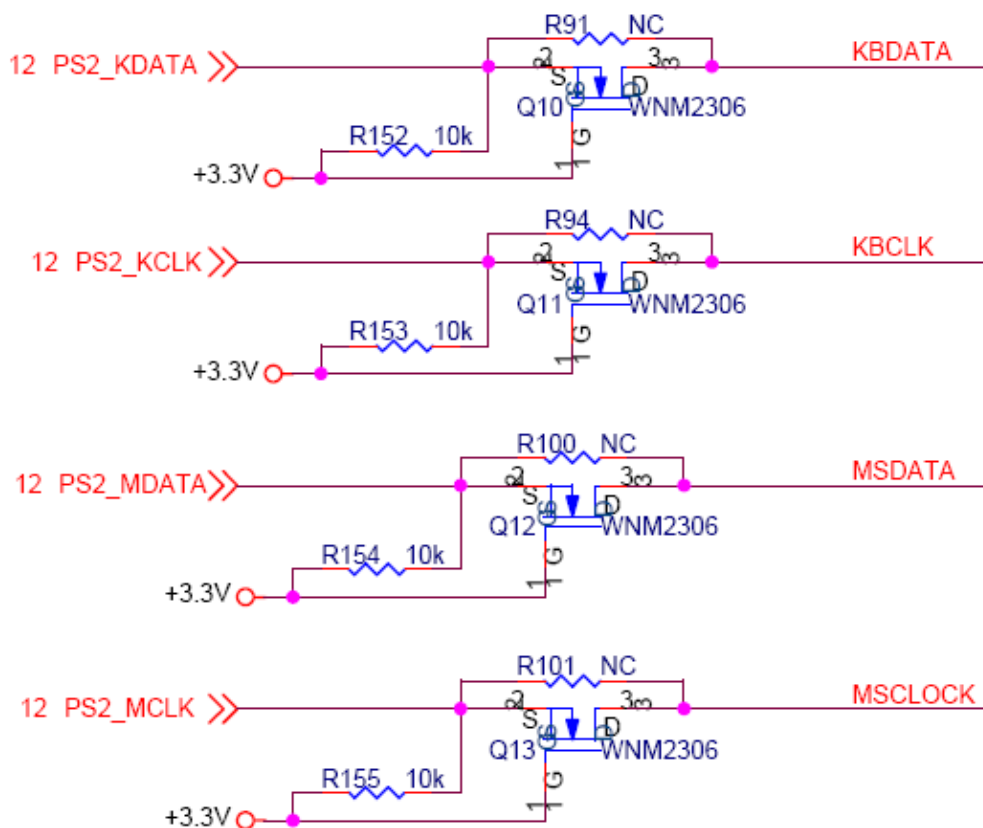
Figure 9-1 Example of Camera Module Interconnection

# 10 PS/2 and Keyboard

## 10.1 Overview

The JZ4760 processor integrate PS/2 keyboard controller (KBC) to provide the functions to a keyboard or to a PS/2 mouse. KBC receives serial data from the keyboard or mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The KBC is compatible with 8042.

The following figure is a typical design.



## PS/2 KEYBOARD AND MOUSE PORT

# 11 SAR A/D Controller

## 11.1 Overview

The A/D in JZ4760 is COMS low-power dissipation 10bit SAR analog to digital converter. It operates with +3.3/+1.2V power supply.

The SAR A/D Controller of JZ4760 can work at three different modes: Touch Screen (measure pen position and pen down pressure), Battery (check the battery power), and SADCIN (external ADC input).

NOTE: AUX0 is a high speed sampling pin, it can be used for AD sampling, but used for analog button is not recommended.

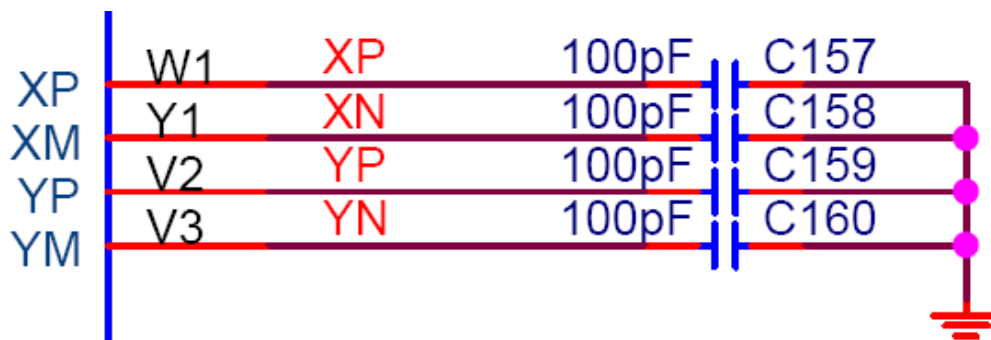
**Table 11-1 SAR ADC Pins Description**

NAME	I/O	Description
XN	AI	Touch screen analog differential X- position input
YN	AI	Touch screen analog differential Y- position input
XP	AI	Touch screen analog differential X+ position input
YP	AI	Touch screen analog differential Y+ position input
VBAT_IR	AI	Analog input for VBAT measurement (0~5V)
AUX0	AI	Auxiliary Input
AUX1	AI	Auxiliary Input
VBAT_ER/AUX2	AI	VBAT direct input * / Auxiliary Input

## 11.2 Touch Screen

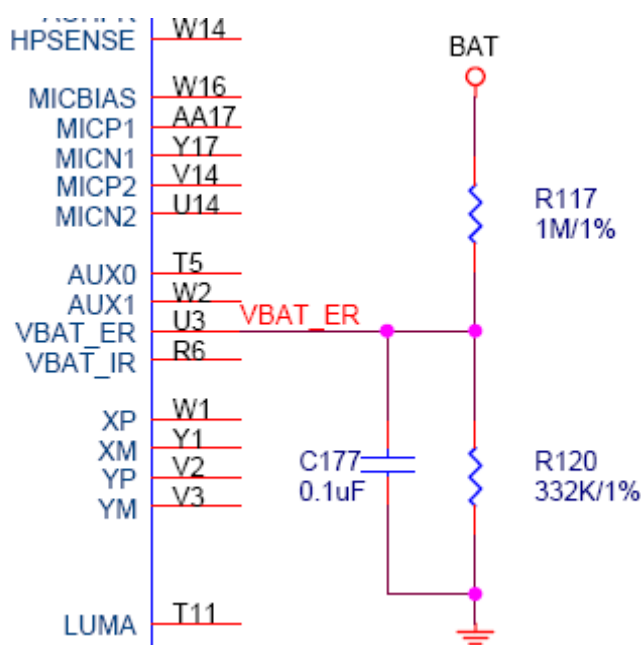
The JZ4760 can support 4-wire resistive touch screen.

There is needed a decouple capacitor for every channel to avoid the crosstalk from LCD. The value is decided by the touch screen and can be from 100pF to 1000pF.



### 11.3 Battery Voltage Measurement

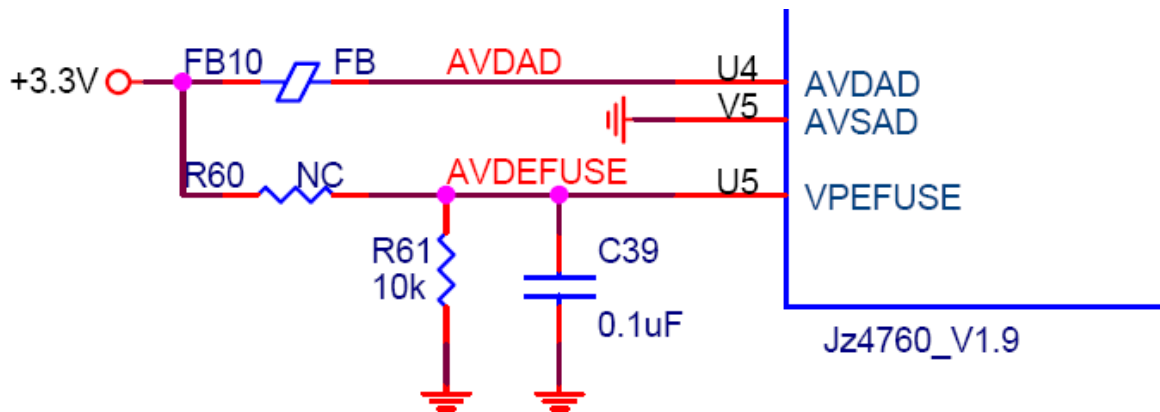
Users who already deployed divider resistors on board level can use VBAT\_ER/AUX2 to directly measure the battery value. Also, the chip provides a built-in 1/4 divider for VBAT measurement on the VBAT\_IR pin. The following figure is the approach we recommend. Use the recommended resistance, and you can control the power consumption easier.



## 12 OTP EFUSE

### 12.1 Overview

Total 256 bits of EFUSE are provided, separated into lower 128bits segment and higher 128bits segment. Each segment can be programmed separately or together. Each segment has a protect bit. Generally, the pin of VPEFUSE should be pull down to ground.





# 13 Ethernet Design Guidelines

## 13.1 Overview

The JZ4760 processor doesn't contain Ethernet media access controller (MAC). So we need an Ethernet controller that is external to the processor. This section describes design guidelines for the LAN on board based JZ4760.

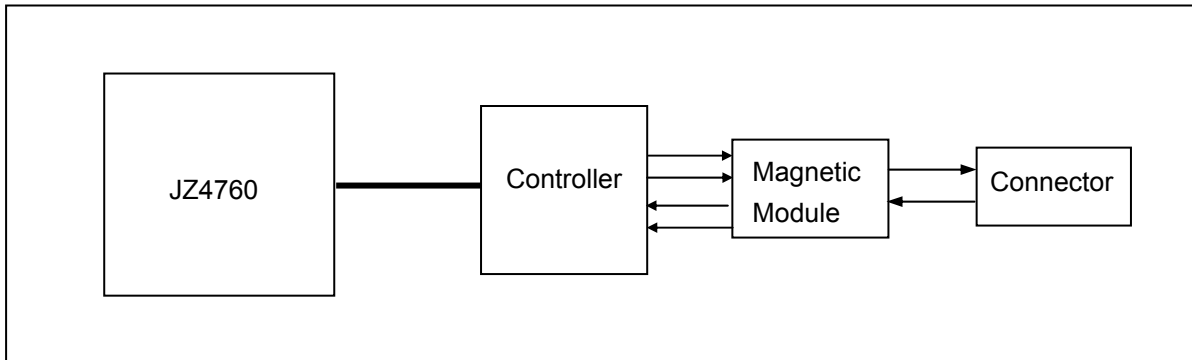


Figure 12-1 LAN On Board Implementation

## 13.2 JZ4760 Ethernet Controller Connection

JZ4760 Ethernet controller interconnection example is shown as figure 12-2, the Ethernet Controller chip maybe varied for specific OEM design targets. JZ4760 RESETOUT\_ drive the RESET# input to reset the CONTROLLER chip when power-up.

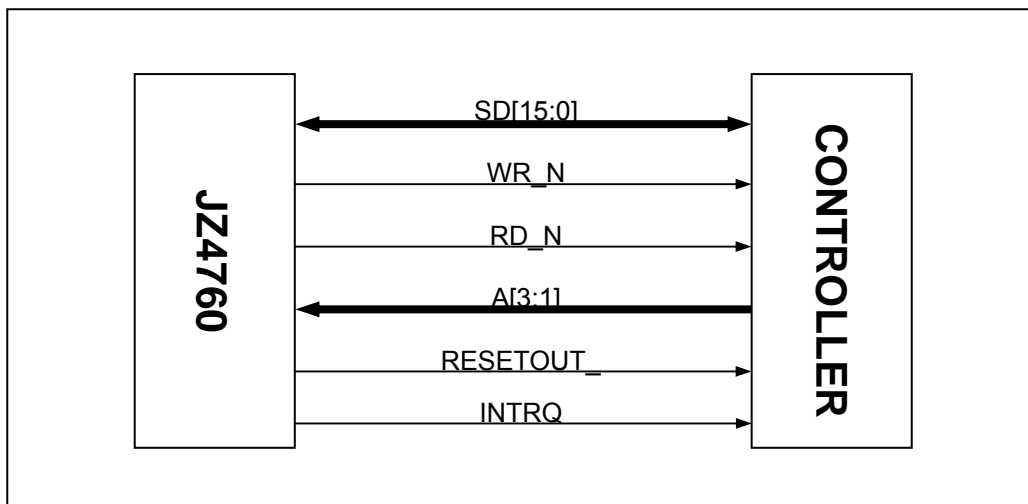


Figure 12-2 Controller Connection

# 14 RTC

## 14.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, a power-on-reset generator, the real time and alarm logic, and the power down and wakeup control logic.

The external WAKEUP\_N pin is with up to 2s glitch filter / alarm wakeup.

## 14.2 RTC Clock

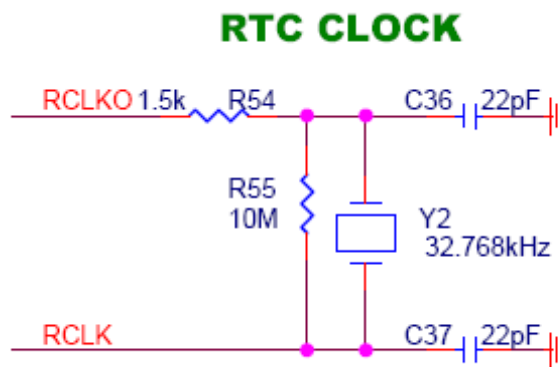


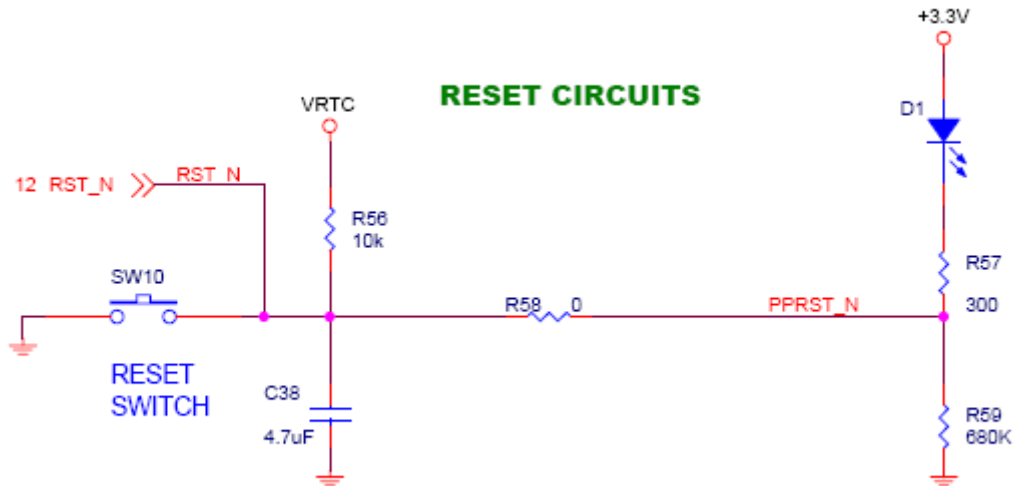
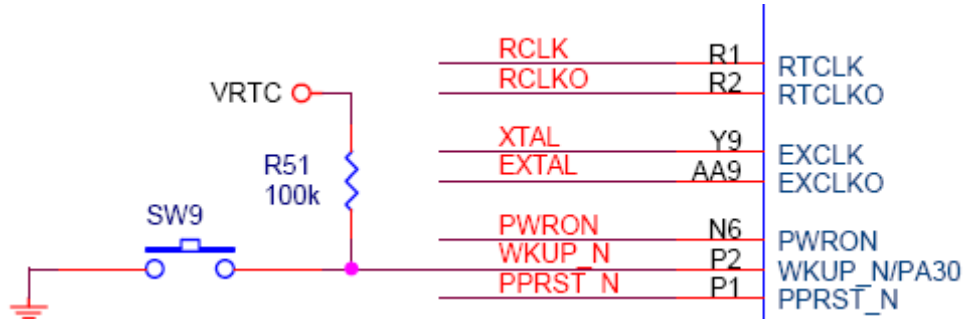
Table 13-1 RTC Clock Routing Summary

Trace Impedance	Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R55, C36, and C37 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R55 = 10M ± 5% C36=C37=33pF±10 % The value of C1, C2 and R1 should be referred to the crystal's specification	Ground

## 14.3 Power Control

The following is the recommended circuit for the system power control.

PWRON is an active high signal from CPU. If the power circuit enable signal is active high signal, you can use the PWRON directly. The resistance of R59 in the next figure is recommended to be 680K ohm, in this case ,you can consume less current when power down mode.



# 15 Miscellaneous Peripheral Design Guidelines

## 15.1 SSI Design Guideline

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The following figures show the connection example:

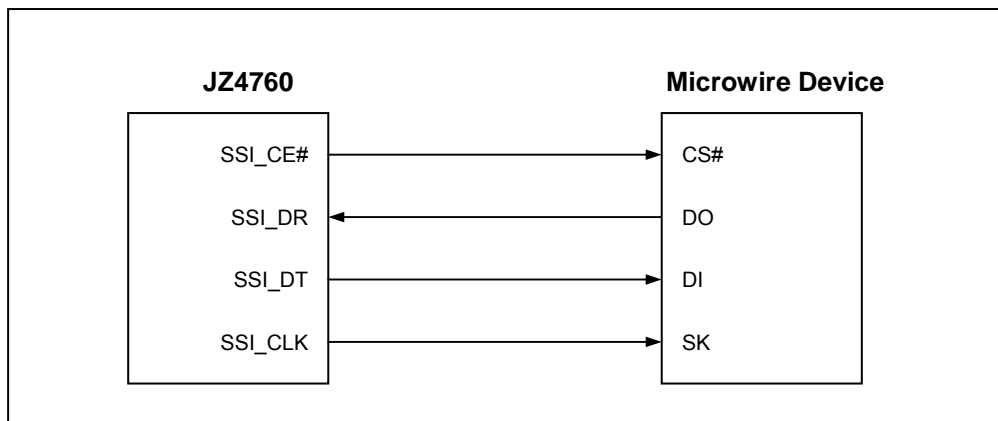


Figure 14-1 Microwire Interconnection

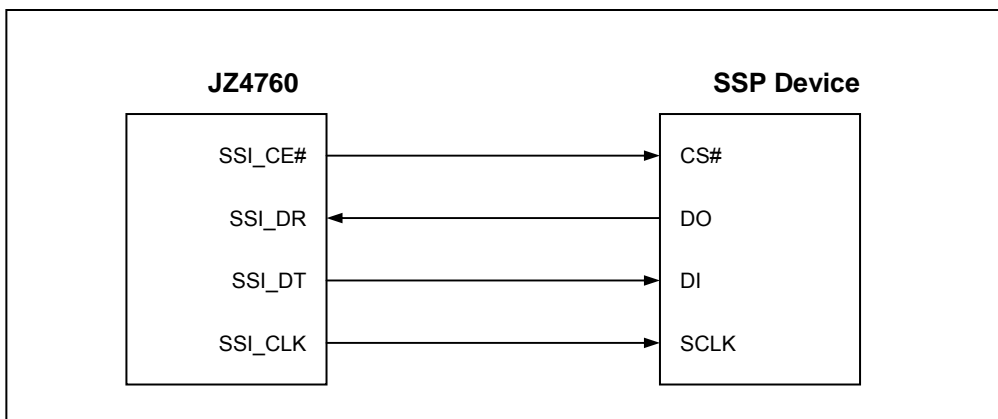


Figure 14-2 SSP Interconnection

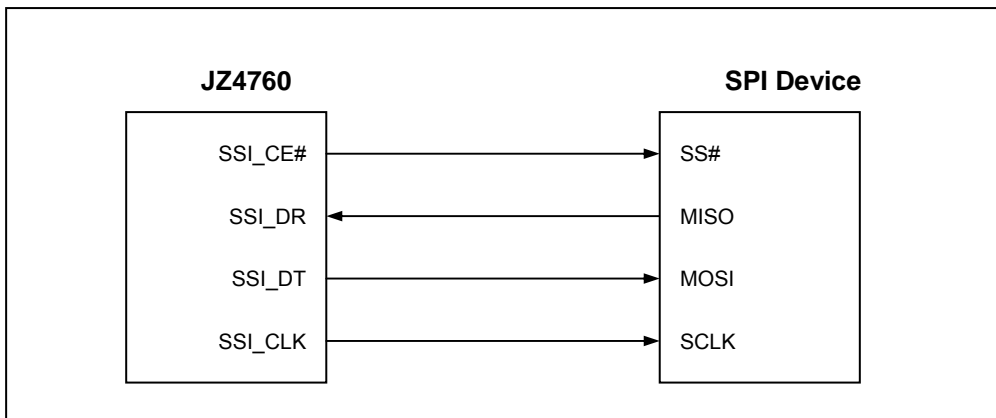


Figure 14-3 SPI Interconnection

## 15.2 UART/IrDA

The JZ4760 processor has four UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550 industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

### 15.2.1 UART Implementation

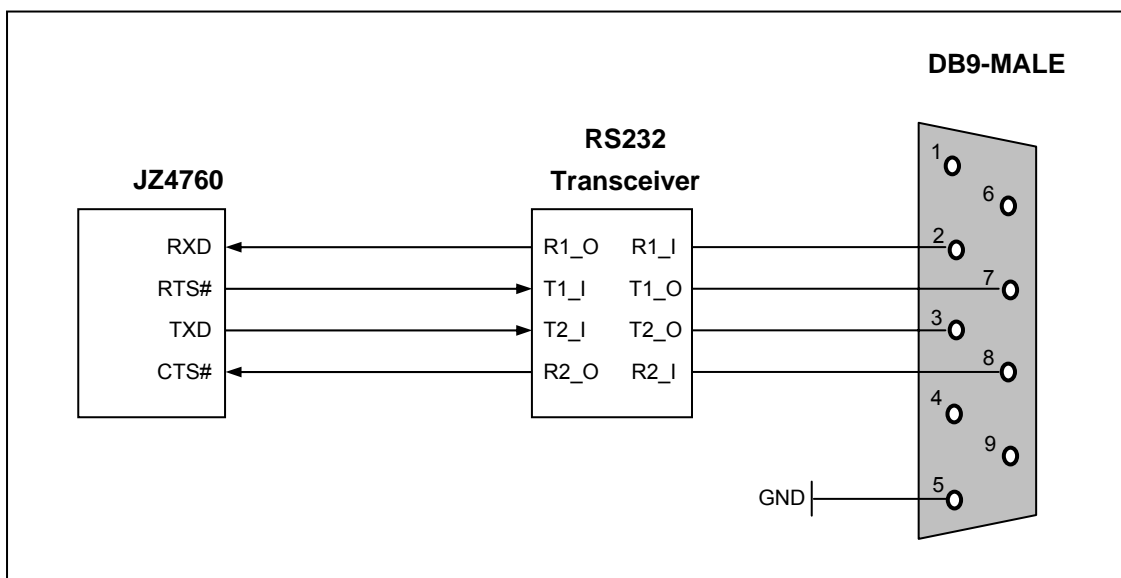


Figure 14-4 RS232 Serial Port Interconnection

### 15.2.2 IrDA Implementation

The Slow Infrared (SIR) interface is used with the UART to support two-way wireless communication that uses infrared transmission. The SIR provides a transmit encoder and receive decoder to support a physical link that conforms to the IrDA Serial Infrared Specification Version 1.1.

The SIR interface does not contain the actual IR LED driver or the receiver amplifier. The I/O pins

attached to the SIR only have digital CMOS level signals. The SIR supports two-way communication, but full duplex communication is not possible because reflections from the transmit LED enter the receiver. The SIR interface supports frequencies up to 115.2 kbps.

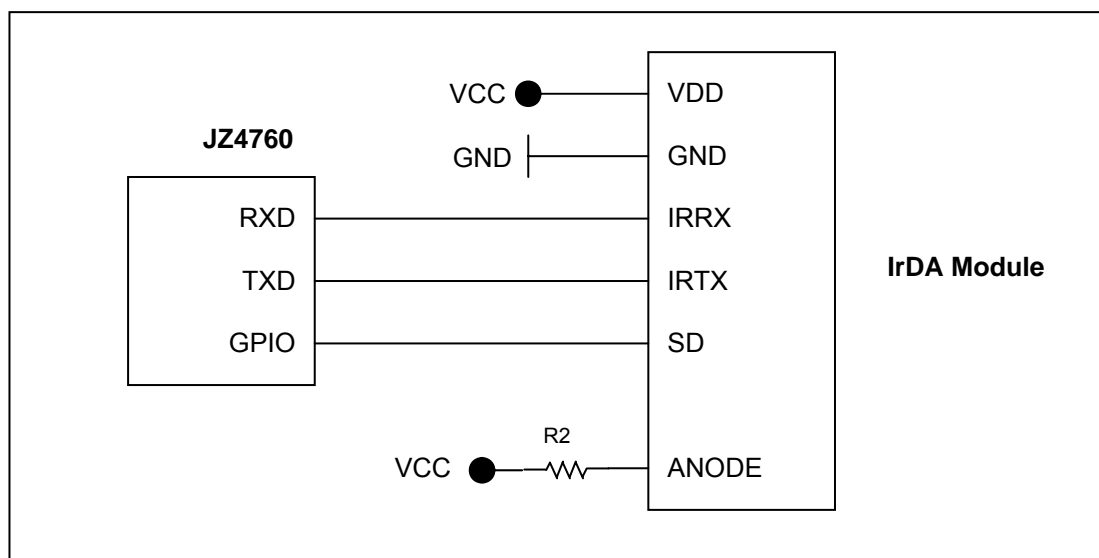


Figure 14-5 IrDA Port Interconnection

### 15.3 I2C Bus

The I2C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I2C bus. The I2C bus requires a minimum amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

The I2C module supports I<sup>2</sup>C standard-mode and fast-mode up to 400 kHz. The interface example is shown as following figure. The I2C bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up (R1, R2=2.2K) is required on SCL and SDA. Refer to The I2C-Bus Specification for complete details on I2C bus operation.

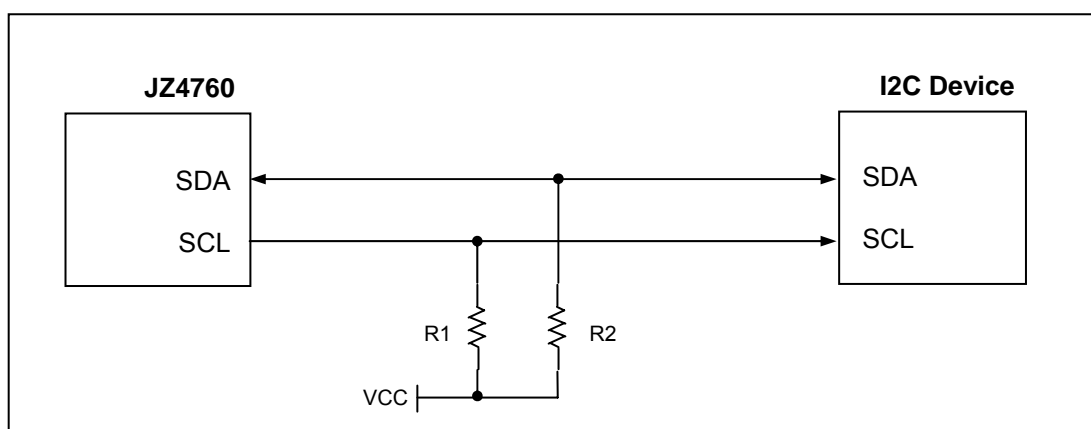


Figure 14-6 I2C Interconnection

### 15.4 PWM

The Pulse Width Modulator (PWM) is used to control the back light inverter or adjust bright or

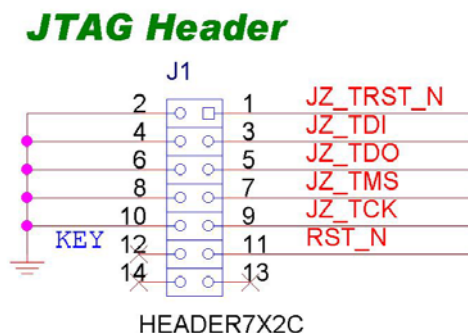
contrast of LCD panel and also can be used to generate tone. PWM consists of a simple free-running counter with two compared registers, each compare register performs a particular task when it matches the count value. The period comparator causes the output pin to be set and the free-running counter to reset when it matches the period value. The width comparator causes the output pin to reset when the counter value matches. JZ4760 contains eight pulse width modulators: PWM0 ~ PWM7.

## 15.5 GPIO

The JZ4760 processor provides 166 multiplexed General Purpose I/O Ports (GPIO) for use in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

## 15.6 JTAG/Debug Port

JZ4760 has a built-in JTAG/Debug port. All JTAG pins are directly connected. The following figure shows the connection of the JTAG port. Pin 11 RST\_N should be connected to system reset circuit. Pin 12 is a KEY. The header should be a 7X2(2.54mm Pitch) male header with coat.



## 16 Platform Clock Guidelines

The JZ4760 processor contains one PLL driven by the 12-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- DDR2 bus clock
- Programmable clocks needed by certain peripherals

The following is the recommended circuit for main clock. When layout the board, you should keep the distance between Y1 and JZ4760 as short as possible.

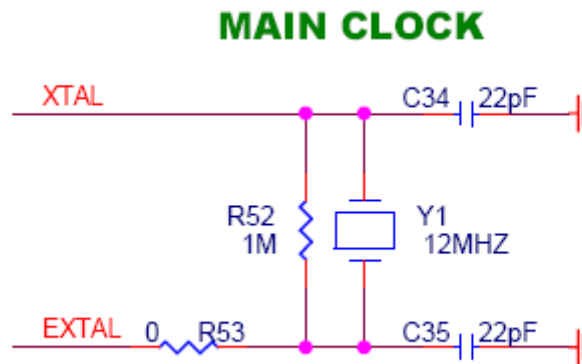


Table 15-1 Main Clock Routing Summary

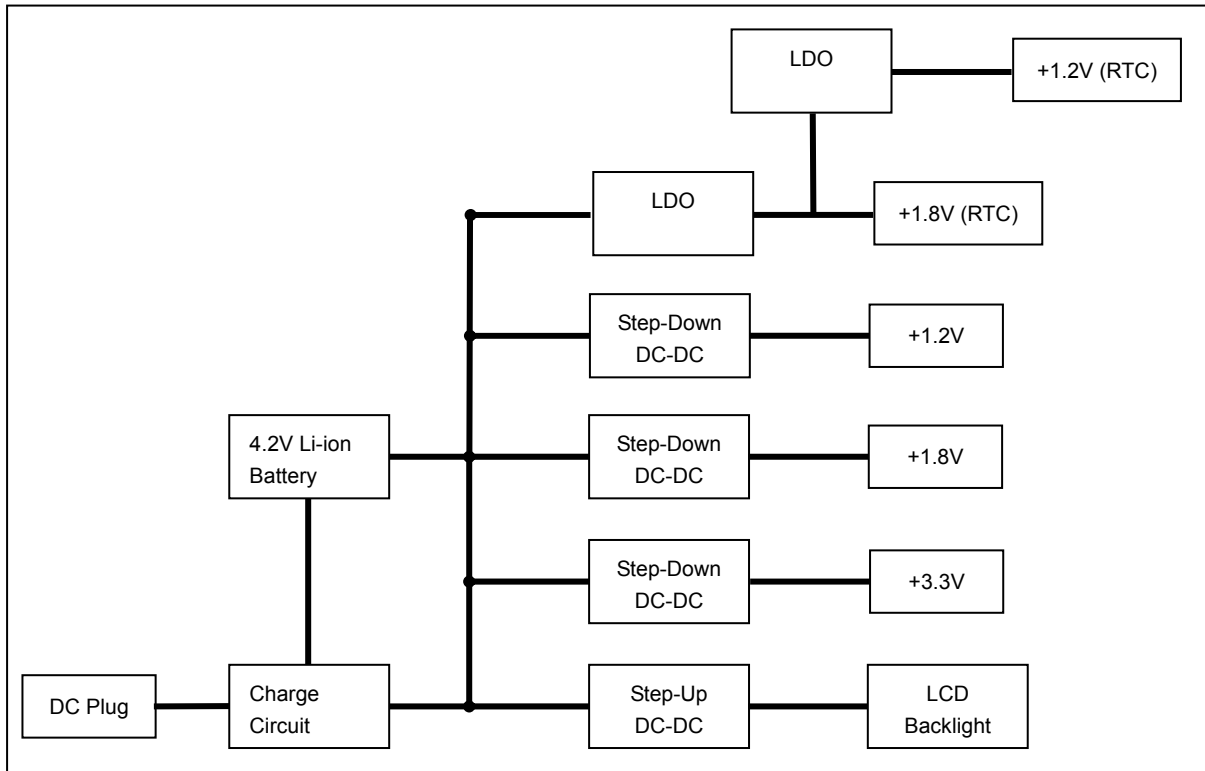
Trace Impedance	Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R52, C34, and C35 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R52 = 1M ± 5% C34=C35=22pF±10 % (Typical) The value of C34, C35 and R52 should be referred to the crystal's specification	Ground



# 17 Platform Power Guidelines

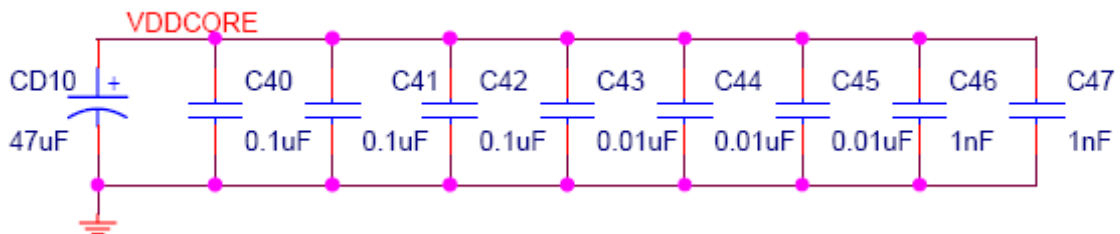
## 17.1 Overview

The JZ4760 processor needs three voltages: +3.3V, +1.8V for I/O and +1.2V for core. The following figure is a typical power circuit in the PMP application.

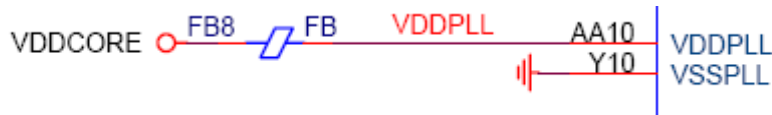


## 17.2 Power Delivery and Decoupling

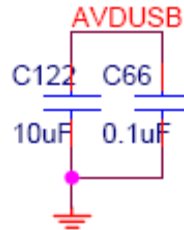
The VDDIO (+3.3V, +1.8V) and VDDCORE (+1.2V) of JZ4760 should be decoupled with 100nF, 10nF and 1nF capacitor.



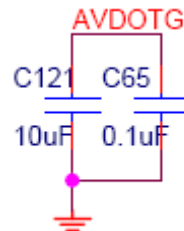
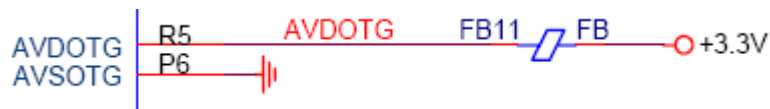
The Power of PLL should be as the following circuit.



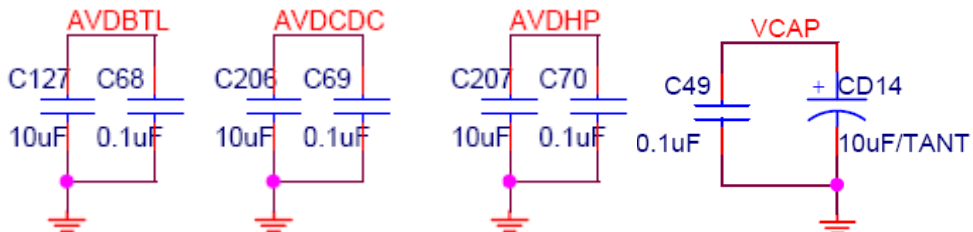
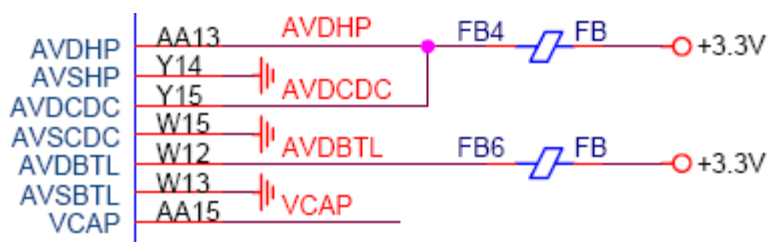
The power of USB should be as the following circuit.



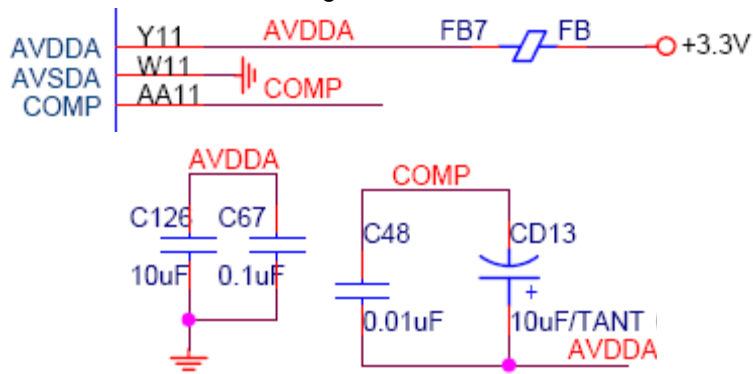
The power of OTG should be as the following circuit.



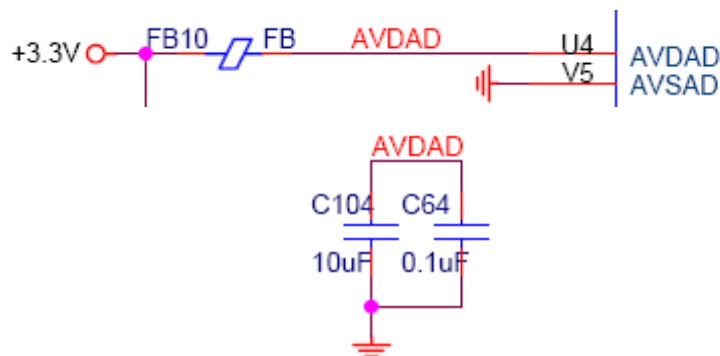
The power of Audio should be as the following circuit.



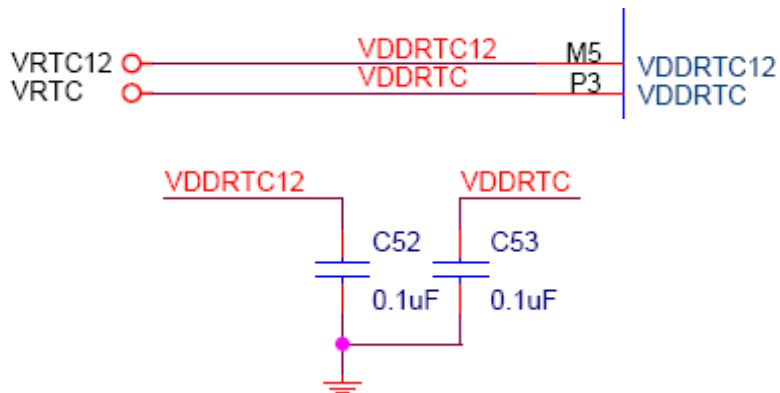
The power of DAC should be as the following circuit.



The power of ADC should be as the following circuit.



The power of RTC should be as the following circuit.



The capacitors should be placed near the Pin of power. The traces from capacitor to the Pin should be short and width.