Jz4730

32 Bits Microprocessor

Application Notes 002: the used of I2S

I2S Controller

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Jz4730 32 Bits Microprocessor

Application Notes 002

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Release history

Date	Revision	Change
Jan. 2007	0.1	Before release
Feb. 2007	0.2	Add information for 3.6864MHz and 4MHz EXCLK

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The use of Jz4730 I2S Controller

1. Overview

This document provides hardware/software guidelines and recommendations of utilization the I2S controller (AIC) in Jz4730 microprocessor to control an external I2S CODEC in audio applications.

In this document, 3 different hardware configurations are discussed. Which one is best depends on the features of the chosen I2S CODEC and hardware platform environment.

(1) If the chosen I2S CODEC contains a PLL and its input clock exists in the hardware platform, configuration described in “2” is recommended
(2) If the chosen I2S CODEC contains a PLL and its input clock does not exists in the hardware platform, configuration described in “0” is recommended
(3) If both above two configurations cannot be used, configuration described in “4” is recommended

The frequently change PLL frequency in Jz4730, especially during normal operation, is not recommended. PLL is usually fixed to the chip maximum frequency. The configuration (1) and (2) relieve the dependence of Jz4730 PLL frequency to audio sample rate. Which gives more freedom to choose the Jz4730 maximum frequency.

2. CODEC in master mode with input clock from other place

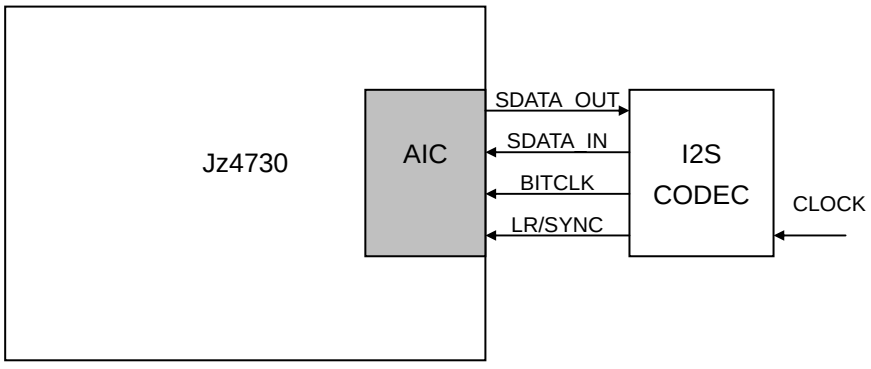

Figure 1 CODEC in master mode with input clock from other place

The I2S CODEC input clock is a fixed frequency clock.

3. CODEC in master mode with input clock from Jz4730

The implementation of this configuration needs an unused SCC in Jz4730. Jz4730 has 2 SCCs, SCC0 and SCC1. The unused SCC clock output is used to output the EXCLK to CODEC. Suppose the CODEC accept 12MHz clock as input. Figure 2 shows the hardware configure, where SCC1_CLK = EXCLK = 12MHz.

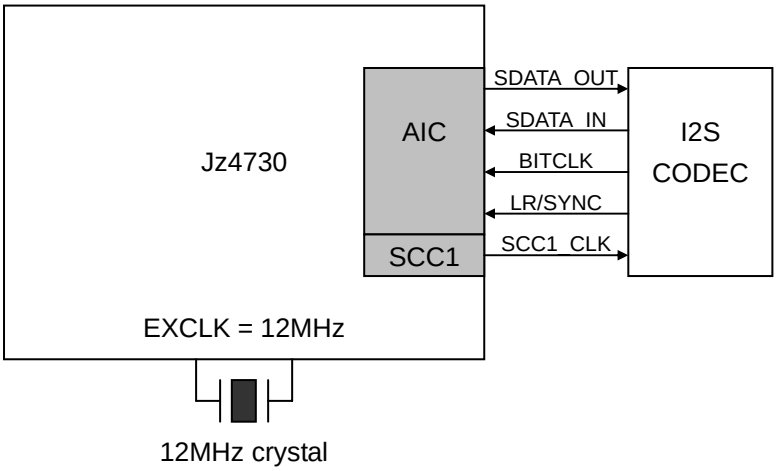

Figure 2 CODEC in master mode with input clock from Jz4730 SCC1

Please follow the following steps to used SCC1 clock output

(1) Initial GPIO sharing: set GP67 to function 01 and keep GP65 (SCC1 data pin) as GPIO in the same time.
(2) Keep SCCTFR1 to its reset value 0x173 (no operation)
(3) Initial flush SCC1 FIFO by write 0x00800000 to SCCCR1
(4) To enable SCC1 clock output, write 0x80000000 to SCCCR1
(5) To disable SCC1 clock output, write 0x00000000 to SCCCR1

4. CODEC in slave mode

In this case Jz4730 PLL frequency or the chip maximum clock is related to audio sample rate. Figure 3 shows the hardware configure, where EXCLK can be other frequencies, here we take 12MHz as an example. Let's consider two cases.

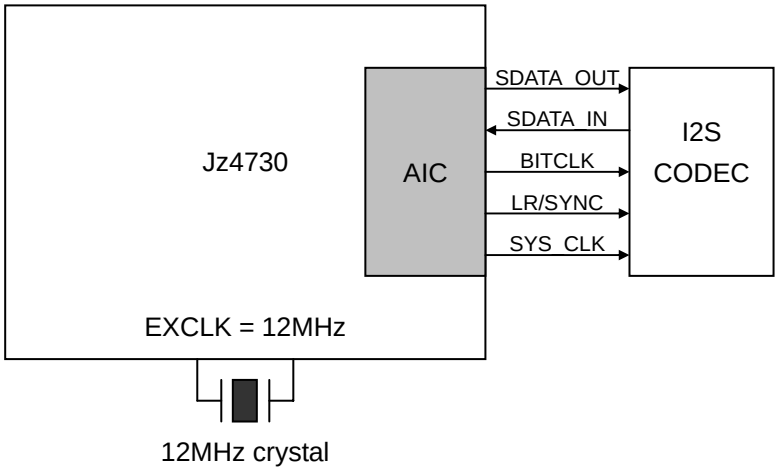

Figure 3 Hardware connection of the master mode configure

Case 1: 48MHz USB clock is generated internally from PLL

In this case, PLL frequency has to be an integer multiple of 48MHz, which usually causes big errors in audio sample rate. Table 1 lists the errors at every usable PLL frequency.

Table 1 Audio sample errors at N * 48MHz PLL frequencies

PLL Freq (MHz)	Audio Sample Rate Errors (%)			MAX Error (%)
	48kHz	44.1kHz	32kHz	
48	-2.34	6.29	-2.34	6.29
96	-2.34	-5.52	-2.34	5.52
144	-2.34	-1.88	-2.34	2.34
192	-2.34	0.04	1.90	2.34
240	-2.34	1.23	1.02	2.34
288	1.90	-1.88	0.45	1.90
336	1.27	-0.79	0.04	1.27
384	0.81	0.04	-0.27	0.81

The 336MHz of PLL frequency can be used. Table 2 gives the register settings and every audio sample errors for it.

Table 2 Jz4730 I2S clock & USB clock generation parameter and sample rate errors

PLL	CFCR		I2SDIV	Sample Rate (kHz)	Error (%)
M = 56, N = 2	I2S	UDIV	DV		
PLL-freq = 336MHz	0	6	27	48	1.27
			30	44.1	-0.79
			41	32	0.04
			55	24	-0.57
			60	22.05	-0.79
			82	16	0.04
			109	12	0.34
			119	11.025	0.04
	1		82	8	0.04

Case 2: PLL does not need to provide 48MHz USB clock

In this case, we have more freedom to select PLL frequency and get less audio sample rate error. Table 3, Table 4 and Table 5 list the errors at every PLL frequency for 3.6864MHz, 4MHz and 12MHz EXCLK respectively.

Table 3 Audio sample errors at different PLL frequencies for EXCLK=3.6864MHz

PLL			Max Sample Rate Error
M	N	Freq (MHz)	
67	2	123.49	0.56%
80	2	147.46	0.47%
139	3	170.80	0.86%
134	2	246.99	0.56%
141	2	259.89	0.86%
147	2	270.95	0.23%
152	2	280.17	0.87%
239	3	293.68	0.42%
248	3	304.74	0.80%
259	3	318.26	0.68%
268	3	329.32	0.74%
278	3	341.61	0.86%
292	3	358.81	0.69%
201	2	370.48	0.56%
208	2	383.39	0.65%
214	2	394.44	0.31%

Table 4 Audio sample errors at different PLL frequencies for EXCLK=4MHz

PLL			Max Sample Rate Error
M	N	Freq (MHz)	
62	2	124	0.91%
110	3	146.67	0.54%
128	3	170.67	0.79%
185	3	246.67	0.69%
130	2	260	0.82%
203	3	270.67	0.12%
210	3	280	0.93%
147	2	294	0.31%
229	3	305.33	0.74%
159	2	318	0.60%
247	3	329.33	0.74%
256	3	341.33	0.79%
269	3	358.67	0.72%
278	3	370.67	0.55%
287	3	382.67	0.61%
197	2	394	0.29%

Table 5 Audio sample errors at different PLL frequencies for EXCLK=12MHz

PLL			Max Sample Rate Error
M	N	Freq (MHz)	
103	10	123.6	0.59%
49	4	147	0.31%
128	9	170.67	0.79%
157	8	235.5	0.87%
103	5	247.2	0.59%
65	3	260	0.82%
45	2	270	0.35%
203	9	270.67	0.12%
113	5	271.2	0.32%
187	8	280.5	0.75%
237	10	284.4	0.81%
49	2	294	0.31%
178	7	305.14	0.67%
53	2	318	0.60%
302	11	329.45	0.70%
256	9	341.33	0.79%
318	11	346.91	0.88%
206	7	353.14	0.90%
299	10	358.8	0.69%
247	8	370.5	0.55%
351	11	382.91	0.55%
230	7	394.29	0.27%