Jz4730

32 Bits Microprocessor

Application Notes 001

Clock

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Release history

Date	Revision	Change
Sep. 2006	0.7	Before release
Oct. 2006	0.8	Enhanced
Nov. 2006	0.9	Add I2S clock generation approach 2
Feb. 2007	1.0	Move I2S clock/configuration to 002

Disclaimer

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Jz4730 Clock

1. Jz4730 clock overview

This section describes clock system in Jz4730.

There is an internal PLL in Jz4730. PLL input clock is an external input clock EXCLK. Theoretically, EXCLK can be 2MHz ~ 20MHz.

cclk is CPU clock. It is usually the fastest clock in the chip. The chip speed is represented by cclk.

hclk is AHB bus, the internal fast peripheral bus, clock; pclk is APB bus, the internal slow peripheral bus, clock; and mclk is external memory bus clock. mclk represents the SDRAM speed.

cclk, hclk, pclk and mclk are synchronous clocks which may have different frequencies. They are from the same clock source, the on chip PLL output clock in most cases. hclk frequency can be equal to cclk or divided cclk by or an integer. pclk frequency can be equal to hclk or divided hclk by or an integer. mclk frequency can be equal to or half of hclk.

ETH, Ethernet MAC, module needs two 25MHz clocks. They are inputted from external Ethernet PHY.

UDC, USB device controller, and UHC, USB host controller, modules need a 48MHz USB clock. USB clock can be selected by software between external input and divided PLL output clock.

AC97 in AIC module needs a 12.288MHz BIT clock. It is input from the external AC97 CODEC chip or other clock source.

I2S in AIC module also needs a BITCLK clock. The frequency of the BITCLK is 64 times of the audio sample rate. Optionally, Jz4730 needs to provide the system clock for the external audio CODEC, which is 256 times of the audio sample rate. So for 48kHz sample rate, BITCLK frequency is 3.072MHz, system clock is 12.288MHz, for 44.1kHz they are 2.8224MHz and 11.2896MHz. The BITCLK can be provided by the external I2S audio CODEC, other chip or by Jz4730, according to CODEC chip and I2S work mode selection. So does the system clock. If Jz4730 needs to provide it, PLL output clock frequency should be set to one of some specified values.

Besides PLL input, EXCLK also provides device clock or one of device clocks for many peripherals, such as, UART, I2C, PWM, SCC, SSI and OST.

Device clock of MSC (MMC/SD) is taken from 48MHz USB clock and divides it by 2 or 3.

LCD's device clock and pixel clock are generated from PLL output clock, which are divided by two independent dividers.

The slowest clock is RTCLK, which is usually 32768Hz. It can be input from external or divided EXCLK by 128.

2. PLL out clock frequency selection

PLL-freq = PLL-freq-raw / NO,   where NO = 1, 2, 4
PLL-freq-raw = EXCLK * M / N,   where M = integer of 2 ~ 513, N = integer of 2 ~ 33

So, to generate a specified PLL-freq, there are many valid sets of NO, M and N value.

Smaller PLL-freq-raw is better since it consumes less power. Reduce PLL-freq-raw from 200MHz to 100MHz saving a few milliwatts. Please beware not put PLL-freq-raw less than 100MHz.

If EXCLK is in small jitter, like a crystal-generated clock, a smaller N is better.

3. USB clock selection

USB 48MHz clock can be selected between an external input and dividing from PLL out. Using an external 48MHz clock needs more hardware components and consumes more power in system view. The drawback of using an internal USB clock is limiting the PLL out clock frequency to an integer multiple of 48MHz. PLL out clock must be one of 96MHz, 144MHz, 192MHz, 240MHz, 288MHz, 336MHz, 384MHz and so on.

4. RTCLK selection

The “real time” clock RTCLK can be selected between RTCLK pin input and EXCLK dividing by 128. The major difference between these two approaches is in hibernating mode. In hibernating mode, if RTCLK pin input is selected, EXCLK OSC can be shut down, which saves more than 100uA power. If real time and hibernating mode are not concerned, choose EXCLK dividing by 128 reduces system components.

5. EXCLK frequency selection

To use Jz4730 processor, a crystal or a clock input, called EXCLK, with frequency between 2MHz and 20MHz is needed.

EXCLK provides PLL input clock, an alternative RTCLK after dividing it by 128, device clocks for UART, SCC, SSI, OST, WDT, I2C, PWM, PS2, UPRT. The PLL output clock provides an alternative USB clock and an alternative I2S clock.

The accurate RTCLK is 32768Hz, but in our design the tolerance is big enough.

UART device clock need to be N * 16 * baud-rate, where N = 1, 2, 3 …, 2.5% tolerance.

SCC device clock should be 1MHz ~ 8MHz (for 3V) / 10MHz (for 5V).

USB clock is 48MHz, 500PPM (0.05% tolerance).

I2S clock is about 147MHz. The error of 1% cannot be recognized by ear.

All others have enough frequency tolerance.

So an arbitrary EXCLK frequency between 2MHz and 20MHz is not suggested. Here are some recommanded EXCLK frequencies.

1) 3.6864MHz
   UART can work at baud-rate of 9600, 19200, 38400, 57600, 115200 and 230400. The baud-rate error is the same as EXCLK.

   SCC is OK.

   USB clock is 47.9232MHz, which has error of 0.16%.

   Please reference to *AN4730_002_i2s.doc* for I2S clock.

2) 4MHz
   UART can work at baud-rate of 9600 and 19200. The baud-rate error is 0.16%.

   SCC is OK.

   USB clock is 48MHz with the error of EXCLK.

   Please reference to *AN4730_002_i2s.doc* for I2S clock.

3) 12MHz
   UART can work at baud-rate of 9600, 19200 and 57600. The baud-rate error is 0.16%.

   SCC cannot be used.

USB clock is 48MHz with the error of EXCLK.

Please reference to *AN4730_002_i2s.doc* for I2S clock.

The software for all above affected modules may need to change according to EXCLK frequency.

6. EXCLK Oscillator

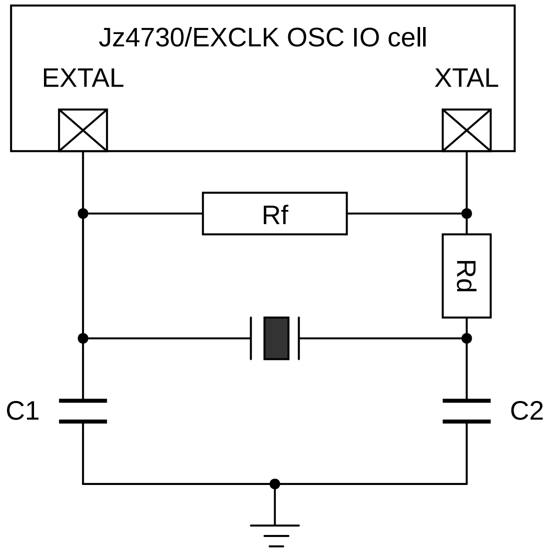

Figure 1. Oscillating circuit for fundamental mode

To turn on the oscillator, the oscillating circuit must provide the negative resistance (-Re) at least five times the equivalent series resistance (ESR) of the crystal sample. For larger -Re value, faster turn on the crystal. Higher gm provides larger -Re therefore can start-up the crystal with higher ESR for the same load capacitance (CL). However, it's required higher power consumption.

There are two key parameters to turn on oscillator. Which are CL and the maximum ESR at the target frequency. By reducing the CL, the -Re can be increased thus; shorter turn on time can be achieved. However, if CL is too small, the deviation from the target frequency will increase because of the capacitance variation. So, a trade-off relationship between short turn on time and small frequency deviation in deciding CL value. The smaller ESR of the crystal sample will reduce turn on time but the price is higher. The typical CL and ESR values for difference target frequencies are listed in Table 1.

Table 1 Typical CL and the corresponding maximum ESR

Target Frequency (Hz)	2M ~ 3M	3M ~ 6M	6M ~ 10M	10M ~ 20M
CL (pf)	25	20	16	12
Maximum ESR (ohm)	1K	400	100	80

Figure 1 shows the oscillating circuit is connected with the oscillator I/O cell. Components feedback resistor (Rf), damping resistor (Rd), C1 and C2 are used to adjust the turn on time, keep stability and accurate of the oscillator.

Rf is used to bias the inverter in the high gain region. It cannot be too low or the loop may not oscillate. For mega Hertz range applications, Rf of 1Mohm is applied.

Rd is used to increase stability, low power consumption, suppress the gain in high frequency region and also reduce -Re of the oscillator. Thus, proper Rd cannot be too large to cease the loop oscillating.

C1 and C2 are deciding regard to the crystal or resonator CL specification. In the steady state of oscillating, CL is defined as (C1*C2)/(C1+C2). Actually, the I/O ports, bond pad, and package pin all contribute the parasitic capacitance to C1 and C2. Thus, CL can be rewrite to (C1'*C2')/(C1'+C2'), where C1'=(C1+Cin,stray) and C2'=(C2+Cout,stray). In this case, the required C1 and C2 will be reduced.

Notice, this oscillating circuit is for parallel resonate but not series resonate. Because C1, C2, Rd and Rf are varying with the crystal specifications; therefore there is no single magic number of all the applications.