

Ingenic[®] Jz4740

Board Design Guide

Revision: 1.1

Date: Sep. 2008



北京君正集成电路有限公司
Ingenic Semiconductor Co. Ltd

Ingenic Jz4740

Board Design Guide

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Release history

| Date | Revision | Change |
|-----------|----------|---|
| Oct. 2007 | 1.0 | First release |
| Apr. 2008 | 1.01 | Fix some clerical error. |
| Sep.2008 | 1.1 | <ol style="list-style-type: none">1. Modified Main Clock and RTC oscillation circuits.2. Modified the Audio headphone and MIC-In circuits.3. Added the Smart LCD (CPU Interface) circuit example. |

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1 Overview

Jz4740 is a Multimedia Applications Processor designed by INGENIC[®], which addresses the Mobile, Multimedia, Low power requirement electronic product. Jz4740 integrates a high performance 32-bits CPU, support many Embedded Operating Systems such as Linux[™], WinCE[™], etc. It also integrates SDRAM memory controller, LCD controller, Audio Codec, Camera controller, Touch Controller, SD/MMC, I2C, USB1.1 Host, USB2.0 Device, Two UARTs, IrDA, GPIO and so on.

1.1 Introduction

This design guide provides recommendations for system designs based on the Jz4740 processor. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor.

The design guidelines in this document are used to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** Items based on INGENIC's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design that provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by INGENIC. They should be used as an example, but may not be applicable to particular designs.

Note: In this manual, processor means the Jz4740 processor if not specified.

The guidelines recommended in this manual are based on experience and simulation work completed by INGENIC while developing systems with Jz4740. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

1.2 Reference Platform

Figure 1-1 shows the Jz4740 Development Board Architecture.

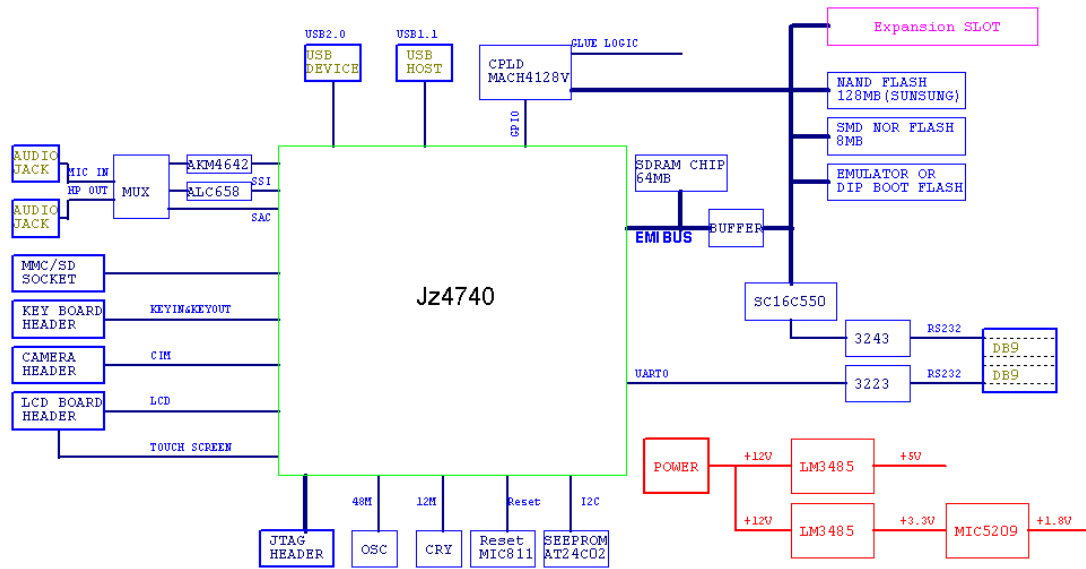


Figure 1-1 Jz4740 Development Board Architecture

2 Platform Stack-Up and Placement

In this section, an example of a Jz4740 platform component placement and stack-up is presented for a PMP product.

2.1 General Design Considerations

This section describes motherboard layout and routing guidelines for Jz4740 platforms. This section does not describe the functional of any bus, or the layout guidelines for an add-in device. If the guidelines listed in this manual are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., $60\Omega \pm 15\%$) is the nominal trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time. Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 2-1

2.2 Nominal 4-Layer Board Stack-Up

The Jz4740 platform requires a board stack-up yielding a target board impedance of $60\ \Omega \pm 5\%$. Recommendations in this design guide are based on the following a 4-layer board stack-up:

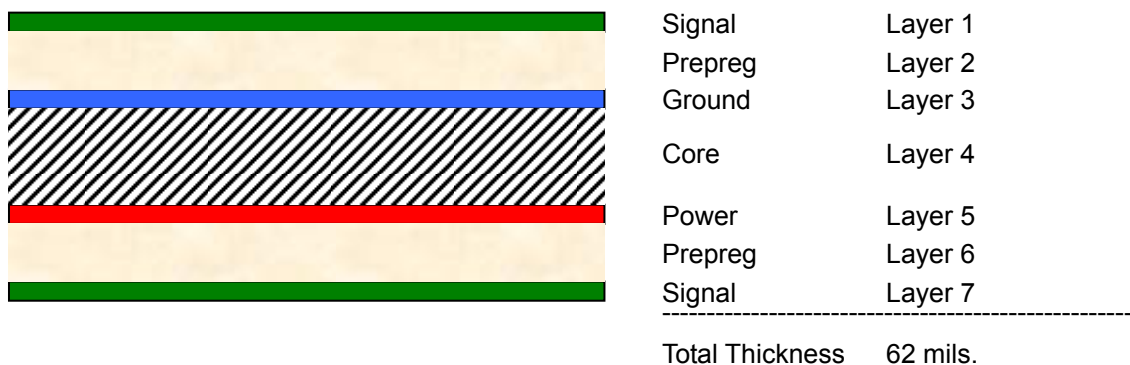


Figure 2-1 4-layer PCB Stack-Up

Table 2-1 PCB Parameter

| Description | Nominal Value | Tolerance | Comments |
|----------------------|---------------|------------|--------------------------------|
| Board Impedance Z0 | 60Ω | ± 15% | With nominal 5 mil trace width |
| Dielectric Thickness | 4.3 mils | ± 0.5 mils | 1 x 2116 Pre-Preg |
| Micro-stripline Er | 4.1 | ± 0.4 | @ 100 MHz |
| Trace Width | 5.0 mils | ± 0.5 mils | Standard trace |
| Trace Thickness | 2.1 mils | ± 0.5 mils | 0.5 oz foil + 1.0 oz plate |
| Soldermask Er | 4.0 | ± 0.5 | @ 100 MHz |
| Soldermask Thickness | 1.0 mils | ± 0.5 mils | From top of trace |

2.3 PCB Technology Considerations

The following recommendation aids in the design of a Jz4740 based platform. Simulations and reference platform are based on the following technology, and we recommend that designers adhere to these guidelines.

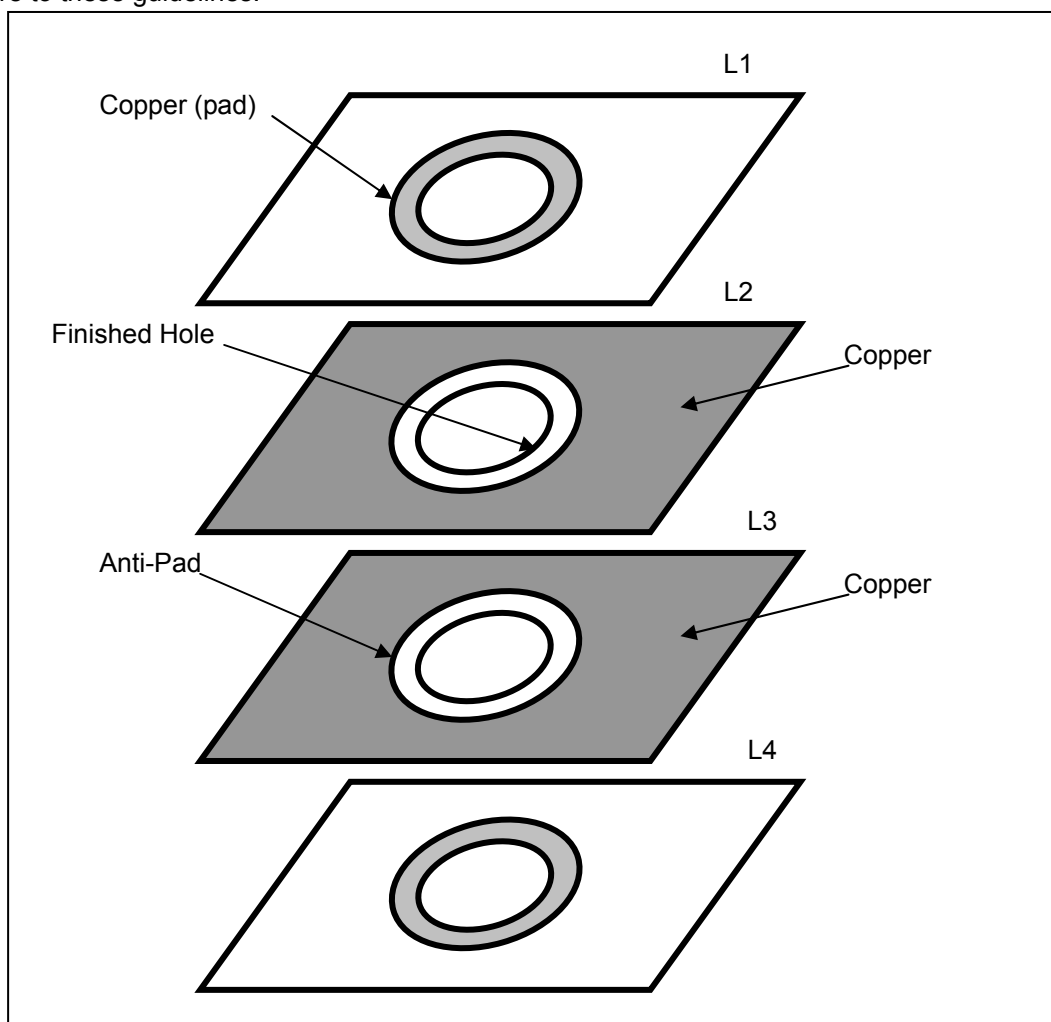


Figure 2-2 PCB Technologies – Stack-Up

Table 2-2 PCB Parameter for Vias

| Number of Layers | |
|-------------------------|--|
| Stack Up | 4 Layer |
| Cu Thickness | 0.5 oz Outer (before plating); 1oz inner |
| Final Board Thickness | 62 mils (- 5mils / +8mils) |
| Material | Fiberglass made of FR4 |
| Signal Via Stack | |
| Via Pad | 10 mils |
| Via Anti-Pad | 18 mils |
| Via Finished Hole | 8 mils |
| Signal Via Stack | |
| Via Pad | 26 mils |
| Via Anti-Pad | 40 mils |
| Via Finished Hole | 14 mils |

3 External Memory Interface Design Guidelines

3.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of memory and bus interfaces. It enables the connection of static memory, NAND flash memory, synchronous DRAM, etc., to this processor.

This section is the design guidelines for the external memory interface.

3.2 Static Memory Interface

The static memory controller provides a glueless interface to ROM, Burst ROM, SRAM, NOR Flash and NAND Flash. It supports 4 chips selection CS4~1# and each bank can be configured separately. Jz4740 supports most types of NAND flashes, including SLC and MLC, 8-bit and 16-bit bus width, 512B and 2KB page size. It also support boot from NAND flash. The data bus width for each chip select region may be programmed to be 8-bit, 16-bit or 32-bit.

3.2.1 Boot Memory

BOOT_SEL[1:0] pins define the boot time configurations as listed in the following table.

Table 3-1 Boot Configuration

| BOOT_SEL[1] | BOOT_SEL[0] | Description |
|-------------|-------------|--|
| 0 | 0 | Boot from external ROM at CS4_ |
| 0 | 1 | Boot from USB device |
| 1 | 0 | Boot from 512 Byte page NAND flash at CS1_ |
| 1 | 1 | Boot from 2k Byte page NAND flash at CS1_ |

3.2.2 SRAM/Flash Memory Connection

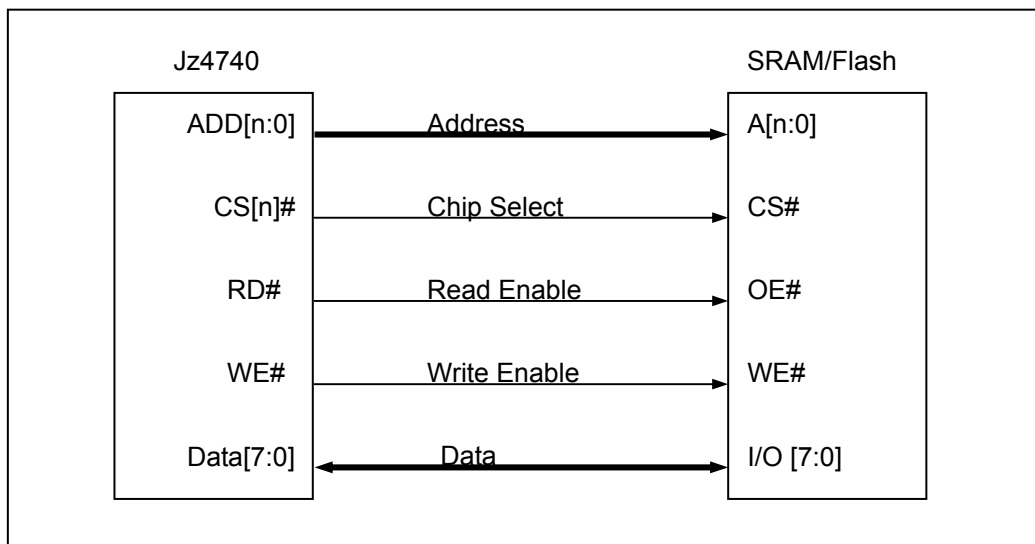


Figure 3-1 8-bit SRAM/Flash Interconnection Example

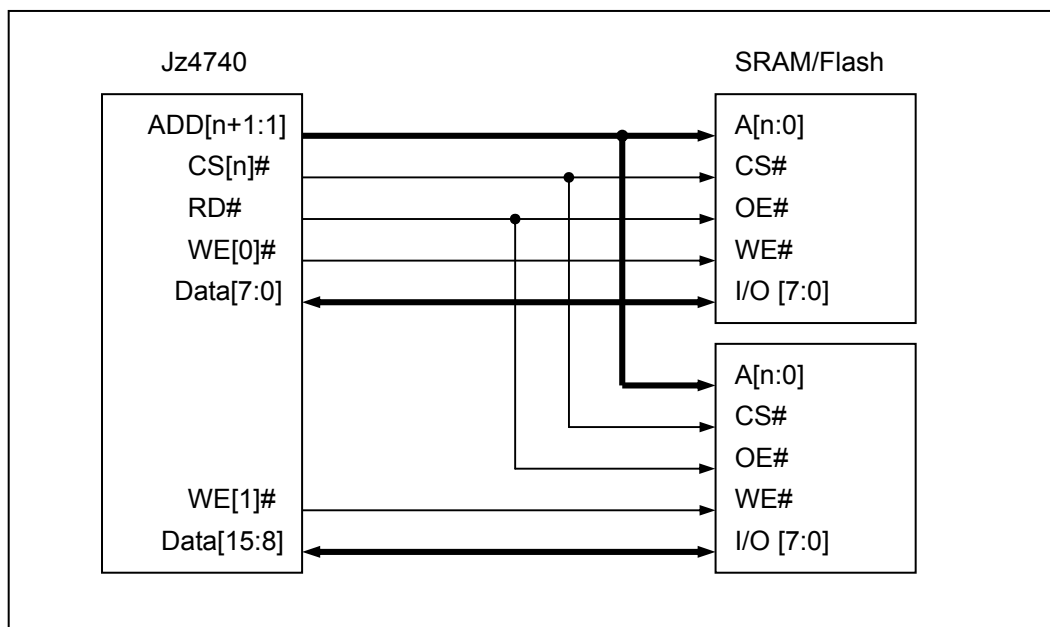


Figure 3-2 16-bit SRAM/Flash Interconnection Example

3.2.3 NAND Flash Connection

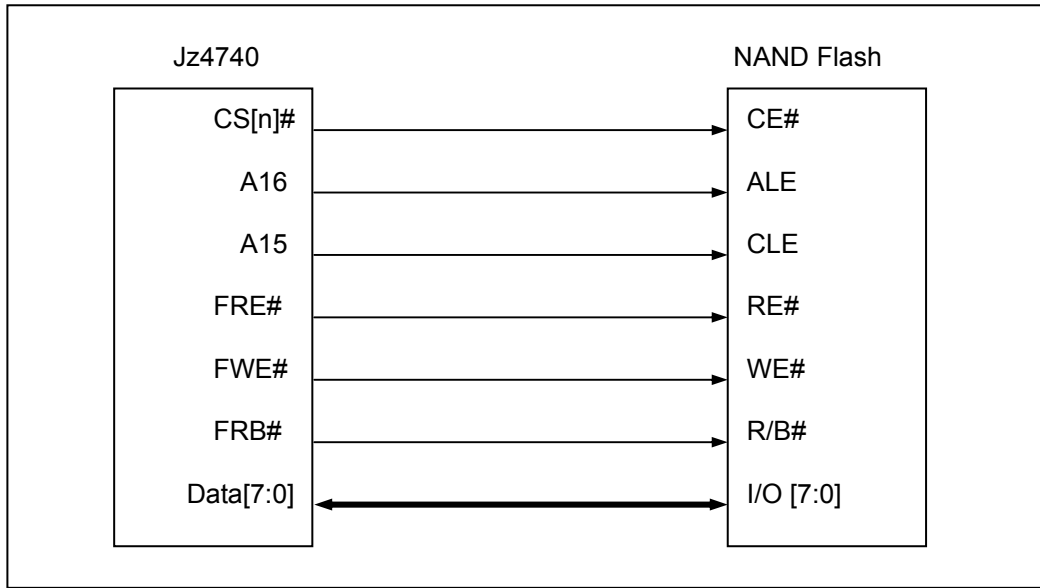


Figure 3-3 8-bit NAND Flash Interconnection Example

3.3 SDRAM

Following figure shows an example of connection of 512K x 16-bit x 2-bank synchronous DRAM.

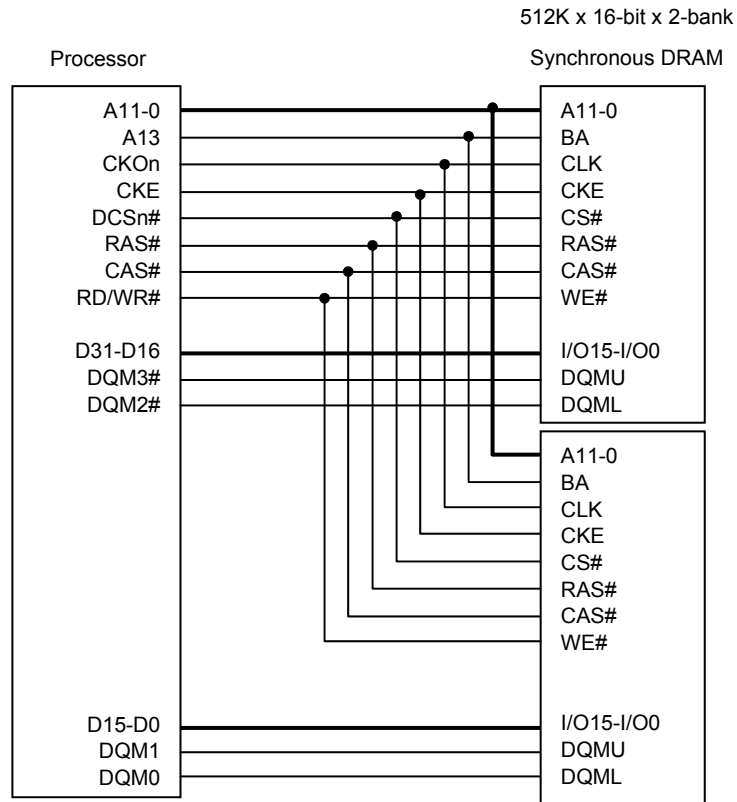


Figure 3-4 Example of Synchronous DRAM Chip Connection (1)

Following figure shows an example of connection of 1M x 16-bit x 4-bank synchronous DRAM.

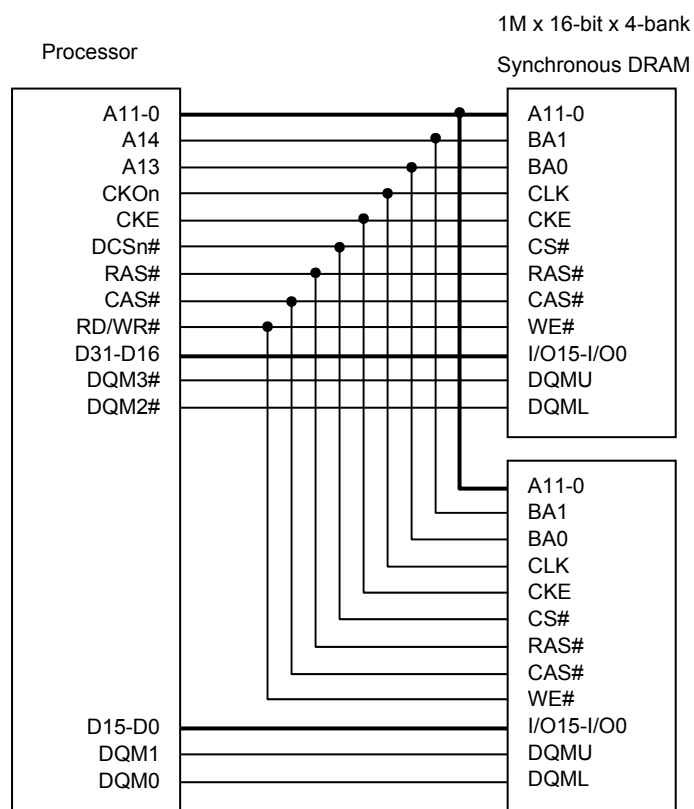


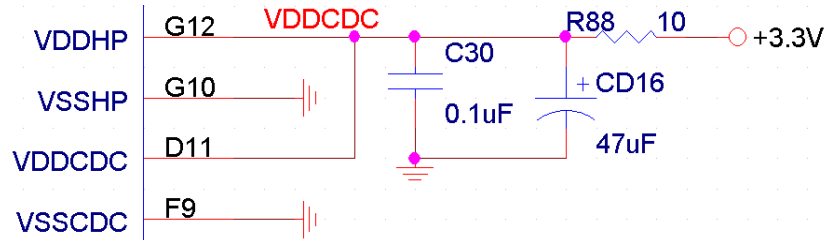
Figure 3-5 Example of Synchronous DRAM Chip Connection (2)

4 Audio Design Guidelines

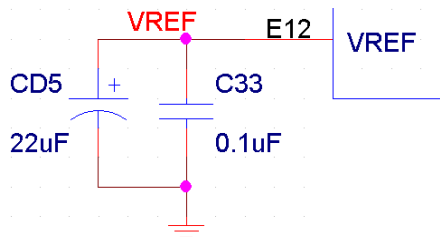
The Jz4740 has an internal Audio Codec with 18 bits DAC and 16 bits ADC.

4.1 Audio Power

VDDHP and VDDCDC should be connected to a cleaned +3.3V power.

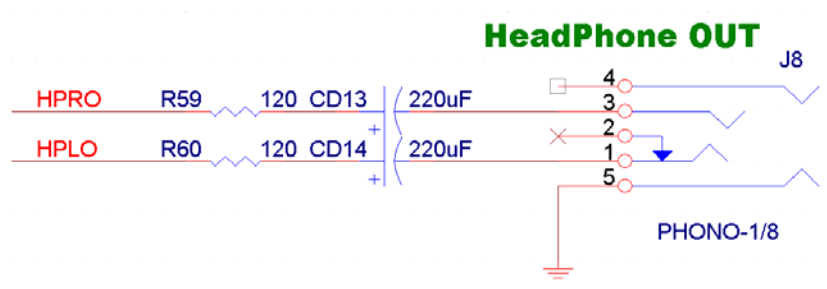


Vref should be connected to a 22uF~47uF Tantalum Capacitor and 0.1uF Ceramic Capacitor.

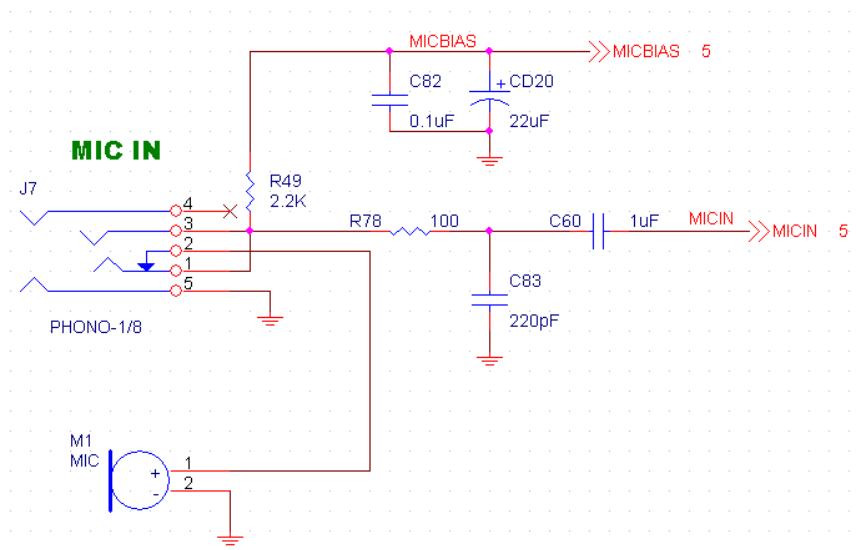


4.2 Headphone Out

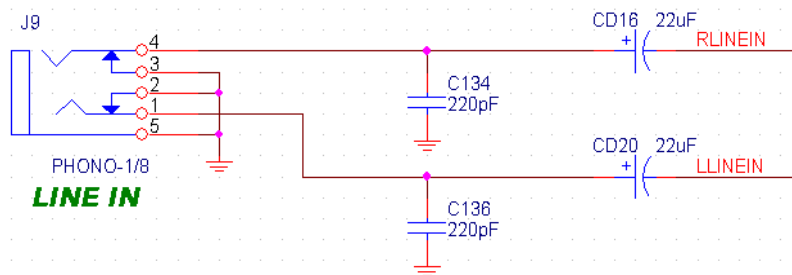
The headphone out should be coupled through a 100uF~220uF Tantalum Capacitor (CD13,CD14). The serial resistor (R59,R60) should be 120 Ohm, they can enhance the low frequency DB correspond to high frequency.



4.3 Mic In



4.4 Line In



4.5 Layout Guideline

To ensure the maximum performance of the Audio, proper component placement and routing techniques are required. These techniques include properly isolating associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes could be provided, with the digital components

over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.

- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

5 USB Design Guidelines

Jz4740 integrates USB Host Controller (UHC), which is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.

Jz4740 also integrates USB device controller (UDC), which is USB Revision 2.0-compliant High-speed device.

The following are general guidelines for the USB Host Revision 1.1 interface:

- Unused USB Host ports should be terminated with 15 k Ω pull-down resistors on both D1+/D1- data lines.
- 15 Ω series resistors should be placed as close as possible to the Jz4740. These series resistors provide source termination of the reflected signal and the value can be adjusted.
- 47-pF caps must be placed as close as possible to the Jz4740 as well as on the processor side of the series resistors on the USB data lines (D1 \pm). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 k Ω \pm 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (D1 \pm). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the D \pm signals should be 45 Ω (to ground) for each USB signal D+ or D-. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 5-1. The impedance is 90 Ω between the differential signal pairs D+ and D-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals'. (i.e., hand-routing preferred). The D+/D- signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the D+/D- signal pair to adjacent signal traces will help to prevent cross-talk. The D+/D- signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

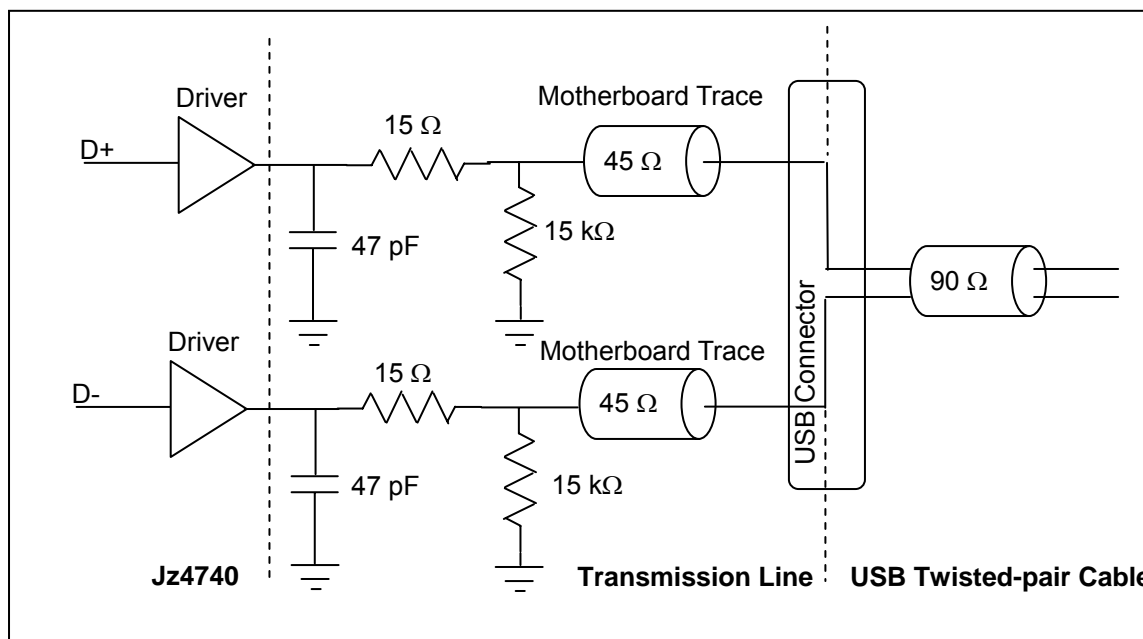


Figure 5-1 Recommend USB Host Schematic

The following are general guidelines for the USB Device Revision 2.0 interface:

- The trace should be connected to the connector directly without any resistors and capacitors.
- The trace impedance for the D_{\pm} signals should be $45\ \Omega$ (to ground) for each USB signal $D+$ or $D-$. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 5-2. The impedance is $90\ \Omega$ between the differential signal pairs $D+$ and $D-$, to match the $90\ \Omega$ USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of $90\ \Omega$ is the series impedance of both wires, which results in an individual wire presenting $45\ \Omega$ impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals'. (i.e., hand-routing preferred). The $D+/D-$ signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the $D+/D-$ signal pair to adjacent signal traces will help to prevent cross-talk. The $D+/D-$ signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

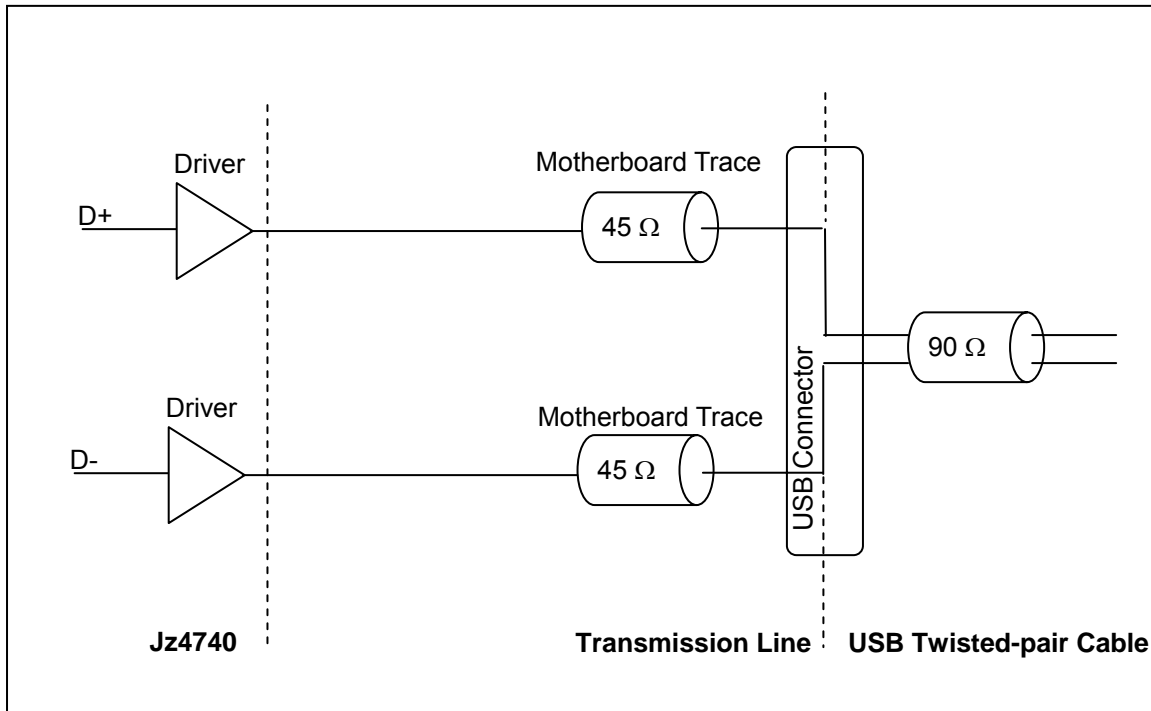


Figure 5-2 Recommend USB Device Schematic

6 LCD

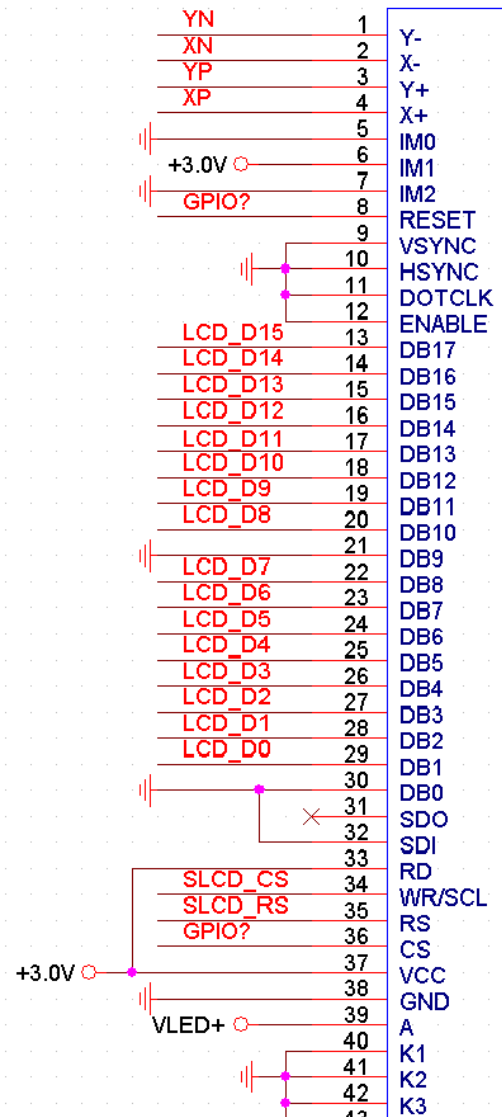
The Jz4740 integrated LCD controller has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller.

Table 6-1 TFT Pin Mapping

| Jz4740 Pin | 8-bit Serial RGB | 16-bit Parallel RGB | 18-bit Parallel RGB | Smart LCD Serial | Smart LCD Parallel |
|-------------------|------------------|---------------------|---------------------|------------------|--------------------|
| LCD_PCLK/SLCD_CLK | CLK | CLK | CLK | CLK | |
| LCD_HSYNC/SLCD_RS | HSYNC | HSYNC | HSYNC | | RS |
| LCD_VSYNC/SLCD_CS | VSYNC | VSYNC | VSYNC | | CS |
| LCD_D17 | | | R7 | | D17 |
| LCD_D16 | | | R6 | | D16 |
| LCD_D15 | | R7 | R5 | Data | D15 |
| LCD_D14 | | R6 | R4 | | D14 |
| LCD_D13 | | R5 | R3 | | D13 |
| LCD_D12 | | R4 | R2 | | D12 |
| LCD_D11 | | R3 | G7 | | D11 |
| LCD_D10 | | G7 | G6 | | D10 |
| LCD_D9 | | G6 | G5 | | D9 |
| LCD_D8 | | G5 | G4 | | D8 |
| LCD_D7 | R7/G7/B7 | G4 | G3 | | D7 |
| LCD_D6 | R6/G6/B6 | G3 | G2 | | D6 |
| LCD_D5 | R5/G5/B5 | G2 | B7 | | D5 |
| LCD_D4 | R4/G4/B4 | B7 | B6 | | D4 |
| LCD_D3 | R3/G3/B3 | B6 | B5 | | D3 |
| LCD_D2 | R2/G2/B2 | B5 | B4 | | D2 |
| LCD_D1 | R1/G1/B1 | B4 | B3 | | D1 |
| LCD_D0 | R0/G0/B0 | B3 | B2 | | D0 |
| LCD_DE | DE | DE | DE | | |
| LCD_PS | | | | | |
| LCD_CLS | | | | | |
| LCD_REV | | | | | |
| LCD_SPL | | | | | |

The following is the example of smart LCD (CPU Interface) circuit:

SLCD_CS can drive either the CS signal or WR signal of smart LCD. Usually we connect the SLCD_CS to WR, and use a GPIO to control the CS signal.



7 Camera

The CIM (Camera Interface Module) of Jz4740 connects to a CMOS or CCD type image sensor. The CIM source the digital image stream through a common parallel digital protocol.

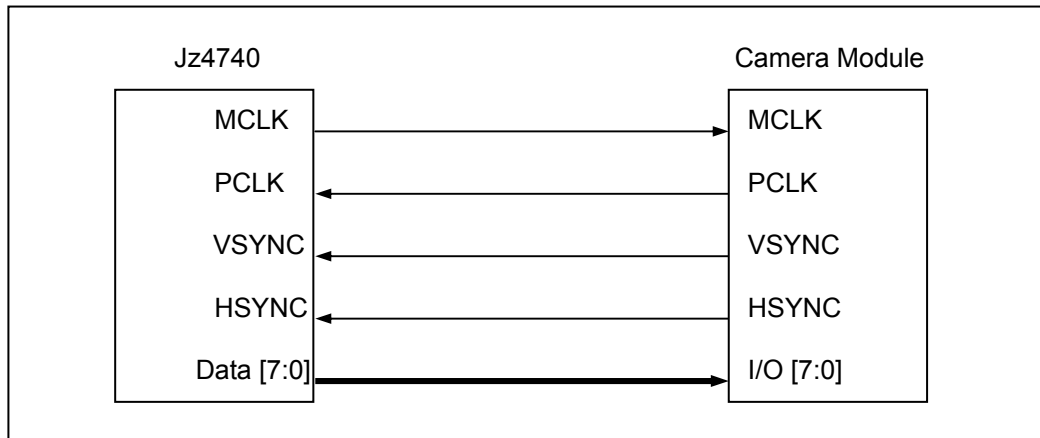


Figure 7-1 Example of Camera Module Interconnection

8 SAR A/D Controller

The A/D in Jz4740 is COMS low-power dissipation 12bit SAR analog to digital converter.

The SAR A/D Controller of Jz4740 can work at three different modes: Touch Screen (measure pen position and pen down pressure), Battery (check the battery power), and SADCIN (external ADC input).

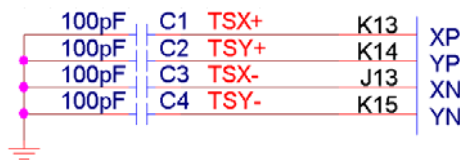
Table 8-1 SADC Pins Description

| NAME | I/O | Description |
|----------------|-----|--|
| XN | AI | Touch screen analog differential X- position input |
| YN | AI | Touch screen analog differential Y- position input |
| XP | AI | Touch screen analog differential X+ position input |
| YP | AI | Touch screen analog differential Y+ position input |
| ADIN0 (PBAT) | AI | Analog input for VBAT measurement (0~5V) |
| ADIN1 (SADCIN) | AI | External SAR-ADC input (0~2.5V) |

8.1 Touch Screen

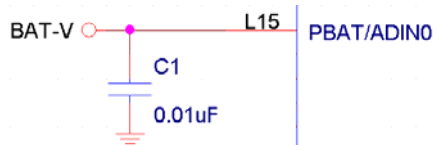
The Jz4740 can only support 4-wire resistive touch screen.

There is needed a decouple capacitor for every channel to avoid the crosstalk from LCD. The value is decided by the touch screen and can be from 100pF to 1000pF.



8.2 Battery Voltage Measurement

The battery voltage measurement can only use the ADIN0 channel. There is needed a decouple capacitor to avoid the crosstalk.



9 Ethernet Design Guidelines

The Jz4740 processor doesn't contain Ethernet media access controller (MAC). So we need an Ethernet controller that is external to the processor. This section describes design guidelines for the LAN on board based Jz4740.

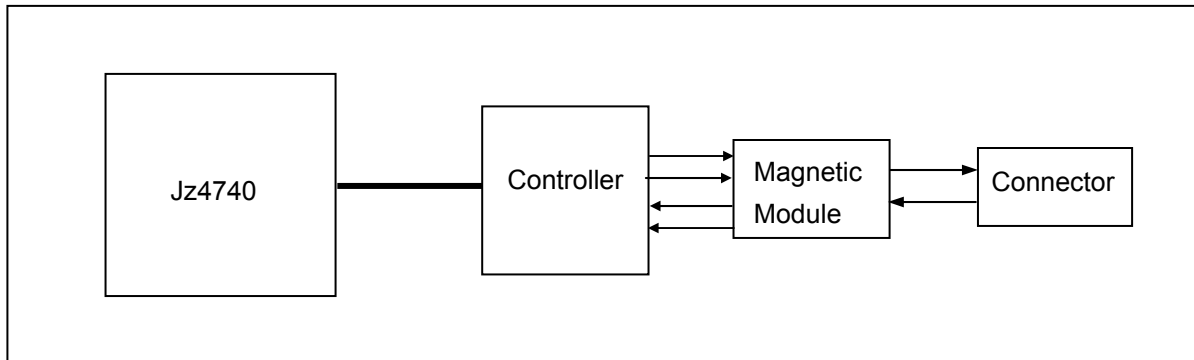


Figure 9-1 LAN On Board Implementation

9.1 Jz4740 Ethernet Controller Connection

Jz4740 Ethernet controller interconnection example is shown as figure 9-2, the Ethernet Controller chip maybe varied for specific OEM design targets. Jz4740 RESETOUT_ drive the RESET input to reset the CONTROLLER chip when power-up.

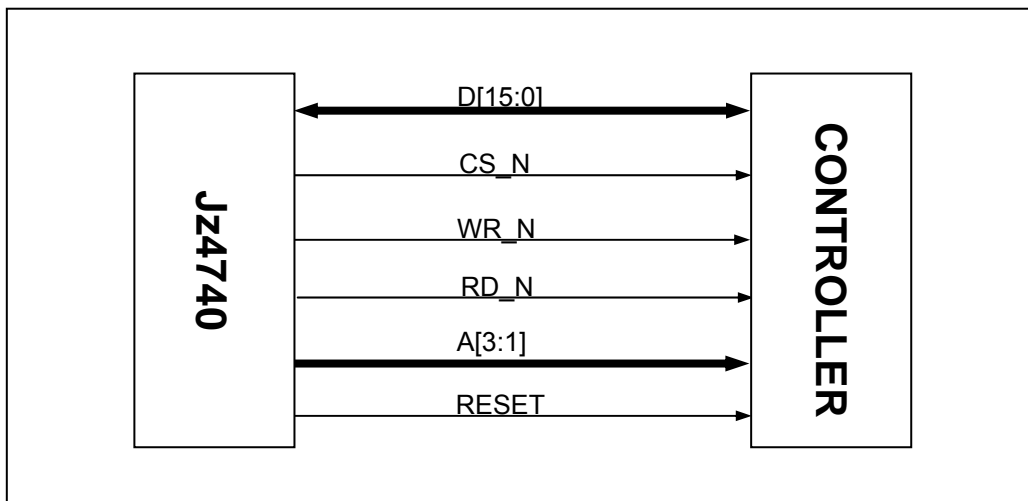


Figure 9-2 CS8900A Ethernet Controller Connection

10 RTC

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, a power-on-reset generator, the real time and alarm logic, and the power down and wakeup control logic.

The external WAKEUP_N pin is with up to 2s glitch filter / alarm wakeup.

10.1 RTC Clock

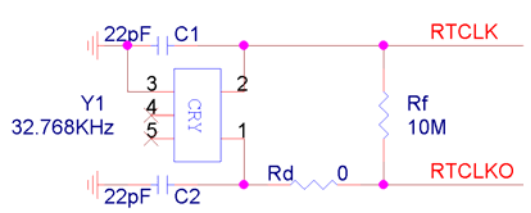


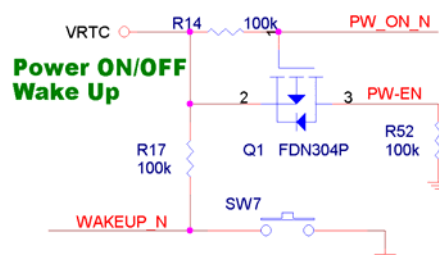
Table 10-1 RTC Clock Routing Summary

| Trace Impedance | Routing Requirements | Maximum Trace Length To Crystal | Signal Length Matching | R1, R2, C1, and C2 Tolerances | Signal Referencing |
|---|--|---------------------------------|------------------------|---|--------------------|
| 45 Ω to 69 Ω , 60 Ω Target | 5 mil trace width (results in ~2pF per inch) | 1 inch | NA | Rf = 10M \pm 5% Rd = 0 Ohm C1=C2=22pF \pm 10% The value of C1, C2 and Rf should be referred to the crystal's specification | Ground |

10.2 Power Control

The following is the recommended circuit for the system power control.

PW_ON_N is an Open-Drain and active low signal from CPU. If the power circuit enable signal is active low signal, you can use the PW_ON_N directly. If the power circuit enable signal is active high signal, you can use the PW-EN signal. VRTC should be on always.



11 Miscellaneous Peripheral Design Guidelines

11.1 SSI Design Guideline

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The following figures show the connection example:

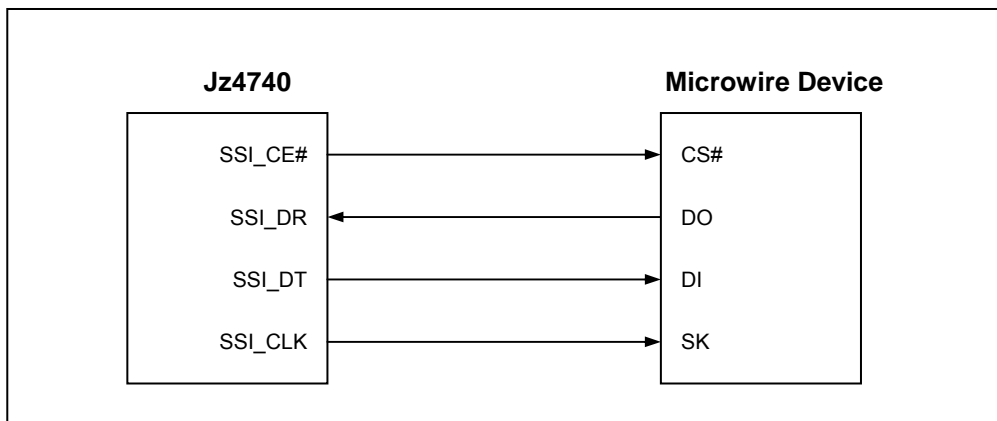


Figure 11-1 Microwire Interconnection

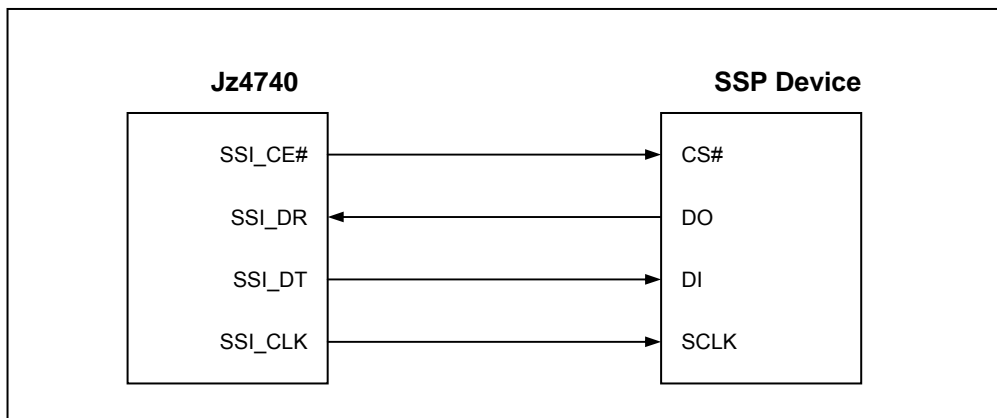


Figure 11-2 SSP Interconnection

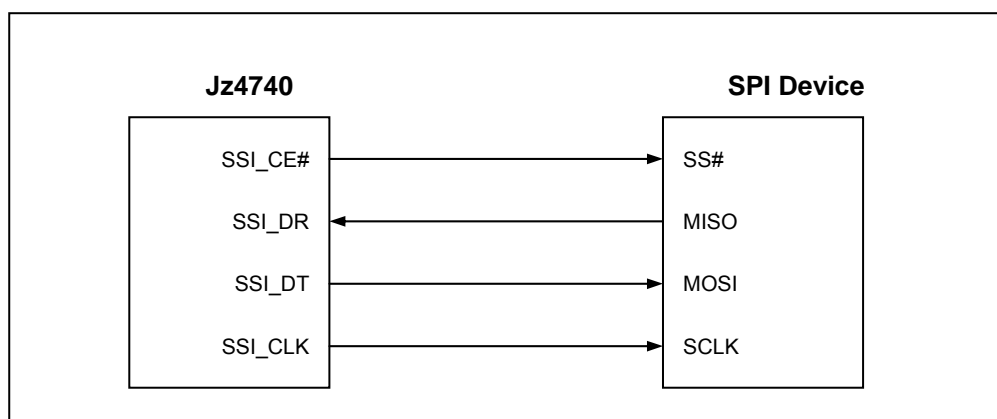


Figure 11-3 SPI Interconnection

11.2 UART/IrDA

The Jz4740 processor has two UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550 industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

11.2.1 UART Implementation

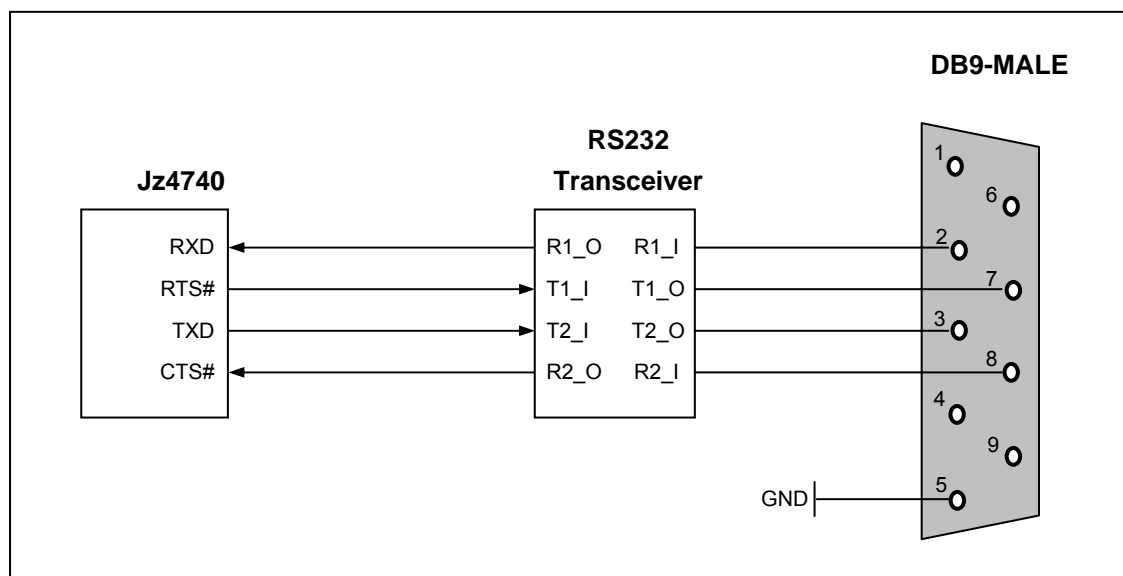


Figure 11-4 RS232 Serial Port Interconnection

11.2.2 IrDA Implementation

The Slow Infrared (SIR) interface is used with the UART to support two-way wireless communication that uses infrared transmission. The SIR provides a transmit encoder and receive decoder to support a physical link that conforms to the IrDA Serial Infrared Specification Version 1.1.

The SIR interface does not contain the actual IR LED driver or the receiver amplifier. The I/O pins attached to the SIR only have digital CMOS level signals. The SIR supports two-way communication, but full duplex communication is not possible because reflections from the transmit LED enter the receiver. The SIR interface supports frequencies up to 115.2 kbps.

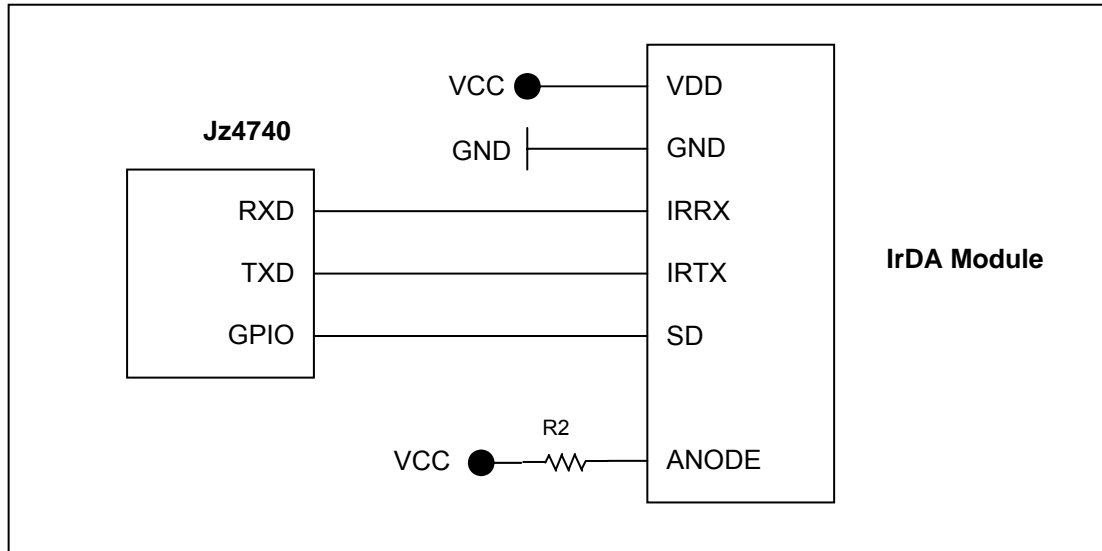


Figure 11-5 IrDA Port Interconnection

11.3 I2C Bus

The I2C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I2C bus. The I2C bus requires a minimum amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

Jz4740 support single master mode only, so only slave devices are supported on the I2C bus attached to Jz4740. The I2C module supports I²C standard-mode and F/S-mode up to 400 kHz. The interface example is shown as following figure. The I2C bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up (R1, R2=2.2K) is required on SCL and SDA. Refer to The I2C-Bus Specification for complete details on I2C bus operation.

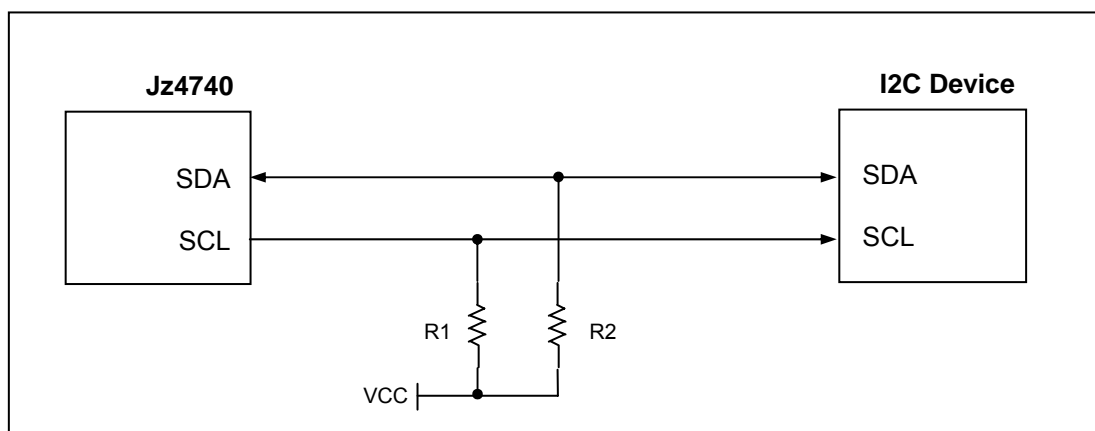


Figure 11-6 I2C Interconnection

11.4 PWM

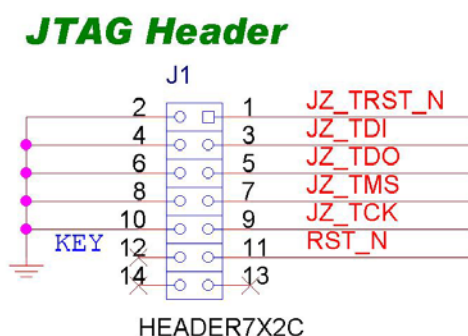
The Pulse Width Modulator (PWM) is used to control the back light inverter or adjust bright or contrast of LCD panel and also can be used to generate tone. PWM consists of a simple free-running counter with two compared registers, each compare register performs a particular task when it matches the count value. The period comparator causes the output pin to be set and the free-running counter to reset when it matches the period value. The width comparator causes the output pin to reset when the counter value matches. Jz4740 contains eight pulse width modulators: PWM0 ~ PWM7.

11.5 GPIO

The Jz4740 processor provides 128 multiplexed General Purpose I/O Ports (GPIO) for use in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

11.6 JTAG/Debug Port

Jz4740 has a built-in JTAG/Debug port. All JTAG pins are directly connected. The following figure shows the connection of the JTAG port. Pin 11 RST_N should be connected to system reset circuit. Pin 12 is a KEY. The header should be a 7X2(2.54mm Pitch) male header with coat.



12 Platform Clock Guidelines

The Jz4740 processor contains one PLL driven by the 12-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- SDRAM bus clock
- Programmable clocks needed by certain peripherals

The following is the recommended circuit for main clock.

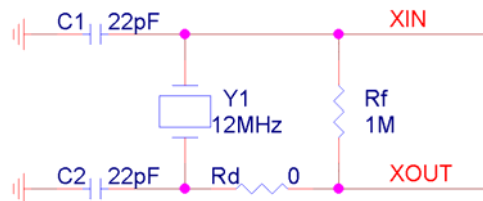
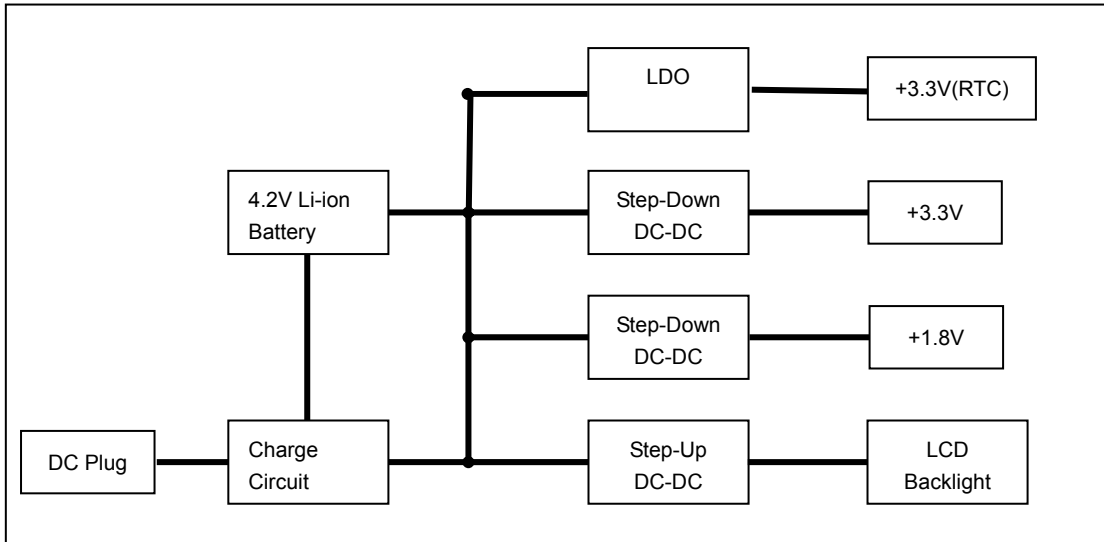


Table 12-1 Main Clock Routing Summary

| Trace Impedance | Routing Requirements | Maximum Trace Length To Crystal | Signal Length Matching | R1, R2, C1, and C2 Tolerances | Signal Referencing |
|---|--|---------------------------------|------------------------|--|--------------------|
| 45 Ω to 69 Ω , 60 Ω Target | 5 mil trace width (results in ~2pF per inch) | 1 inch | NA | Rf = 1M \pm 5% Rd = 0 Ohm C1=C2=22pF \pm 10% (Typical) The value of C1, C2 and Rf should be referred to the crystal's specification | Ground |

13 Platform Power Guidelines

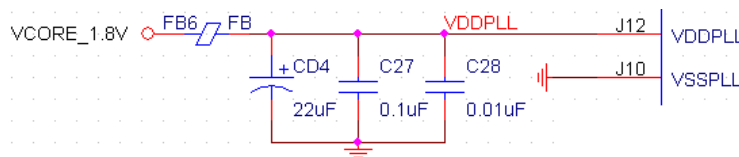
The Jz4740 processor needs two voltages: +3.3V for I/O and +1.8V for core. The following figure is a typical power circuit in the PMP application.



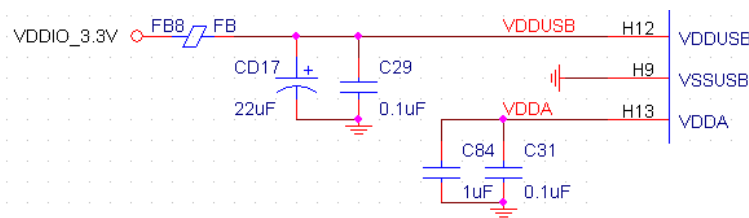
13.1 Power Delivery and Decoupling

The VDDIO (+3.3V) and VCORE (+1.8V) of Jz4740 should be decoupled with 0.1uF capacitor.

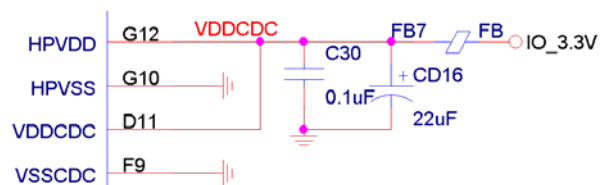
The Power of PLL should be as the following circuit.

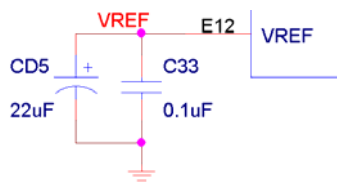


The power of USB should be as the following circuit.

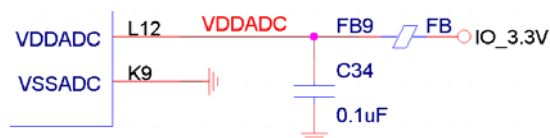


The power of Audio should be as the following circuit.





The power of ADC should be as the following circuit.



The power of RTC should be as the following circuit.



The capacitors should be placed near the Pin of power. The traces from capacitor to the Pin should be short and width.