# Ingenic® Jz4730

Board Design Guide

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# Ingenic Jz4730

## Board Design Guide



**Release history**

| Date | Revision | Change |
|---|---|---|
| Feb. 2007 | 1.0 | First release |

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# Content

# 1 Overview

Jz4730 is a Multimedia Applications Processor designed by INGENIC®, which addresses the Mobile, Multimedia, Low power requirement electronic product. Jz4730 integrates a high performance 32-bits CPU, support many Embedded Operating Systems such as Linux™, WinCE™, etc. It also integrates SDRAM memory controller, MAC, LCD controller, AC'97/I2S controller, Camera controller, SCC, SD/MMC, I2C, USB1.1 Host/Device, four UARTs, IrDA, GPIO and so on.

## 1.1 Introduction

This design guide provides recommendations for system designs based on the Jz4730 processor. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor.

The design guidelines in this document are used to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** Items based on INGENIC's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design that provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by INGENIC. They should be used as an example, but may not be applicable to particular designs.

**Note:** In this manual, processor means the Jz4730 processor if not specified.

The guidelines recommended in this manual are based on experience and simulation work completed by INGENIC while developing systems with Jz4730. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

## 1.2 Reference Platform

Figure 1-1 shows the Jz4730 Development Board Architecture.

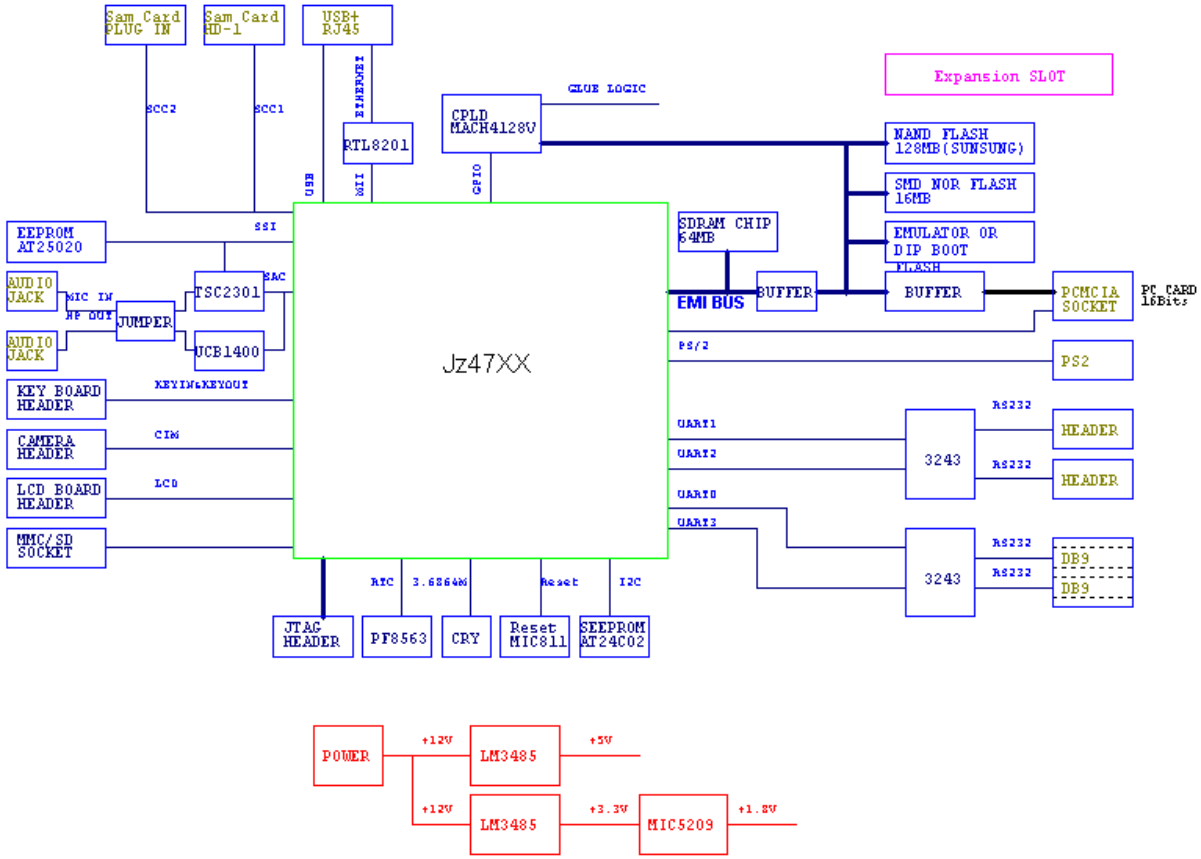



**Figure 1-1 Jz4730 Development Board Architecture**

# 2 Platform Stack-Up and Placement

In this section, an example of a Jz4730 platform component placement and stack-up is presented for a PMP product.

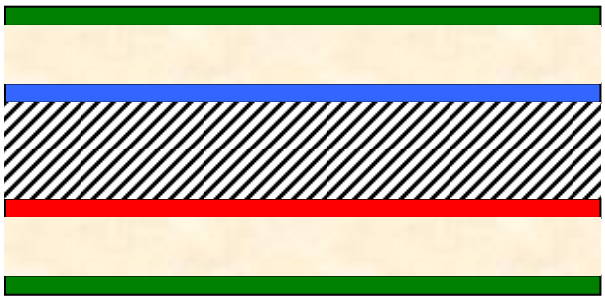
## 2.1 General Design Considerations

This section describes motherboard layout and routing guidelines for Jz4730 platforms. This section does not describe the functional of any bus, or the layout guidelines for an add-in device. If the guidelines listed in this manual are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., 60Ω ± 15%) is the nominal trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time. Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 2-1

## 2.2 Nominal 4-Layer Board Stack-Up

The Jz4730 platform requires a board stack-up yielding a target board impedance of 60 Ω ± 5%. Recommendations in this design guide are based on the following a 4-layer board stack-up:



| | |
|---|---|
| Signal | Layer 1 |
| Prepreg | Layer 2 |
| Ground | Layer 3 |
| Core | Layer 4 |
| Power | Layer 5 |
| Prepreg | Layer 6 |
| Signal | Layer 7 |
| Total Thickness | 62 mils. |

**Figure 2-1 4-layer PCB Stack-Up**

**Table 2-1 PCB Parameter**

| Description | Nominal Value | Tolerance | Comments |
|---|---|---|---|
| Board Impedance Z0 | 60Ω | ± 15% | With nominal 5 mil trace width |
| Dielectric Thickness | 4.3 mils | ± 0.5 mils | 1 x 2116 Pre-Preg |
| Micro-stripline Er | 4.1 | ± 0.4 | @ 100 MHz |
| Trace Width | 5.0 mils | ± 0.5 mils | Standard trace |
| Trace Thickness | 2.1 mils | ± 0.5 mils | 0.5 oz foil + 1.0 oz plate |
| Soldermask Er | 4.0 | ± 0.5 | @ 100 MHz |
| Soldermask Thickness | 1.0 mils | ± 0.5 mils | From top of trace |

## 2.3 PCB Technology Considerations

The following recommendation aids in the design of a Jz4730 based platform. Simulations and reference platform are based on the following technology, and we recommend that designers adhere to these guidelines.

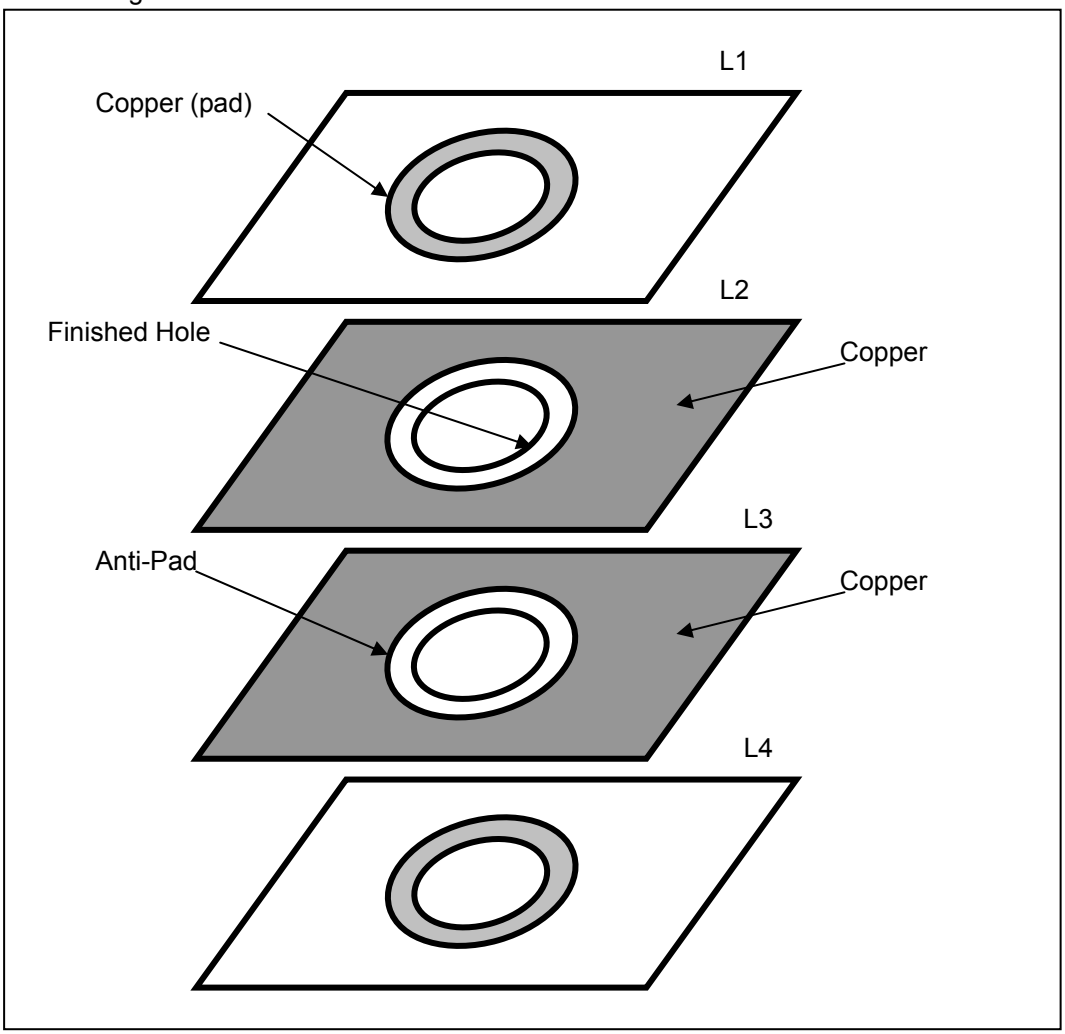



**Figure 2-2 PCB Technologies – Stack-Up**

**Table 2-2 PCB Parameter for Vias**

| **Number of Layers** | |
|---|---|
| Stack Up | 4 Layer |
| Cu Thickness | 0.5 oz Outer (before plating); 1oz inner |
| Final Board Thickness | 62 mils (- 5mils / +8mils) |
| Material | Fiberglass made of FR4 |
| **Signal and Power Via Stack** | |
| Via Pad | 26 mils |
| Via Anti-Pad | 40 mils |
| Via Finished Hole | 14 mils |

# 3 External Memory Interface Design Guidelines

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of memory and bus interfaces. It enables the connection of static memory, NAND flash memory, synchronous DRAM, etc., to this processor. It also supports the PCMCIA interface.

This section is the design guidelines for the external memory interface.

## 3.1 Overview

## 3.2 Static Memory Interface

The static memory controller provides a glue less interface to ROM, Burst ROM, SRAM, NOR Flash and NAND Flash. It support 6 chip selection CS5~0# and each bank can be configured separately. NAND flash interface is provided on CS3, sharing with static memory bank 3. Jz4730 support most types of NAND flashes, including 8-bit and 16-bit bus width, 512B and 2KB page size. It also support boot from NAND flash. The data bus width for each chip select region may be programmed to be 8-bit, 16-bit or 32-bit.

### 3.2.1 Boot Memory

BOOT_SEL[3:0] pins define the boot time configurations as listed in the following table.

**Table 3-1 Boot Configuration**

| BOOT_SEL[3] | BOOT_SEL[2] | BOOT_SEL[1] | BOOT_SEL[0] | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Boot from CS0 with 32-bit width |
| 0 | 0 | 0 | 1 | Boot from CS0 with 16-bit width |
| 0 | 0 | 1 | 0 | Boot from CS0 with 8-bit width |
| 0 | 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Boot from NAND Flash on CS3 with 8-bit width, 512B page size, 2 page address cycles |
| 1 | 0 | 0 | 1 | Boot from NAND Flash on CS3 with 16-bit width, 512B page size, 2 page address cycles |
| 1 | 0 | 1 | 0 | Boot from NAND Flash on CS3 with 8-bit width, 2KB page size, 2 page address cycles |
| 1 | 0 | 1 | 1 | Boot from NAND Flash on CS3 with 16-bit width, 2KB page size, 2 page address cycles |
| 1 | 1 | 0 | 0 | Boot from NAND Flash on CS3 with 8-bit width, 512B page size, 3 page address cycles |
| 1 | 1 | 0 | 1 | Boot from NAND Flash on CS3 with 16-bit width, 512B page size, 3 page address cycles |

| | | | | |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | Boot from NAND Flash on CS3 with 8-bit width, 2KB page size, 3 page address cycles |
| 1 | 1 | 1 | 1 | Boot from NAND Flash on CS3 with 16-bit width, 2KB page size, 3 page address cycles |

When boot from CS0, BOOT_SEL[1:0] is used to define the memory width which can be 8,16 or 32 bits. When boot from NAND flash, the data width of static memory bank 3 is defined by BOOT_SEL[0] pins which can be 8 or 16 bits. Data width of other static memory banks can be configured to 8, 16 or 32 bits by software.

### 3.2.2 SRAM/Flash Memory Connection

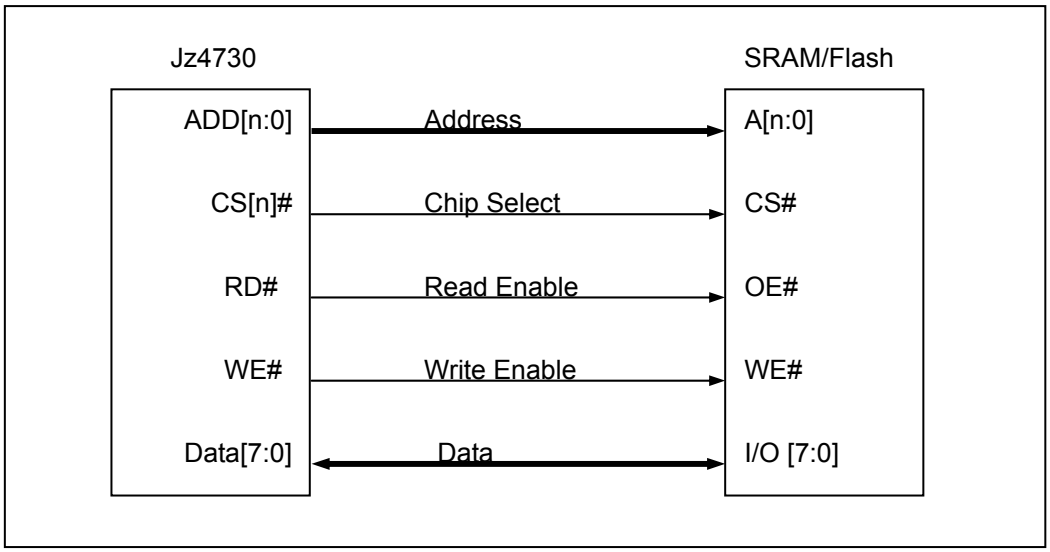



**Figure 3-1 8-bit SRAM/Flash Interconnection Example**

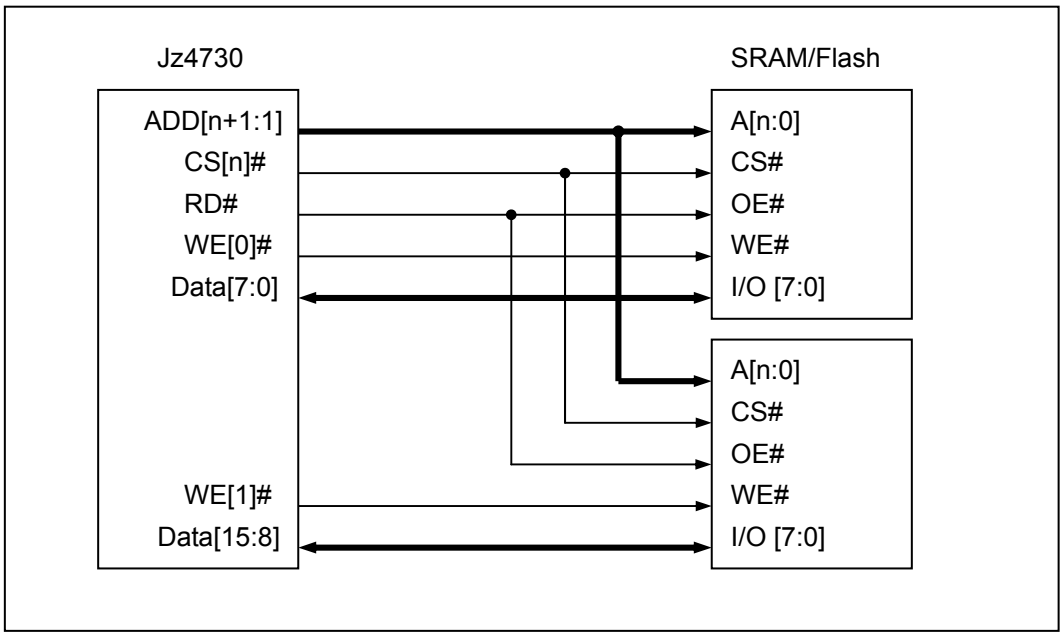



**Figure 3-2 16-bit SRAM/Flash Interconnection Example**

### 3.2.3 NAND Flash Connection

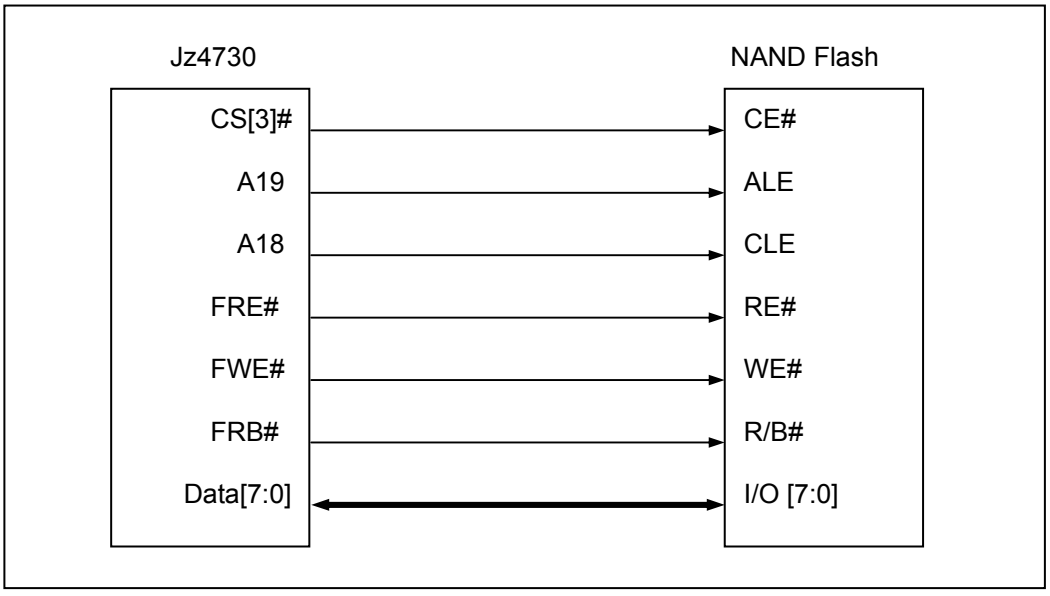



**Figure 3-3 8-bit NAND Flash Interconnection Example**

### 3.2.4 16-bit PC Card/CF Card Interface

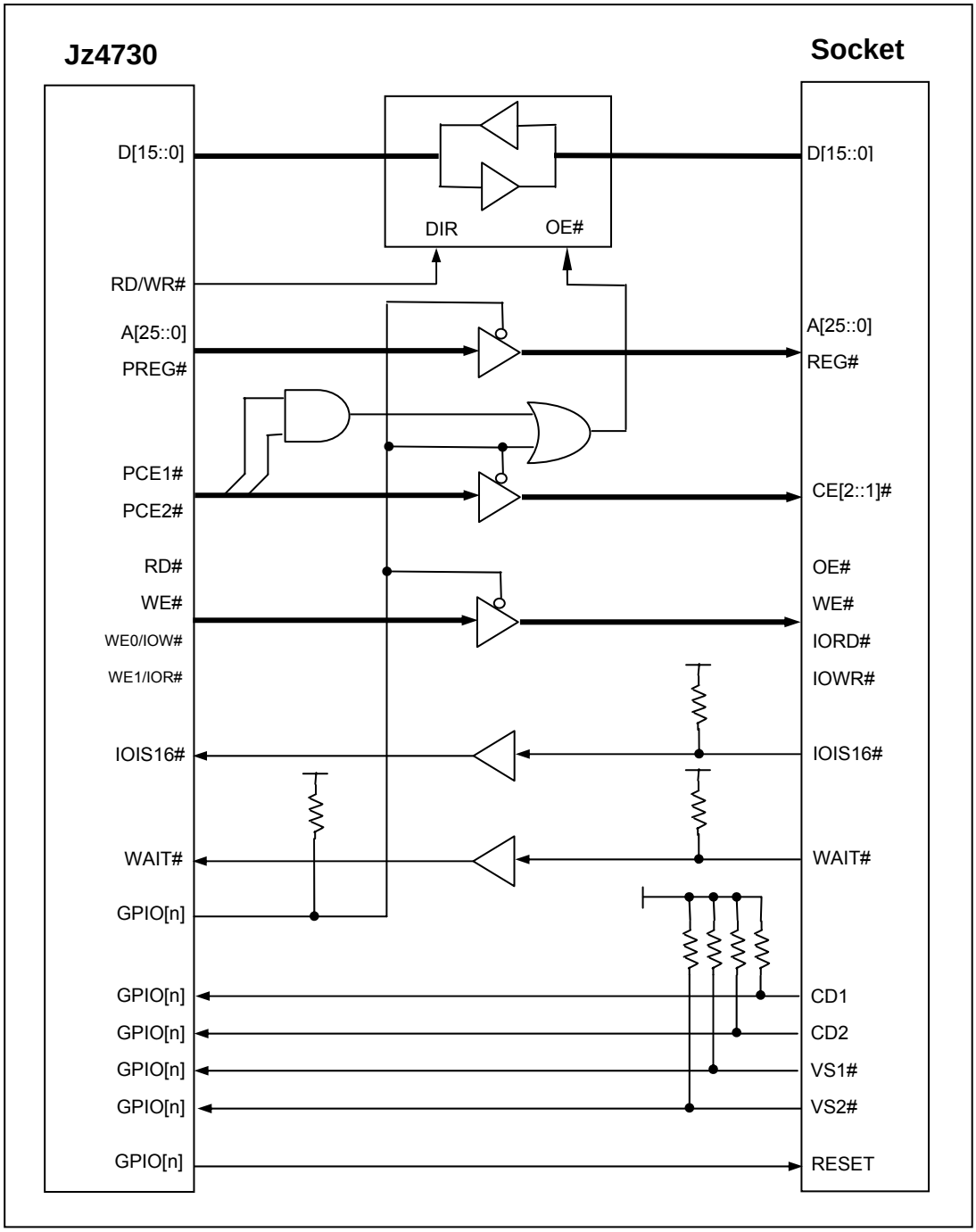
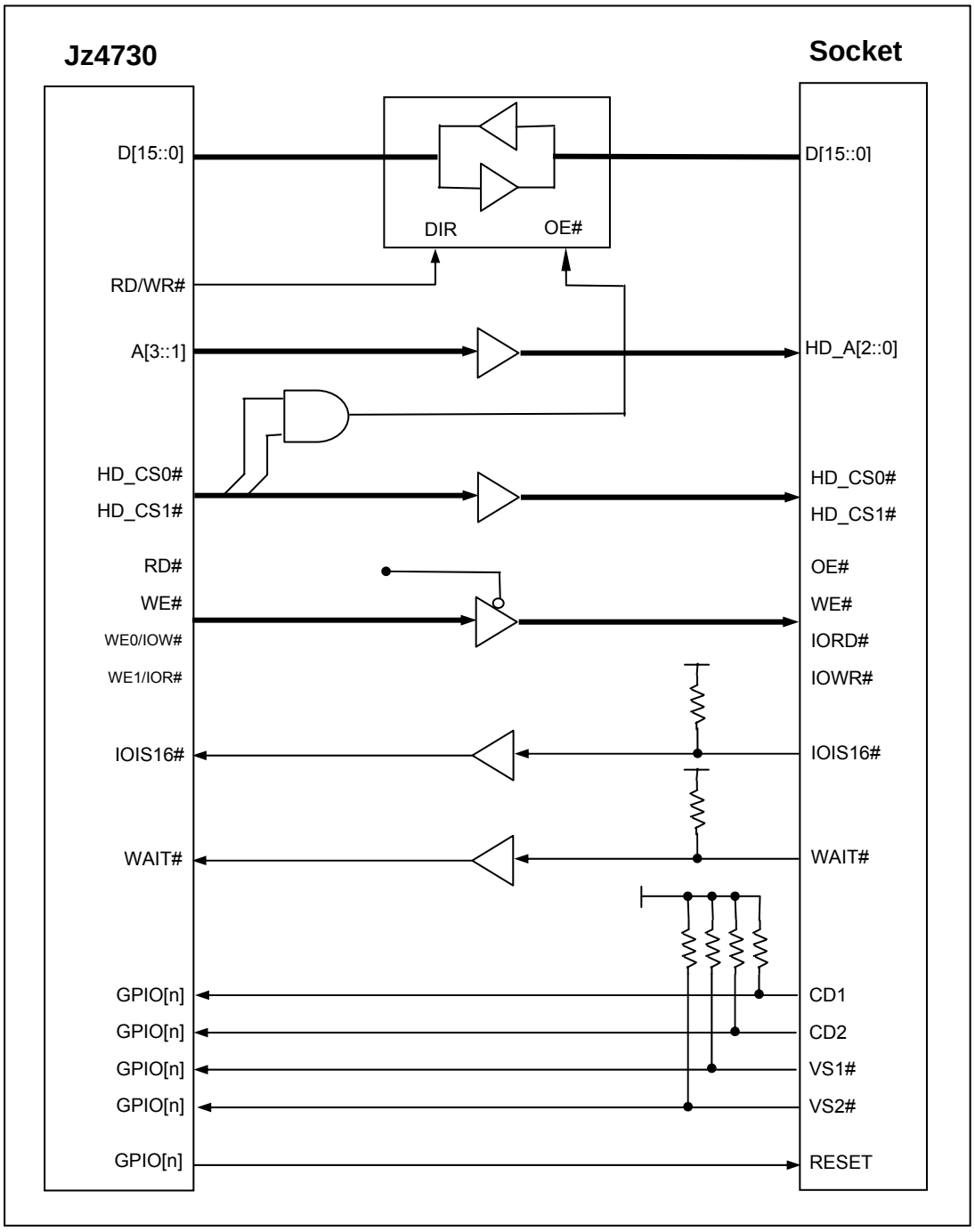



**Figure 3-4 16-bit PC Card Interconnection Example**

### 3.2.5 Support IDE PIO Mode



## 3.3 SDRAM

Following figure shows an example of connection of 1M x 16-bit x 2-bank synchronous DRAM

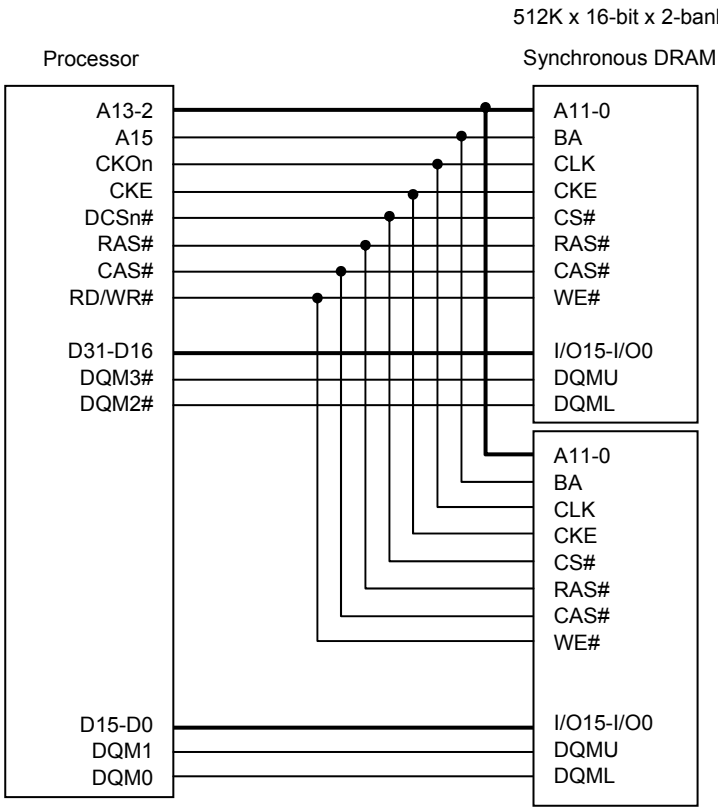



**Figure 3-5 Example of Synchronous DRAM Chip Connection (1)**

Following figure shows an example of connection of 1M x 16-bit x 4-bank synchronous DRAM.

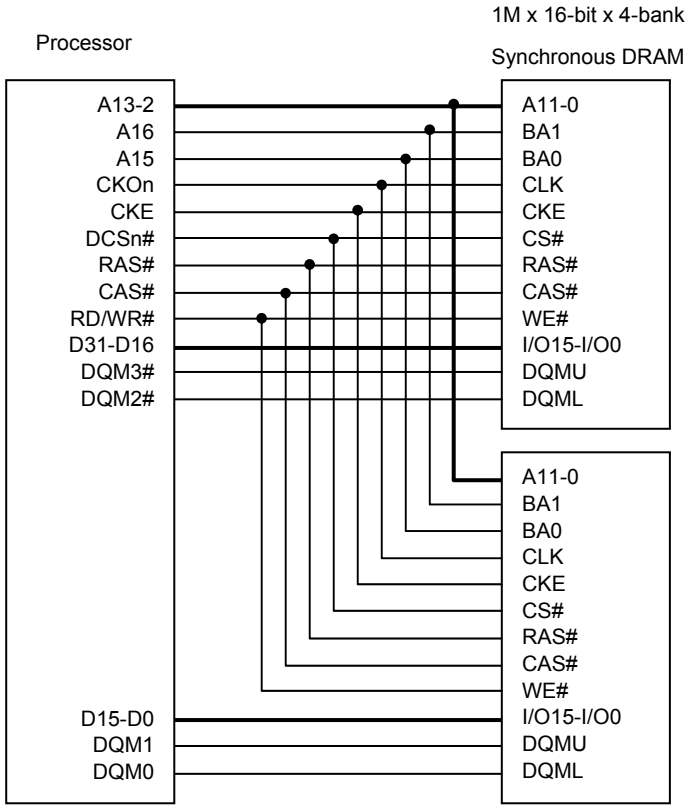



**Figure 3-6 Example of Synchronous DRAM Chip Connection (2)**

# 4 AC97/I2S Design Guidelines

The AIC(AC'97 and I2S Controller) of Jz4730 supports the Audio Codec '97 Component Specification 2.3 for AC-link format and I2S or IIS (for inter-IC sound), a protocol defined by Philips Semiconductor. Both normal I2S and the MSB-justified I2S formats are supported by AIC.

The AC-link is a synchronous, fixed-rate serial bus interface for transferring CODEC register control and status information in addition to digital audio. Where both normal I2S and MSB-justified-I2S work with a variety of clock rates, which can be obtained either by dividing the PLL clock by two programmable dividers or from an external clock source.

For I2S systems that support the L3 control bus protocol, additional pins are required to control the external CODEC. CODECs that use an L3 control bus require 3 signals: L3_CLK, L3_DATA, and L3_MODE for writing bytes into the L3 bus register. The AIC supports the L3 bus protocol via software control of the general-purpose I/O (GPIO) pins. The AIC does not provide hardware control for the L3 bus protocol.

The AC'97 interface and I2S interface can't be used at the same time, and if the AIC function is disabled, its pins may be used for GPIO functions.

## 4.1 AC97 Implementation

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots.

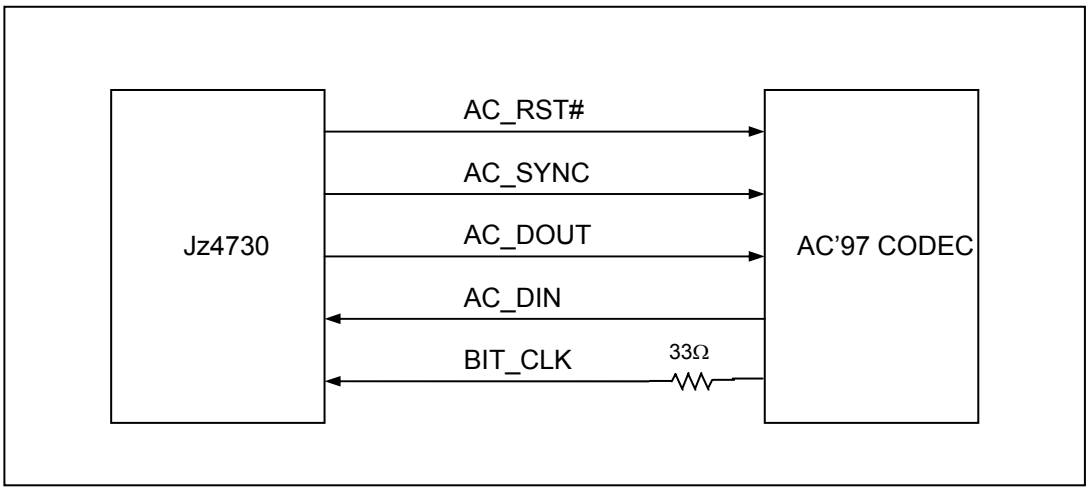



**Figure 4-1 AC-Link Interconnection**

## 4.2 I2S Implementation

The following figure shows an connection example between Jz4730 and I2S Codec. The I2S Codec is a Master device and Jz4730 is a Slave device. MCLK is the master clock input for I2S Codec.
For details please refer to the document: **AN4730_002_i2s.pdf**

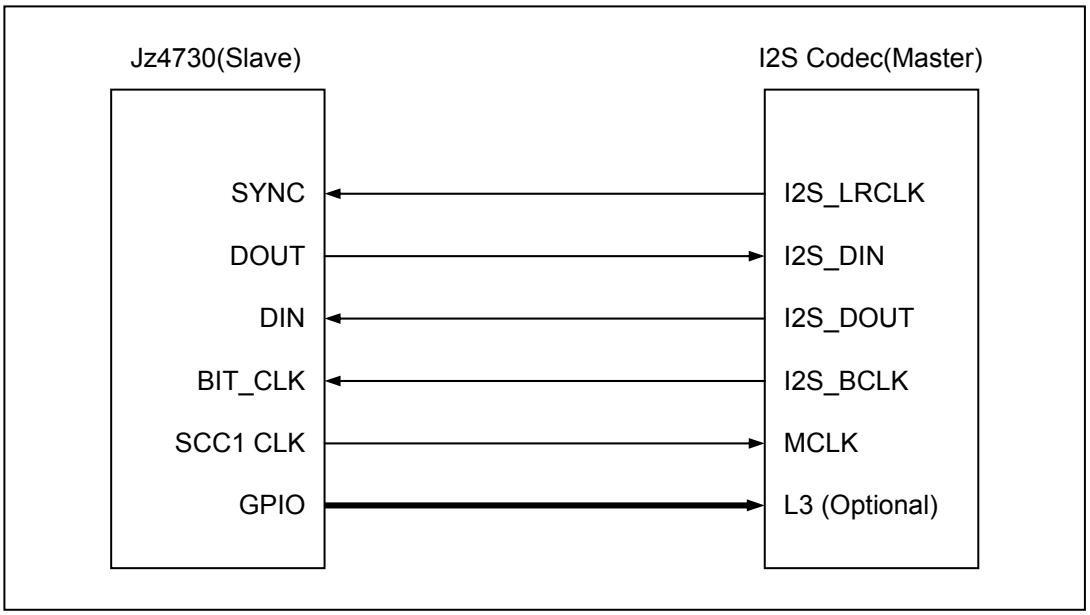



**Figure 4-2 I2S Interconnection**

## 4.3 Layout Guideline

Using the assumed 4-layer stack-up, the AC97/I2S interface can be routed using 5 mil traces with 5-mil spacing between the traces. Maximum length between Jz4730 to CODEC is 15 inches. Trace impedance should be Z0 = 60 Ω ± 15%.

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.

- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

# 5 USB Design Guidelines

Jz4730 integrates USB Host Controller (UHC), which is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.

Jz4730 also integrates USB device controller (UDC), which is USB Revision 1.1-compliant full-speed device.

**Note:**

USB device port is multiplexed with USB host port 0 and is selected by SBA_CNTL.USBCFG register.

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both D+/D- data lines.
- 15 Ω series resistors should be placed as close as possible to the Jz4730. These series resistors provide source termination of the reflected signal.
- 47-pF caps must be placed as close as possible to the Jz4730 as well as on the processor side of the series resistors on the USB data lines (D0±, D1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (D0±, D1±). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the D0± and D1± signals should be 45 Ω (to ground) for each USB signal D+ or D-. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 3-1. The impedance is 90 Ω between the differential signal pairs D+ and D-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting 45Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as ‘critical signals’. (i.e., hand-routing preferred). The D+/D- signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the D+/D- signal pair to adjacent signal traces will help to prevent cross-talk. The D+/D- signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

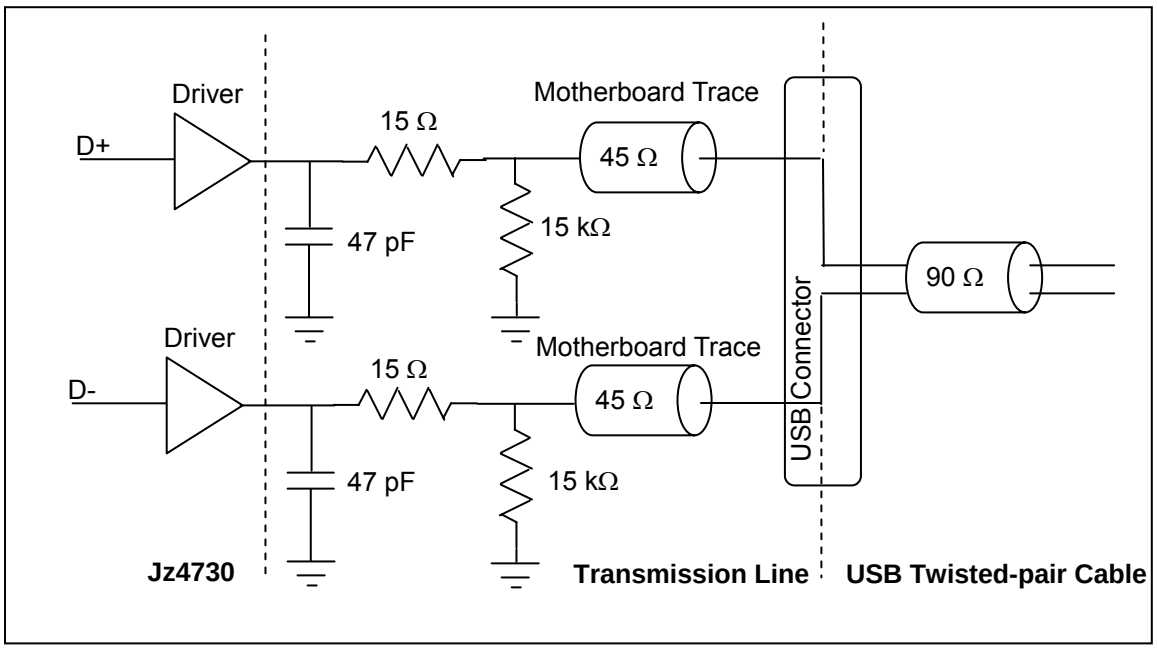



**Figure 5-1 Recommend USB Host Schematic**

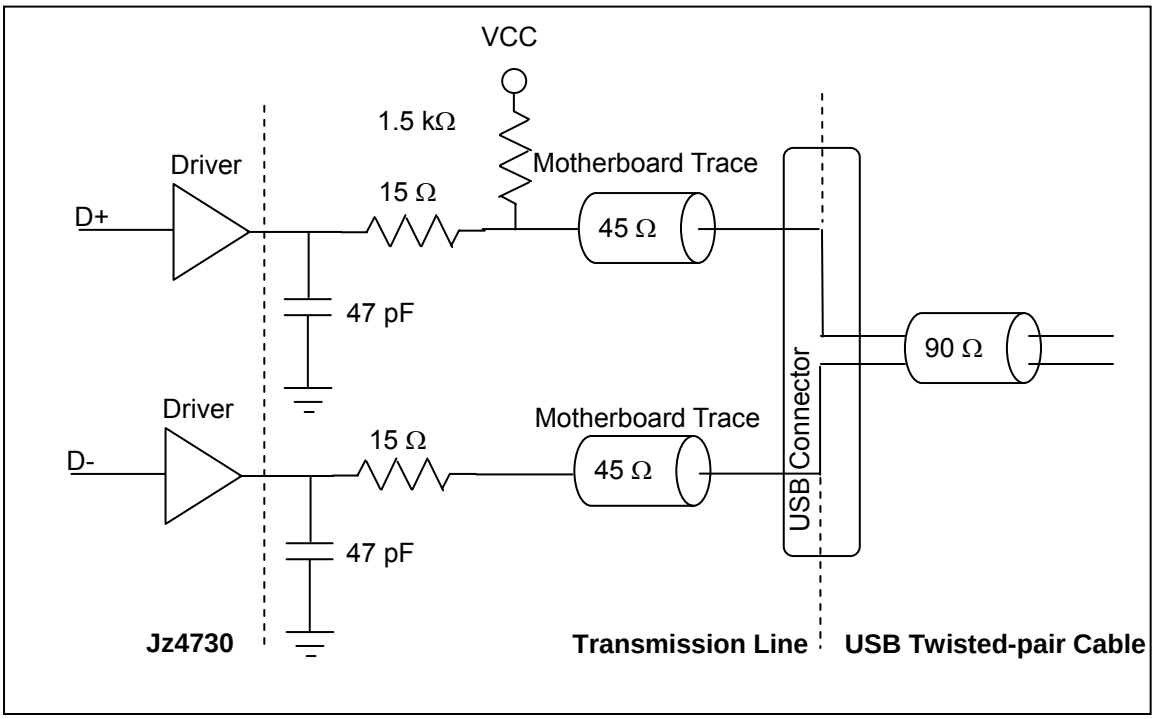



**Figure 5-2 Recommend USB Device Schematic**

# 6 LCD Design Guidelines

The Jz4730 integrated LCD controller has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller.

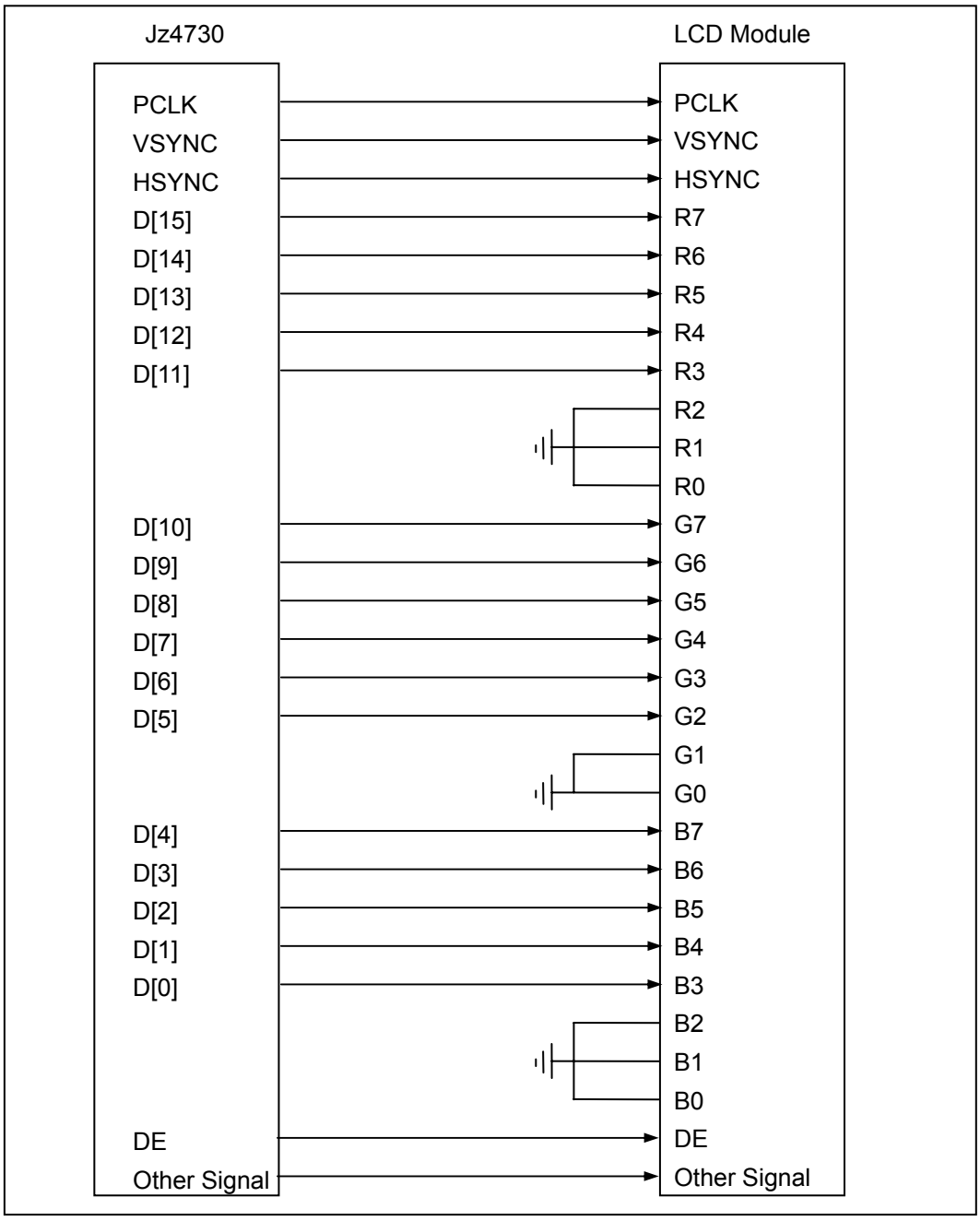



**Figure 6-1 24-bit LCD Module Connection Example**

# 7 Ethernet Design Guidelines

The Jz4730 processor contains one Ethernet media access controller (MAC) that supporting 10/100Mbps Ethernet. The MAC provides the interface between the host application and the PHY layer through the media independent interface (MII). The PHY layer device is external to the processor. This section describes design guidelines for the LAN on board based Jz4730.

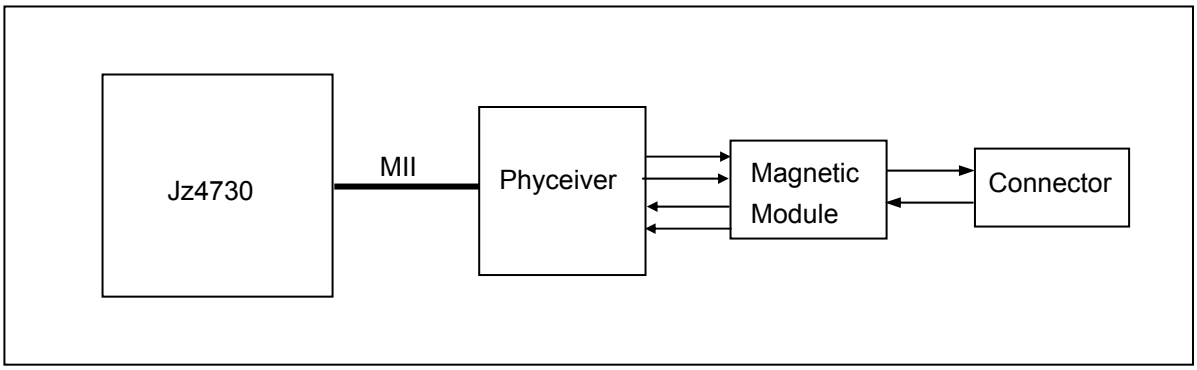



**Figure 7-1 LAN On Board Implementation**

## 7.1 Jz4730 MII Connection

Jz4730 MII interconnection example is shown as figure 7-2, the Ethernet PHY chip maybe varied for specific OEM design targets. Two source termination resistors (R1, R2) are recommended for better signal integrity for the two clock signals (MII_TXCLK and MII_RXCLK, 25MHz at 100M LAN), the value of R1 and R2 maybe 33 Ω (refer to the PHY chip datasheet) to compensate for minor the difference between the chip output and PCB trace impedance. The R1 and R2 should be placed as close as possible to the PHY chip. R3 is a 1.5K Ω pull-up resistor because the signal MII_MDIO is an open-drain pad for most phyceiver chip. Jz4730 RESETOUT_ drive the RESET# input to reset the PHY chip when power-up.

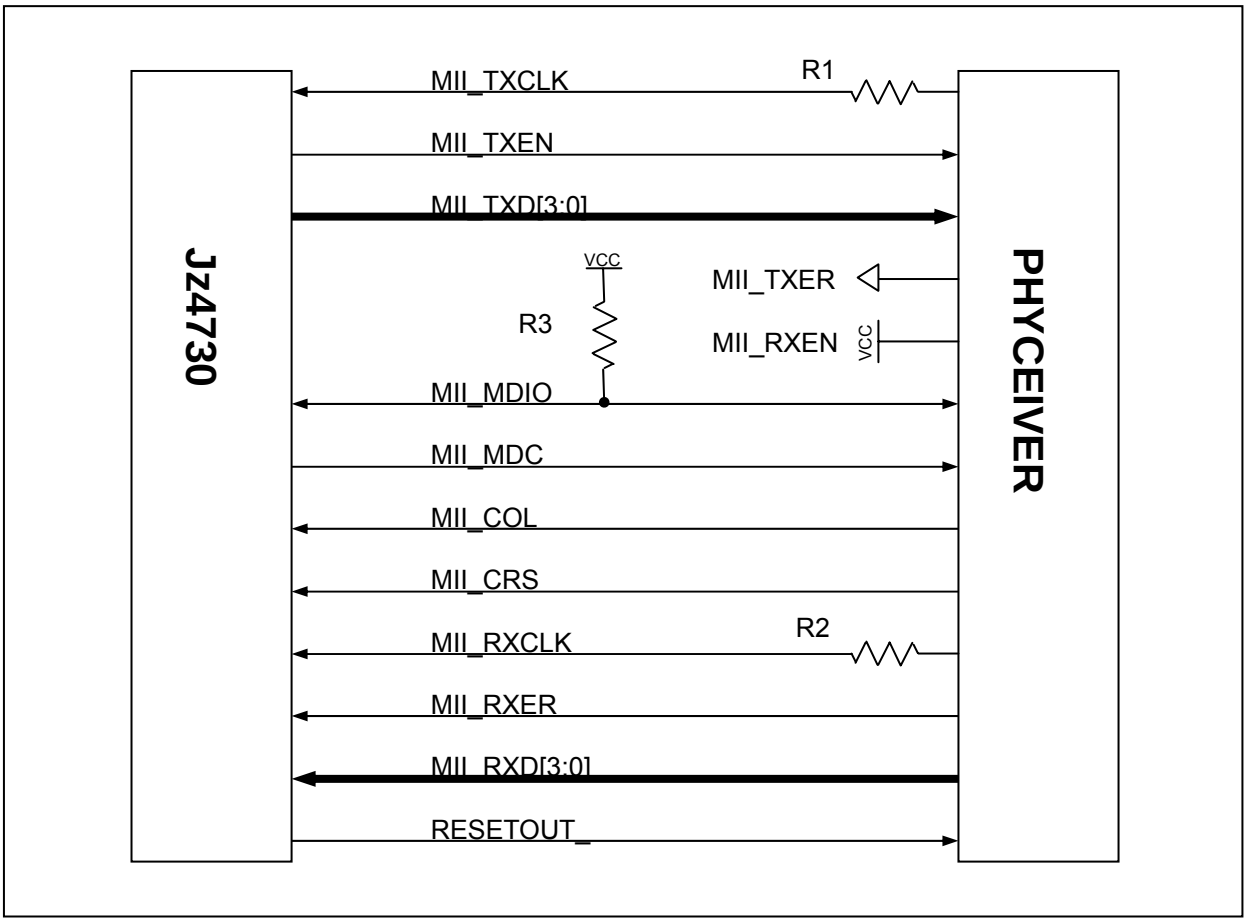



**Figure 7-2 MII Connection**

| Parameter | Routing Guidelines |
|---|---|
| Topology | Point-to-Point |
| Reference Plane | Ground Referenced |
| Nominal Trace Width, Spacing | 5 mils Width, 7 mil Spacing |
| Characteristic Trace Impedance | (Zo) 60 Ω ± 15% |
| Jz4730 Breakout Guidelines | 5 mils width with 6-mil spacing for a max of 350 mils.<br>**Note:** Use of breakout guidelines should be minimized. |
| Trace Length | Max = 8 inches |
| CLK Signals Trace Width, Spacing | 8 mils Width, 12 mil Spacing |
| Termination Resistor (R1, R2) | 10 – 100 Ω (Refer to the PHY Chip Datasheet) |
| Maximum via Count per signal | 4 vias (The number of vias over 2 should be minimized.) |
| Trace Length Match For MII_TXCLK, MII_TXD[3:0] and MII_TXEN | Each trace is either equal in length to the MII_TXCLK trace or up to 0.5 inch shorter than the MII_TXCLK trace. |
| Trace Length Match For MII_RXCLK, MII_RXD[3:0] and MII_RXER | Each trace is either equal in length to the MII_RXCLK trace or up to 0.5 inch shorter than the MII_RXCLK trace. |

# 8 Miscellaneous Peripheral Design Guidelines

## 8.1 SSI Design Guideline

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.
The following figures show the connection example:

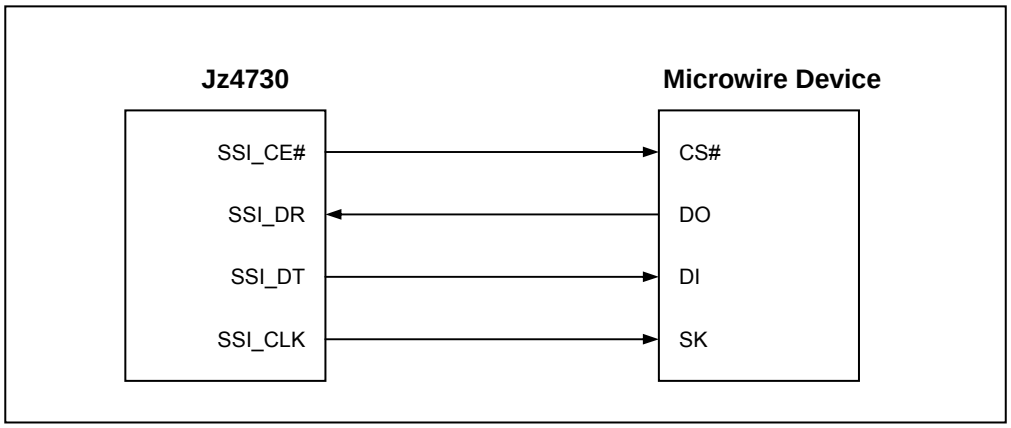



**Figure 8-1 Microwire Interconnection**

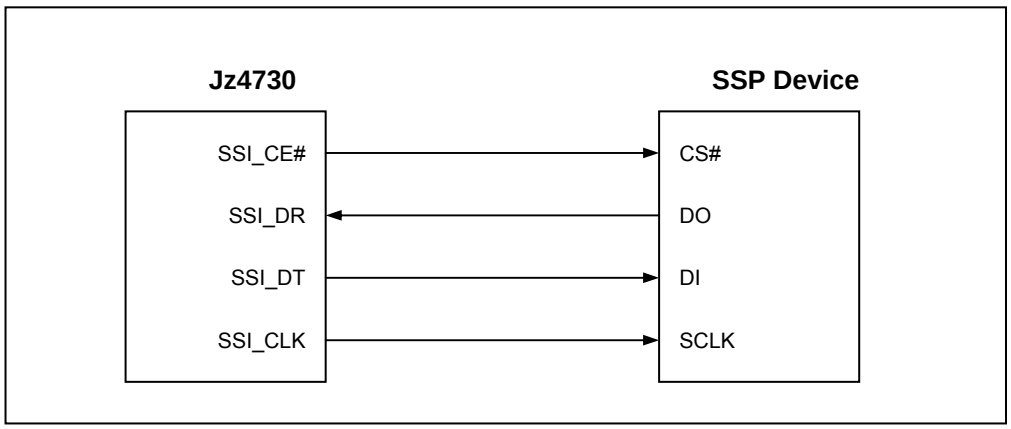



**Figure 8-2 SSP Interconnection**

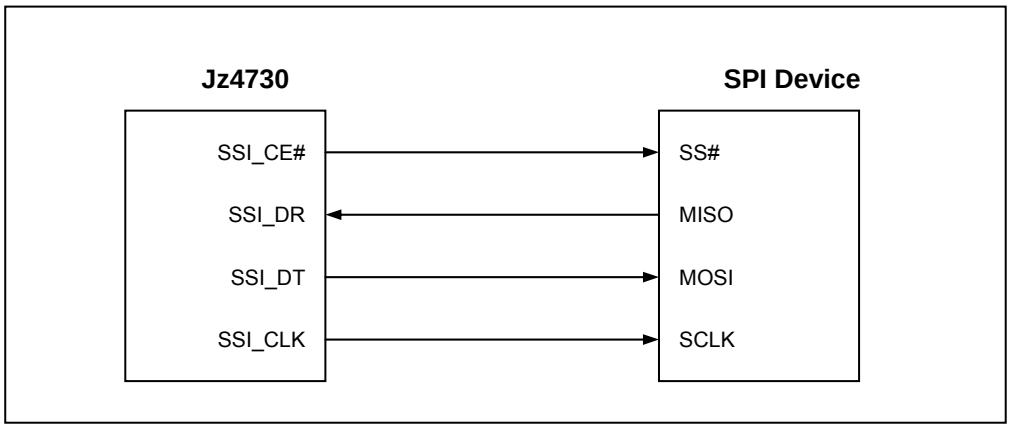



**Figure 8-3 SPI Interconnection**

## 8.2 UART/IrDA

The Jz4730 processor has four UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550 industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

### 8.2.1 UART Implementation

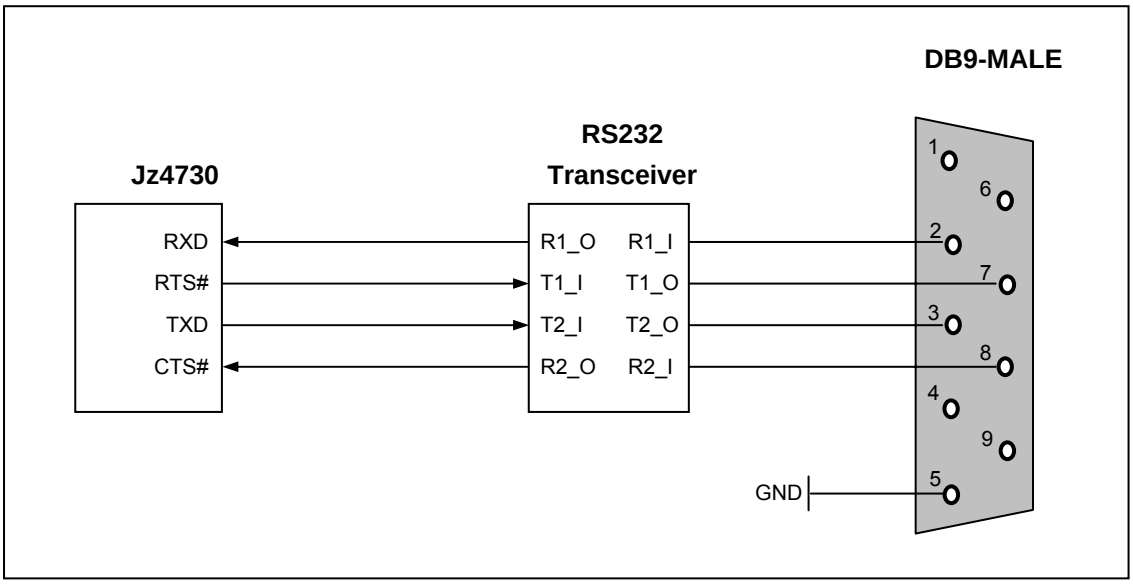



**Figure 8-4 RS232 Serial Port Interconnection**

### 8.2.2 IrDA Implementation

The Slow Infrared (SIR) interface is used with the UART to support two-way wireless communication that uses infrared transmission. The SIR provides a transmit encoder and receive decoder to support a physical link that conforms to the IrDA Serial Infrared Specification Version 1.1.

The SIR interface does not contain the actual IR LED driver or the receiver amplifier. The I/O pins attached to the SIR only have digital CMOS level signals. The SIR supports two-way communication, but full duplex communication is not possible because reflections from the transmit LED enter the receiver. The SIR interface supports frequencies up to 115.2 kbps.

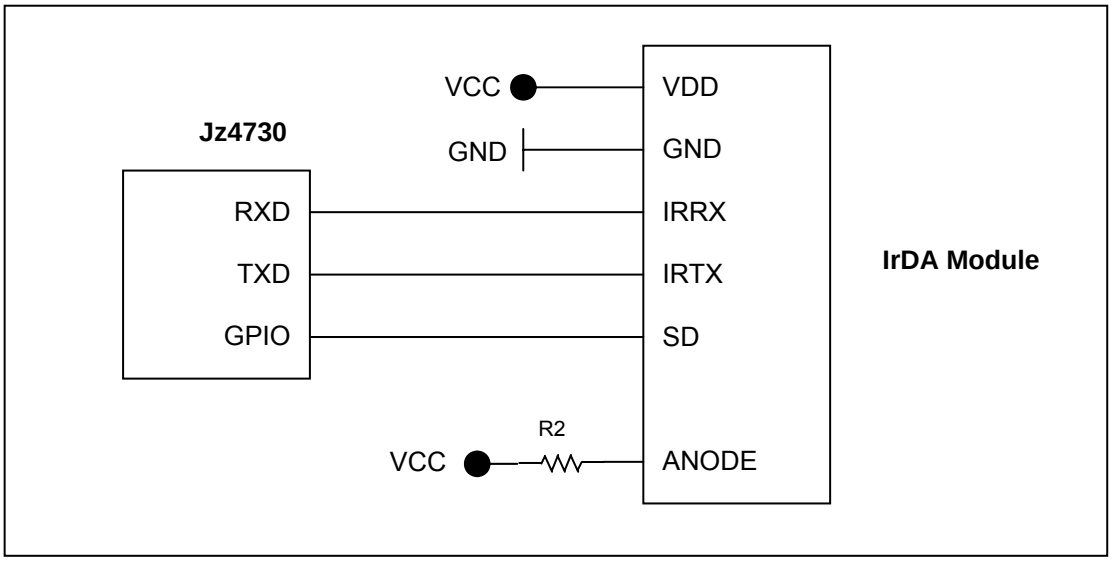



**Figure 8-5 IrDA Port Interconnection**

## 8.3 I2C Bus

The I2C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I2C bus. The I2C bus requires a minimum amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

Jz4730 support single master mode only, so only slave devices are supported on the I2C bus attached to Jz4730. The I2C module supports I²C standard-mode and F/S-mode up to 400 kHz. The interface example is shown as following figure. The I2C bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up is required on SCL and SDA. Refer to The I2C-Bus Specification for complete details on I2C bus operation.

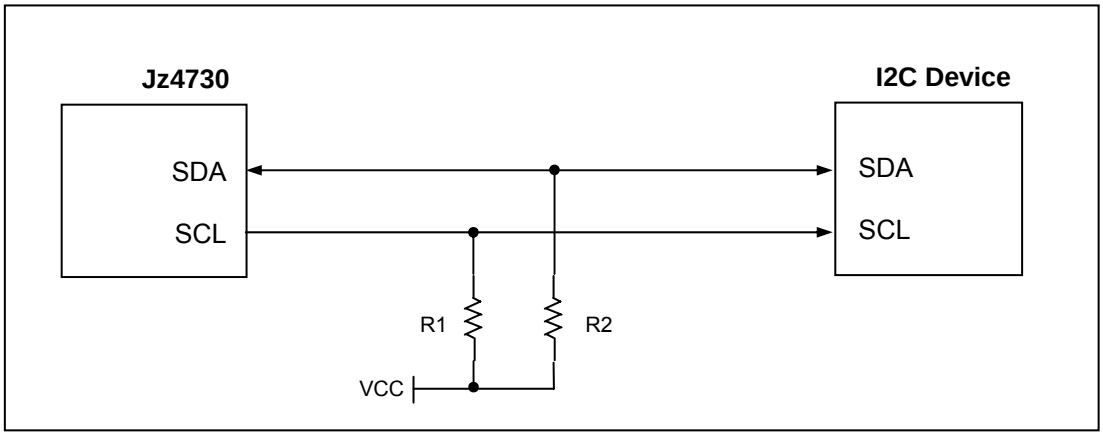



**Figure 8-6 I2C Interconnection**

## 8.4 PWM

The Pulse Width Modulator (PWM) is used to control the back light inverter or adjust bright or contrast of LCD panel and also can be used to generate tone. PWM consists of a simple free-running counter with two compared registers, each compare register performs a particular task when it matches the count value. The period comparator causes the output pin to be set and the free-running counter to reset when it matches the period value. The width comparator causes the output pin to reset when the counter value matches. Jz4730 contains two pulse width modulators: PWM0 and PWM1.

## 8.5 GPIO

The Jz4730 processor provides 120 multiplexed General Purpose I/O (GPIO) pins for use in generating and capturing application-specific input and output signals. Each pin can be programmed as an output, an input or function pin that serves certain peripheral. As input, pull up/down can be enabled/disabled for the pin and the pin also can be configured as level or edge tripped interrupt source.

### Note:

If a GPIO is used as a wakeup source of HIBERNATE mode, it must be configured as an input in the GPIO Controller and either rising edge or falling edge must be selected in the HRER or HFER. Only GPIO16, 17, 21, 23 and GPIO96~103 can be used to wakeup HIBERNATE mode.

## 8.6 Smart-Card

Smart Card Controller (SCC) interface is a primary device and communications interface for kinds of IC cards. The SCC interface supports communication with smart cards as specified in standard ISO7816-3. There are two SCC interfaces integrated in Jz4730.

The following is a example of smart-card implementation.

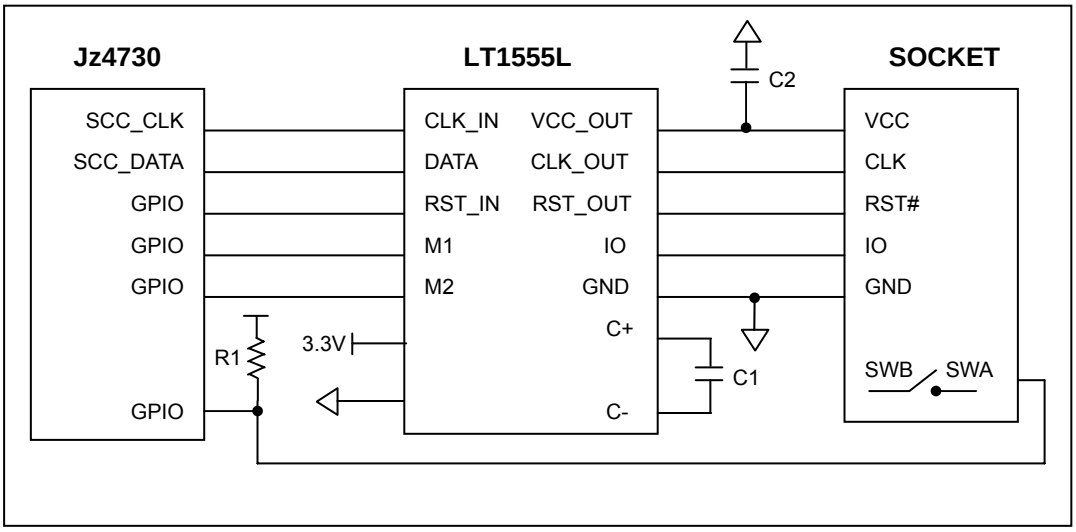
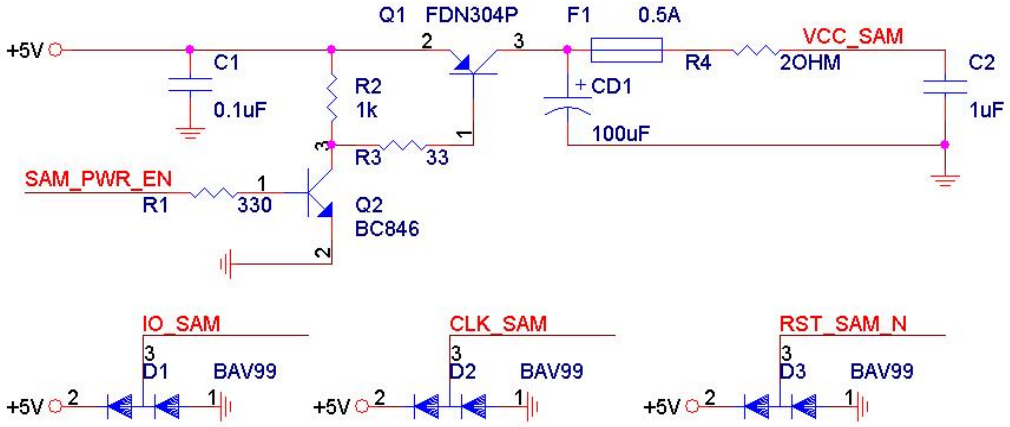



**Figure 8-7 Smart Card implementation**

The Linear Technology® LTC1555L provides power conversion and level shifting needed for smart card. Please refer to the manufacturer data-sheet for detail information of LTC1555L. You can use the discrete component to realize the function as LTC1555L for cost down.

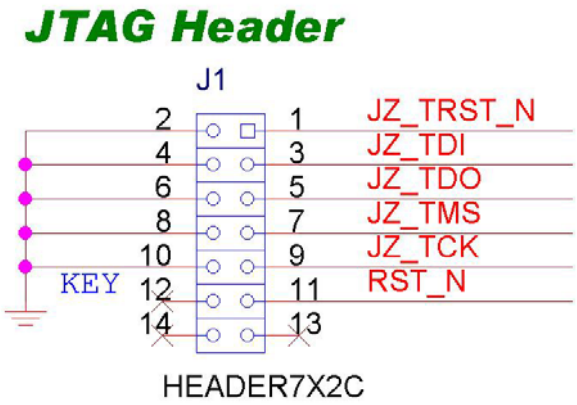



## 8.7 RTC

The Jz4730 must use a external RTC chip to get the Real Time Clock. The Jz4730 can communicate with RTC chip through I2C Bus. The Jz4730 has a RTC clock input pin, if the system need to work in HIBERNATE mode, a external RTC clock should be connected to this pin. Usually the RTC chip has a RTC clock output pin.

## 8.8 JTAG/Debug Port

Jz4730 has a built-in JTAG/Debug port. All JTAG pins are directly connected. The following figure shows the connection of the JTAG port. Pin 11 RST_N should be connected to system reset circuit. Pin 12 is a KEY. The header should be a 7X2(2.54mm Pitch) male header with coat.



# 9 Platform Clock Guidelines

The Jz4730 processor contains one PLL driven by the 12-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- SDRAM bus clock
- Programmable clocks needed by certain peripherals

If the system need to work in HIBERNATE mode, a external RTC clock should be provided.

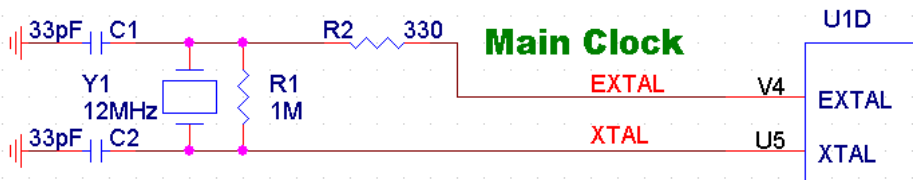
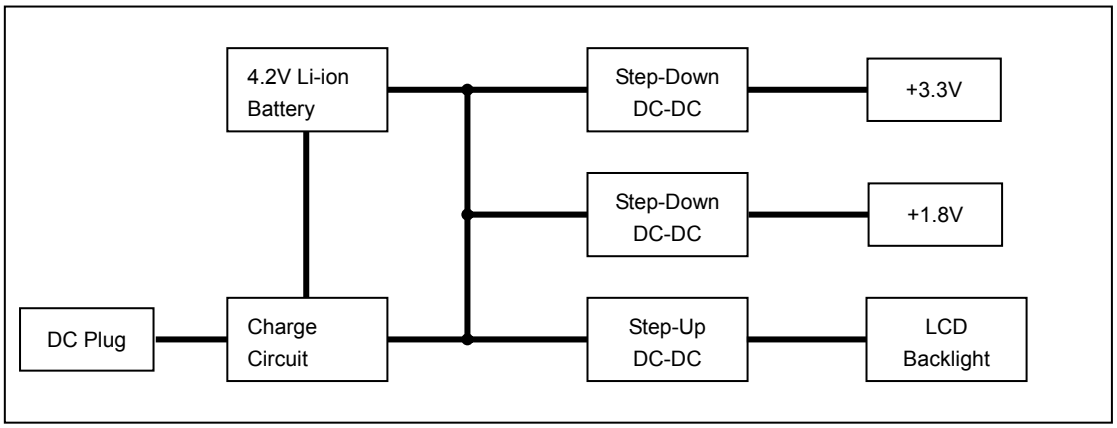



**Table 9-1 Main Clock routing Summary**

| Trace Impedance | Mail Clock Routing Requirements | Maximum Trace Length To Crystal | Signal Length Matching | R1, R2, C1, and C2 Tolerances | Signal Referencing |
|---|---|---|---|---|---|
| 45 Ω to 69 Ω, 60 Ω Target | 5 mil trace width (results in ~2pF per inch) | 1 inch | NA | R1 = 1M. ± 5%<br>R2 = 330 ± 5%<br>C1=C2=33pF±10% (Typical)<br>(NPO class)<br>The capacitance value of C1 and C2 should be referred to the crystal's specification | Ground |

# 10 Platform Power Guidelines

The Jz4730 processor needs two voltages: +3.3V for I/O and +1.8V for core. The following figure is a typical power circuit in the PMP application.

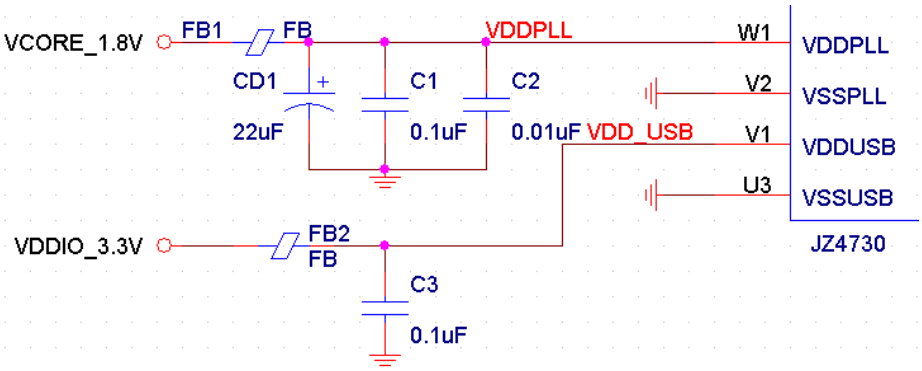



## 10.1 Digital Power Delivery and Decoupling

The VDDIO and VCORE of Jz4730 should be decoupled with 0.1uF capacitor.

## 10.2 Analog Power Delivery Decoupling

The VDDPLL and VDDUSB of Jz4730 are analog power, we advise user to design as the following circuit.




The C1 ,C2 and C3 should be placed near the Pin of power. The trace from capacitor to the Pin should be width.