Ingenic® RD4730_PMP Reference Design

Hardware Manual

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Release history

Date	Revision	Change
Apr. 2006	1.0	First release

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Content

1 Overview

Jz4730 is a multimedia application processor, which has a very high performance and low power 32-bit RISC engine. Jz4730 integrates various peripherals for embedded application, such as memory controller, USB1.1 host and device interface, Ethernet interface, LCD controller, AC'97/I2S interface, CMOS sensor interface, MMC/SD controller, SSI interface, I2C interface, UART, IrDA, GPIO, and so on.

The RD4730_PMP is a reference design with Jz4730 addressing to consumer electronic equipment, that help engineer to quickly develop their own products in hardware and software. This design also provides flexible interface to extend other module.

With this reference design, there have richness development package include supporting WinCE™, CE-Linux™, and RTOS

1.1 Functions of RD4730_PMP

- High-performance processor Jz4730 running up to 400MHz, support CE-Linux and Windows CE。
- SDRAM: HY57561620-ECHT X 2 ，64MB。
- FLASH: NOR FLASH 2MB–8MB（optional），NAND FLASH K9F1G08 128MB
- LCD: 480X272 4inch TFT，touch panel is optional。
- Multimedia: AC'97 interface with UCB1400，support MP3/MP4 player, MP4 decoder support 320X240 30f/s；stereo record with gain control; stereo line/headphone output with bass/treble control.
- CMOS sensor interface: 0.3 – 4 Mega Pixel.
- 5 key, can provide sound-button and soft power on/off; 8X8 keypad interface.
- USB1.1 Host / Device interface.
- 2-UART: support GPS+GSM module extension.
- MMC/SD extend interface: 256MB-2GB.
- Backlight control with PWM.
- Power on by RTC timer.
- Advanced power manager: Lithium-Ion battery charge; two low power mode of CPU sleep and power off; quickly system power up in 1 minute; support RTC alarm and power up; very low power consumption: less than 200MA in normal condition, Max. 350MA, and <=1MA in standby mode; battery charging status indicator, and battery voltage monitor; auto in sleep mode when no operation.

1.2 RD4730_PMP System Architecture

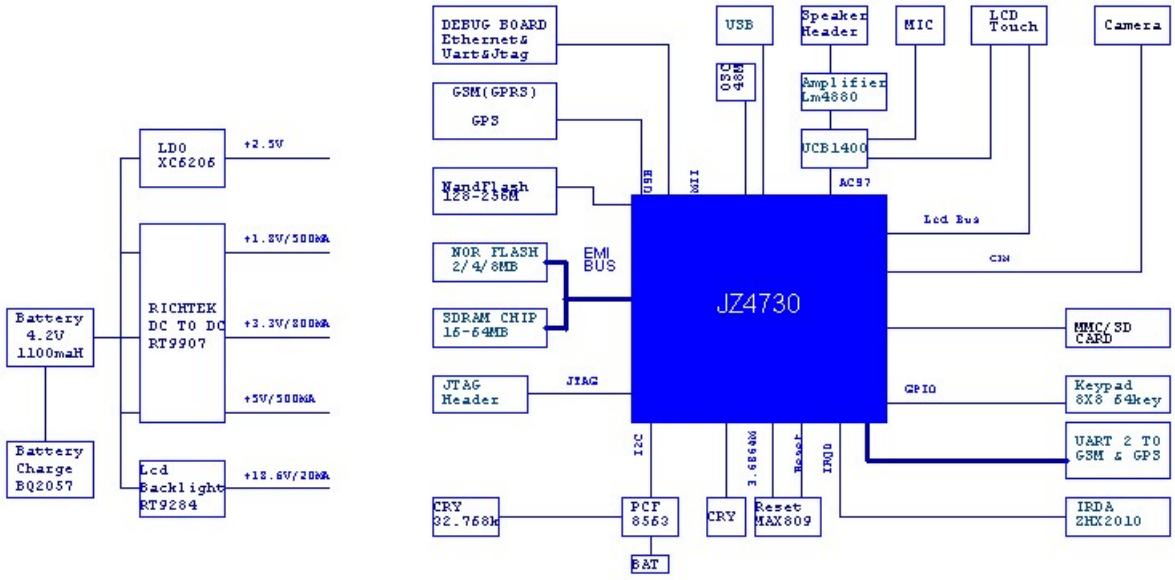

Figure 1-1 RD4730_PMP System Architecture

2 Hardware Description

In this section, will describe every hardware module of this design, please refer to the user's manual of Jz4730 first. For the others components, please refer to associated datasheet. For the details of the design, please refer to the schematic design.

2.1 RD4730_PMP Layout

Figure 2-1shows the layout of main components and connectors。

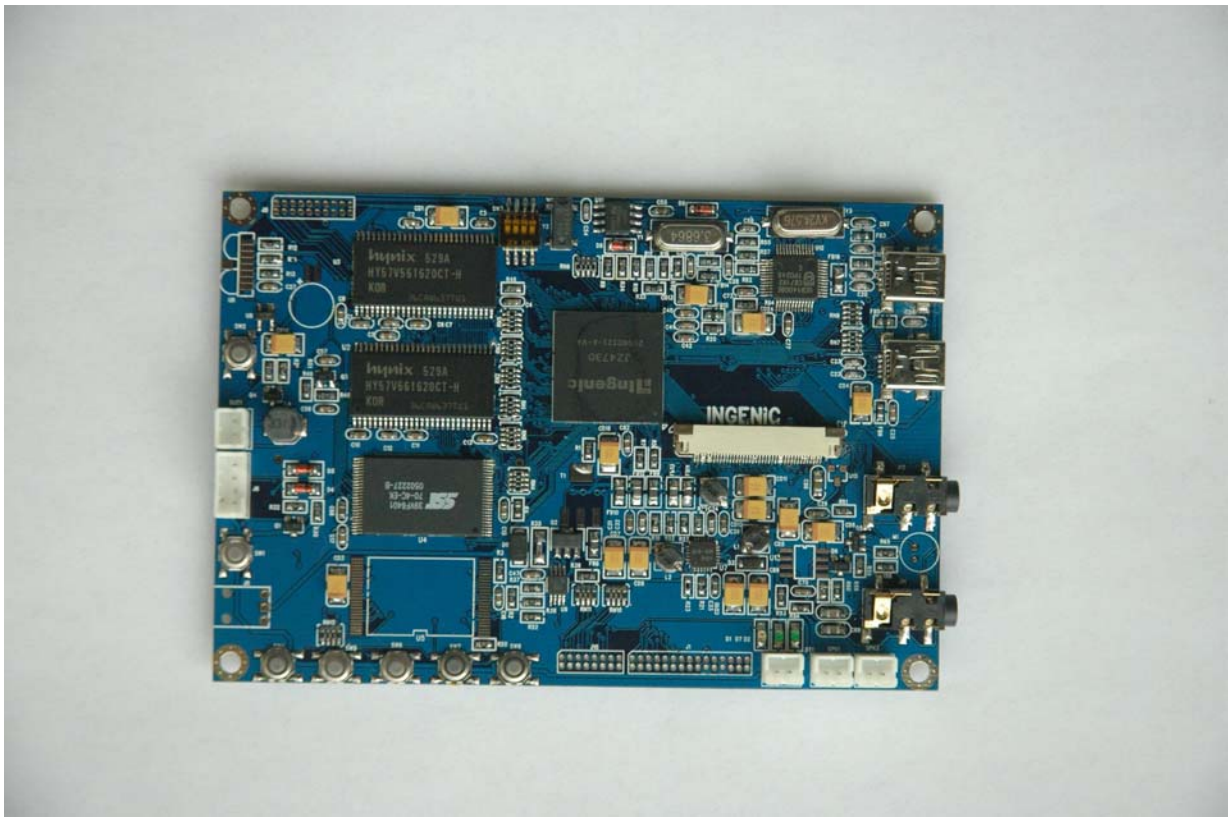

Figure 2-1 RD4730_PMP Layout

2.2 Power

The RD4730_PMP board is powered by 3.7V Lithium-Ion battery, via header BT1. The button SW1, is power on/off switch. When in power off status, push SW1 will power on the board and the CPU should output 1 on PW_O port immediately in order to keep the power. When the system is running, push

SW1 will assert a interrupt to CPU, then the software can clear PW_O to power off the board after associated processing.

The main power chip is U7 – RT9907, provides +5V, +3.3V, and +1.8V power supply. And the LED D1 indicates the status of +3.3V power.

The LCD backlight power is generated by U14 – RT9284, can provide about 20.8MA current. And U15 – XC6206 provides +2.5V power for LCD.

J8 is the external power supply jack, should connect with 6-7V 1A DC power adapter, together for battery charge. LED D7 indicates the charge status that light when charging, and inform to CPU via GPIO125 (can assert interrupt). The charge current is 550MA.

This board also can be powered with USB device port when connect to PC, and charge the battery together.

In this design there has a RTC chip U10 (PCF8563) powered by the coin cell battery B1, provides precision real time for system. When the system is in power off, it can provide time switch on the system via Q1.

2.3 System Reset

U8 (MIC811) makes up of the hardware reset circuit, provides system reset signal to all components when power on. SW2 is the manual reset button. And LED D2 can be used as status indicator when system software is running, that it connect to GPIO92.

2.4 Bootstrap

There has two modes of bootstrap in this design:

- Bootstrap from NOR Flash U4。
- Bootstrap from NAND Flash U5 /U11。

When boot from NAND Flash, it can be from U5 or SMC U11. That U5, U1have the same address NAND flash.

In this design, SW1 sets the bootstrap mode. When boot from U4, the setting of SW1 should be:

Table 2-1 BOOT SETUP （SW3 ON=1）

B_SEL0	**SW1.2**	1

B_SEL1	**SW1.3**	0
B_SEL2	**SW1.4**	0
B_SEL3	**SW1.1**	Boot select input 3: 0->boot from ROM at CS0;1->boot from NAND flash device at CS3

Table 2-2 describes the setting of SW1 when boot from NAND Flash.

Table 2-2 BOOT SETUP （SW3 ON=1）

B_SEL0	**SW1.2**	Boot select input 0: NAND flash width when boot from it,0->8bit;1->16bit
B_SEL1	**SW1.3**	Boot_select input 1: NAND flash page size when boot from it, 0->512B;1->2048B
B_SEL2	**SW1.4**	Boot select input 2: NAND flash address cycles when boot from it,0->low cycle;1->high cycle
B_SEL3	**SW1.1**	Boot select input 3: 0->boot from ROM at CS0;1->boot from NAND flash device at CS3

For details about boot select setting, please refer to the Jz4730 Hardware Manual.

2.5 SDRAM

This board has 64MB SDRAM, consist of two chips – U2 and U3, 4Banks X 4M X 16Bit.

2.6 LCD Interface

J13 is the LCD interface, that can directly connect to SAMSUNG™ LTP400WQ-F01 LCD panel. Or extend to connect to other LCD panel. Table 2-2 lists the signals definition of J13.

Table 2-3 LCD Interface（J13）Signals Definition

Pin Number	Signal	Pin Number	Signal
1	GND	2	GND
3	+2.5V	4	+2.5V
5	GND	6	GND
7	GND	8	LCD_D11
9	LCD_DD12	10	LCD_DD13
11	LCD_DD14	12	LCD_DD15
13	GND	14	GND
15	LCD_DD5	16	LCD_DD6
17	LCD_DD7	18	LCD_DD8
19	LCD_DD9	20	LCD_DD10

21	GND	22	GND
23	GND	24	LCD_DD0
25	LCD_D1	26	LCD_D2
27	LCD_D3	28	LCD_D4
29	GND	30	LCD_PCLK
31	DISP_OFF_N	32	LCD_HSYNC
33	LCD_VSYNC	34	LCD_DE
35	+5V	36	+5V
37	GND	38	GND
39	VLED-	40	VLED+

In JP15, there has some special control signals for some LCD panel: 1-LCD_SPL; 2-LCD_CLS; 3-LCD_PS; 4-LCD_REV. For details please refer to Jz4730 User's Manual.

2.7 USB Interface

There has one USB 1.1 host port J4, one USB 1.1 device port J3. The source of USB clock (48MHz) can be external on board, or internal in Jz4730.

2.8 Audio System

The audio system of this design, consist of AC'97 audio Codec U12 (UCB1400), MIC-in jack J12, and output/headphone jack J11. There has two amplifier for external speaker connecting to the header SPK1 and SPK2. When plug a headphone in J11, the amplifier will be off.

The output volume, bass/treble boost and,
The audio system provides stereo record with gain control; stereo line/headphone output with bass/treble boost, and output volume control by software.

2.9 Camera Interface

J16 is the CMOS sensor interface which directly connect with OV7649 module. Support maximum 400 Mega Pixel (2048X2048) camera module.

The signals of this interface are defined as below:

Table 2-4 Camera Interface（J16）Signals Definition

Pin Number	Signal	Pin Number	Signal
1	GND	2	CIM_HSYNC

3	CIM_VSYNC	4	PWDN
5	CIM_PCLK	6	+2.5V
7	+3.3V	8	I2C_SDA
9	CLK_24MHz_CAM	10	I2C_SCK
11	CIM_D0	12	CIM_D1
13	CIM_D2	14	CIM_D3
15	GND	16	CIM_D4
17	CIM_D5	18	CIM_D6
19	CIM_D7	20	RESET

2.10 GSM+GPS Extension

In this design, there has a socket J5 for GSM and GPS module extension, that include: two UART port – 0 and 3; audio in/out port; GSM control signals.

Table 2-5 J5 Signals Definition

Pin Number	Signal	GPIO Number
1	TXD0	
2	RXD0	
3	TXD3	
4	RXD3	
5	CTS3	
6	RTS3	
7	GSM_BOOT	GPIO72
8	GSM_RESET	GPIO73
9	GSM_EN	GPIO74
10	GSM_RING	GPIO75
11	GND	
12	MIC_GSM_IN	
13	AGC_GND	
14	IO_3.3V	
15	GND	
16	GND	
17	BAT_V	
18	BAT_V	
19	AC97LINE_IN	
20	+5V	

2.11 IrDA

RD4730_PMP provides a IrDA transceiver U6, that can communication with SIR device, support maximum 4Mbps. And the UART 1 of Jz4730 can not be used in this design, since it has been set to IrDA mode.

2.12 Keypad Interface

There has a 8X8 matrix keypad interface J10, can connect a keypad as input device. GPIO98 – GPIO103, GPIO64 and GPIO76 are defined as input with pull-up. GPIO105 – GPIO111 are defined as output controlled by software. For details, please refer to the table below.

Table 2-6 J5 Signals Definition

Pin No.	Signal	GPIO No.	Pin No.	Signal	GPIO No.
1	Keyin1	GPIO76	2	Keyin2	GPIO64
3	Keyin3	GPIO98	4	Keyin4	GPIO99
5	Keyin5	GPIO100	6	Keyin6	GPIO101
7	Keyin7	GPIO102	8	Keyin8	GPIO103
9	Keyout1	GPIO104	10	Keyout2	GPIO105
11	Keyout3	GPIO106	12	Keyout4	GPIO107
13	Keyout5	GPIO108	14	Keyout6	GPIO109
15	Keyout7	GPIO110	16	Keyout8	GPIO111

When push a key, the driver can make a sound through the signal PWM1 (with 2KHz) driving the buzzer BUZ1. You can adjust the frequency of PWM1 to make it euphonious.

GPIO27, GPIO65, GPIO67, GPIO88, and GPIO89 have been pulled-up，used as normal key input. Marked as SW4 – SW8 in the design.

RD4730_PMP also support PS/2 keyboard though header J6.

2.13 MMC/SD Card

J9 is the MMC/SD card socket for extension memory, supports 32MB – 2GB MMC or SD card.

2.14 LCD Backlight

By adjusting the PWM0 signal duty cycle, make the dimming control of LCD backlight consecutively and easily.

2.15 Debug Board Interface（RD4730_PMP_DEBUG）

In order to make the system debugging facility, there has a debug board – RD4730_PMP_DEBUG, connecting to the main board through head J1. It provides JTAG port – J3, UART3 port (DB9, RS-232) – J4, and Ethernet port (RJ45) – J2.

2.16 System Status LED

There has three LED for system status indicator:

- LED D1 indicates the power status
- LED D2 connects to GPIO92, that controlled by software for system status
- LED D7 indicates the charge status that light when charging.

3 Quick Start of RD4730_PMP

When you get the RD4730_PMP board, it has been initialized with U-Boot, CELinux kernel and file system on the main board and SD card. Before power on the board, you should do the following step:

- Connecting the debug board – RD4730_PMP_DEBUG
- Connecting serial port – UART3 to a host PC as console（J6 on debug board），the configuration is 115200-8N1
- Connecting to your LAN
- Connecting a USB mouse to J4
- Connecting a battery to BT1, or use external DC power (6V, 1A)

Three manual have been used as:

- SW1: system power on/off and wakeup manual. Pushing it will switch on the board, long pushing will switch off then. When in sleep mode, pushing it will wake up the system.
- SW2: system reset manual.
- SW8: dimming control manual of LCD backlight.

After power on the board, there will be output on the console via serial port and LCD panel. After a moment, the demo of a QTOPIA application will be launched, letting you into a rich and colorful multimedia world.