Ingenic® Libra Development Board for Jz4730

Hardware Guide

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Ingenic Libra Development Board for Jz4730

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Release history

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Content

1 Overview

Libra is the development platform for the Multimedia Applications Processor Jz4730. It provides access to all of the Jz4730 native functions, and is flexible to extend. Libra can be used as a prototype for Jz4730 based design via proper extension, which can reduce the hardware and software development risk and the time-to-market greatly.

Jz4730 is a Multimedia Applications Processor designed by INGENIC®, which addresses the Mobile, Multimedia, Low power requirement electronic product. Jz4730 integrates a high performance 32-bits CPU, support many Embedded Operating Systems such as Linux™, WinCE™, etc. It also integrates SDRAM memory controller, MAC, LCD controller, AC'97/I2S controller, Camera controller, SCC, SD/MMC, I2C, USB1.1 Host/Device, four UARTs, IrDA, GPIO and so on.

1.1 Hardware Feature

- On board Jz4730.
- On board two SDRAM chips support maximum 128M Bytes. Default is 64M Bytes.
- On board 16M Bytes NOR Intel Flash Memory on board.
- Supports more than 2G Bytes NAND Flash Memory on board. Default is 16M Bytes.
- One DIP32 socket support 8-bit Boot ROM/Flash and DOC.
- I^2C EEPROM for system information and MAC ID (SPC).
- One RTC chip (PCF8563) supplies 32.768kHz clock.
- On board one 10/100M RJ45 Ethernet Port.
- On board two USB1.1 Host ports, one USB1.1 Device port is multiplexed with the first Host port.
- On board one LCD connector, supports kinds of STN and TFT LCD panel.
- On board camera interface FPC connector.
- On Board two audio CODEC, one is AC97, another is I2S, can only enable one of them at the same time. Board supplies MIC IN and Headphone OUT jacks.
- On board one ISO7816 socket for IC card and one for SIM Card.
- Four RS232 serial ports are from Jz4730 directly.
- On board one infrared (IrDA) port is multiplexed with UART1.
- On board one PS2 Keyboard port.
- One 8x8 keypad connector.
- On board one JTAG Port.
- One expansion slot (EMI bus and peripherals signal) for custom extension.
- Two 7-segment LED digits and four discrete LED diode indicators.
- One SD/MMC Card socket (optional).
- One PCMCIA socket for PC Card (16-bit) device (optional).
- Four Mictor38 Logic analyzer test pods (optional).

Libra supplies full SDK and CE-Linux™ operating system. The system can quickly boot and has better reliability.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

1.2 System Architecture

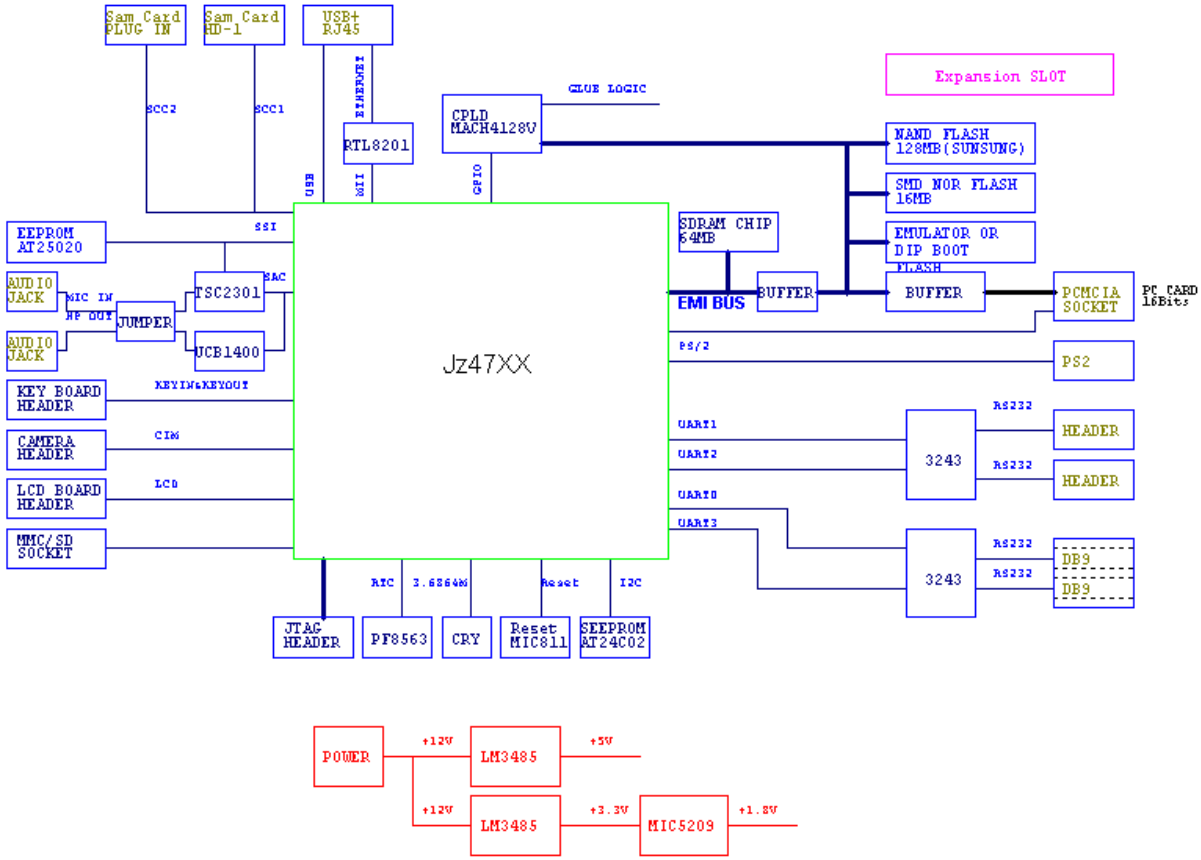


Figure 1-1 Libra System Architecture

2 Hardware Description

This chart describes the Libra development platform hardware, using this platform effectively requires a sound knowledge of the INGENIC® Jz4730 microprocessor. The other chips of the design require detail reference the manufacture's data sheet. If you want to know the detail of Libra, please reference the schematics of Libra.

2.1 Development Platform Components Location Diagram

Figure 2-1 shows the baseboard layout and major components location.

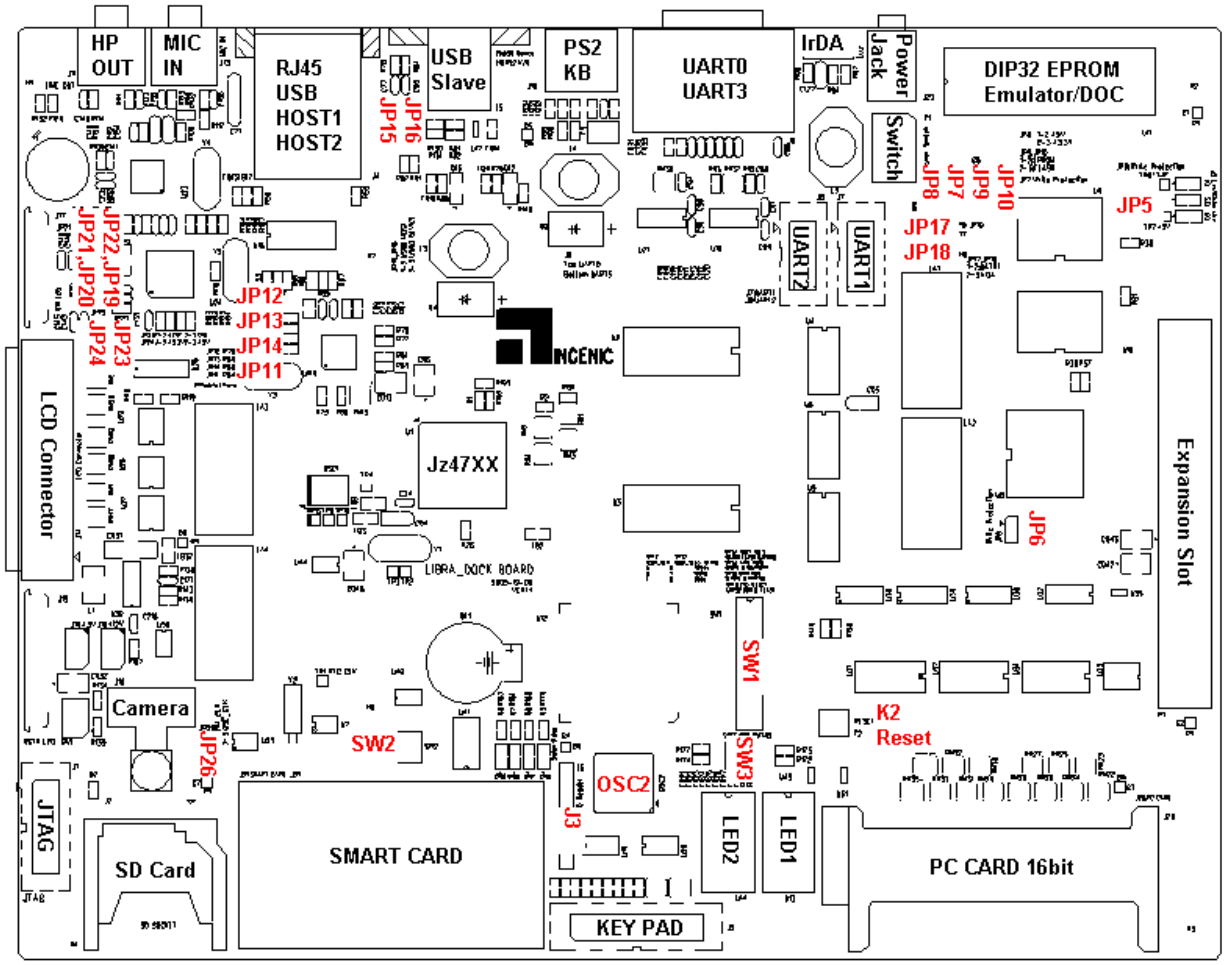


Figure 2-1 Development Platform Components Location Diagram

2.2 Power Supply and Regulation

The Libra development platform uses a +12V DC power supply, provides over current protection through a 1.5A self-recover fuse. The switch K1 turns power to the board on and off.

The Libra uses LM3485 (Switch Regulator) to generate the +5V, +3.3V. Red LED D1 and D2 indicate the power (+3.3V and +5V) on.

The Libra uses MIC5209 to generate core power supply that can be adjusted from +1.3V to +2.5V by 0.1V step. +2.5V for camera is generated by a MIC5209.

2.3 Reset

An on-board reset circuit (MIC811) provides the active low reset signal for microprocessor and other devices when power-up, the push button K2 can also reset the microprocessor and peripheral devices when push-down (manual reset). Blue LED D3 indicates the RESET signal valid.

2.4 RTC

The Real Time Clock 32.768kHz of Libra is provided by PCF8563. In Hibernate Mode, the RTC is needed to wakeup Jz4730. The system can access the PCF8563 through I2C bus.

2.5 Static Memory

The Libra provides three blocks Flash memory devices
The U11 is a DIP32 socket, supports 8bits FLASH, EPROM, DOC and ROM Emulator.
The U8 is an Intel StrataFlash 28F128J3A 16MB Flash.
The U9 is Samsung K9F2808U0C 16MB NAND Flash.

The Libra can boot from any of these devices by set the Switch SW1.
Table 2-1 shows the static memory mode

Table 2-1 Memory Usage and Mapping (SW1 ON=0)

SW1.1	SW1.2	SW1.3	SW1.4	SW1.8	Memory Mapping				Note
B_SEL0	B_SEL1	B_SEL2	B_SEL3	B_SEL4	CS0	CS1	CS2	CS3	
1	0	0	0	1	U8(Boot)	U11		U9	
0	1	0	0	1	U11(Boot)	U8		U9	
0	0	0	1	0		U8	U11	U9(Boot)	

Table 2-2 shows how to select U11 memory type

Table 2-2 U11 memory type Select Jumpers

JP9	JP10	JP8	Boot Memory Type	Note
A18/WE	A18/19	Power	Signal Select	
2-3	2-3	2-3	DISK ON Chips up to 72Mbytes, 3.3V	
2-3	2-3	1-2	FLASH, 5V	
2-3	2-3	2-3	FLASH, 3.3V	
1-2	1-2	1-2	EPROM, 5V	
1-2	1-2	2-3	EPROM, 3.3V	
1-2	1-2	OFF	ROM Emulator	

Avoid to destroy the code of static memory, there are write-protected Jumpers for them.

Table 2-3 Write-Protected Jumpers

	Short(ON) is Write-Protected(Default is OFF)
JP5	U9 Write-Protected Jumper
JP6	U8 Write-Protected Jumper
JP7	U11 Write-Protected Jumper

2.6 SDRAM

Libra provides 64MB SDRAM by two 4Banks X 4M X 16Bit SDRAM chips.

2.7 10/100M Ethernet Port

Libra supports 10/100M Base-T Ethernet port through a RTL8201BL Ethernet PHY chip.

2.7.1 PHY Power-ON Configuration

Three jumpers are used to control PHY (U28) mode when power on, the JP12, JP13, JP14 are listed as below.

Table 2-4 PHY1 Power-ON Configuration

JP12	JP13	JP14	Mode
OFF	OFF	OFF	Auto negotiation enables all capabilities (Default)
ON	ON	ON	Manually select 10TX HDX
ON	OFF	ON	Manually select 10TX FDX
ON	ON	OFF	Manually select 100TX HDX
ON	OFF	OFF	Manually select 100TX FDX

2.7.2 Working Status

On RJ45 connector, there are two LED to indicate the status of the Ethernet port, the yellow one means 10M link; the green one means 100M link.

The JP11 is shorted to disable RTL8201BL. The default is OPEN.

2.8 LCD Connector

The Libra provides a LCD connector J14 (2X20 2mm socket). The user can use Libra's extended LCD card directly, also connect your own LCD panel.
The LCD connector signals are defined as table below:

Table 2-5 LCD (J14) Connector Signals Definition

Pin Number	Signal	Pin Number	Signal
1	LCD_VCC	2	GND
3	+5V	4	GND
5	DISP_OFF_N	6	LCD_GP2
7	GND	8	GND

9	LCD_DD0	10	LCD_DD1
11	LCD_DD2	12	LCD_DD3
13	LCD_DD4	14	LCD_DD5
15	LCD_DD6	16	LCD_DD7
17	LCD_DD8	18	LCD_DD9
19	LCD_DD10	20	LCD_DD11
21	LCD_DD12	22	LCD_DD13
23	LCD_DD14	24	LCD_DD15
25	LCD_GP1	26	PWM0
27	LCD_PPCLK	28	LCD_LLCLK
29	LCD_FFCLK	30	GND
31	LCD_DE_B	32	LCD_SPL_B
33	LCD_REV_B	34	LCD_CLS_B
35	LCD_PS_B	36	GND
37	TSX+	38	TSX-
39	TXY+	40	TSY-

JP24 is used to select LCD_VCC voltage:

1-2 short: LCD_VCC=+3.3V (Default);

2-3 short: LCD_VCC=+5V

JP19，JP20，JP21，JP22 is used to select Touch Panel controlled by U23 (UCB1400) or U24 (TSC2301) dual to Audio Subsystem:

1-2 short: U23 control (Default);

2-3 short: U24 control.

2.9 USB Ports

The Libra provide two USB 1.1 HOST ports, one USB 1.1 Client port. When use USB Client port, USB HOST0 must be disable. It is set by JP15, JP16 and software configuration.

JP15, JP16:

1-2 short: USB HOST0 enabled;

2-3 short: USB Device enabled.

2.10 Audio Subsystem

There are two audio codec on the Libra. One is AC'97 audio codec UCB1400 (U23); another is I2S audio codec TSC2301 (U24). The signals of AC'97 and I2S are multiplexed; two codecs can't work at the same time.

JP23 is used to select which one work:

1-2 short: AC'97 codec work;

2-3 short: I2S codec work.

2.11 Camera Connector

The Libra provides a Camera FPC connector J16. You can use your own Camera Module.

The Camera Connector signals are defined as table below:

Table 2-6 Camera Connector (J16) Signals Definition

Pin Number	Signal	Pin Number	Signal
1	GND	2	CIM_HSYNC
3	CIM_VSYNC	4	PWDN
5	CIM_PCLK	6	+2.5V
7	+3.3V	8	I2C_SDA
9	CLK_24MHz_CAM	10	I2C_SCK
11	CIM_D0	12	CIM_D1
13	CIM_D2	14	CIM_D3
15	GND	16	CIM_D4
17	CIM_D5	18	CIM_D6
19	CIM_D7	20	RESET

JP26 is used to select the clock of Camera supplied by Jz4730 or OSC2:

1-2 short: By CPU;

2-3 short: By OSC.

2.12 Smart Card Socket

The Libra provide two smart card, meet the ISO7816 standard. The socket J21 is for big card; another J22 is for small card (rear of baseboard). The Libra uses LTC1555L to provide power and lever shift for smart card, and more than 10kV ESD Protection. The power of card is set by SW2. This version can't support card hot-plug, please set the SW2 before power up the board.

The table below shows the SW2 configuration:

Table 2-7 SW2 Configuration

SW2.1	SW2.2	SW2.3	SW2.4	Boot Memory Type
0	0	X	X	J21: Shutdown
0	1	X	X	J21:VCC=VIN
1	0	X	X	J21:VCC=+3.3V
1	1	X	X	J21:VCC=+5V
X	X	0	0	J22: Shutdown
X	X	0	1	J22:VCC=VIN
X	X	1	0	J22:VCC=+3.3V
X	X	1	1	J22:VCC=+5V

2.13 PS2 Port

The Libra provides a standard PS2 keyboard connector (J10), can't support PS2 mouse.

2.14 Serial Ports

The Libra provides four RS232 serial ports. Ports 0,1,2 can only support TXD, RXD signals. Port 3

supports TXD, RXD, CTS, RTS signals. Ports 0,3 are located a standard Dual DB9 connector (J6). Ports 1,2 are located two female sockets (2X5 pins, 2.54mm pitch) J7 and J8.

Table 2-8 J7, J8 signals definition

Pin Number	Signal	Pin Number	Signal
1	NC	2	RXD
3	TXD	4	NC
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

2.15 IrDA

The Libra provide a IrDA transmitter U6, can communicate with SIR Device. IrDA is multiplexed with Serial Port 1.

JP17,JP18 are used to select which one work:

Table 2-9 JP17, JP18 Configuration

JP17,JP18		Mode
1-2	2-3	
ON	OFF	UART1 enabled
OFF	ON	IrDA enabled

2.16 JTAG Connector

The Libra provides a standard MIPS EJTAG connector J1. The customer can use standard MIPS EJTAG debug tools or JDI of INGENIC® to develop software and hardware.
JTAG signals are defined as table below:

Table 2-10 JTAG Connector (J1) signals definition

Pin Number	Signal	Pin Number	Signal
1	JZ_TRST_N	2	GND
3	JZ_TDI	4	GND
5	JZ_TDO	6	GND
7	JZ_TMS	8	GND
9	JZ_TCK	10	GND
11	RST_N	12	KEY
13	NC	14	+3.3V

2.17 Matrix Keypad Connector

The Libra provides a 8X8 matrix keypad connector which is connected to static memory bus. The customer can connected a keypad for system input. The signals of Keypad connector J9 are defined as table below:

Table 2-11 Keypad connector (J9) signals definition

Pin Number	Signal	Pin Number	Signal
1	KOUT0	2	KOUT1
3	KOUT2	4	KOUT3
5	KOUT4	6	KOUT5
7	KOUT6	8	KOUT7
9	KIN0	10	KIN1
11	KIN2	12	KIN3
13	KIN4	14	KIN5
15	KIN6	16	KIN7
17	CPLD_T1(Reserved)	18	CPLD_T2(Reserved)
19	KEY	20	GND

2.18 System Expansion Slot

In order to the customer add other module , the Libra provides an Expansion Slot P1. Expansion Slot signals Include:

- Static Memory Bus
- One DMA Channel
- I2C Bus
- SSI Bus
- +3.3V, +5V, +12V

P1 signals are defined as table below:

Table 2-12 Expansion Slot (P1) signals definition

Pin Number	Signal	Pin Number	Signal
A1	+3.3V	B1	+3.3V
A2	NC	B2	NC
A3	DREQ0	B3	DACK0
A4	CPLD_T2(Reserved)	B4	CPLD_T1(Reserved)
A5	EOP	B5	BWAIT_N
A6	NC	B6	NC
A7	AEN	B7	CPLD_CS2(Reserved)
A8	NC	B8	NC
A9	CPLD_CS1	B9	CPLD_CS0
A10	IOIS16_N	B10	INPACK_N
A11	PBVD2	B11	PSKTSEL
A12	PCE1_N	B12	PCE2_N
A13	GND	B13	GND
A14	FRB_N	B14	FRE_N
A15	FEW_N	B15	SSI_CE1_N
A16	I2C_SDA	B16	I2C_SCK
A17	SSI_DT	B17	SSI_CLK
A18	SSI_CE2_N	B18	SSI_DR

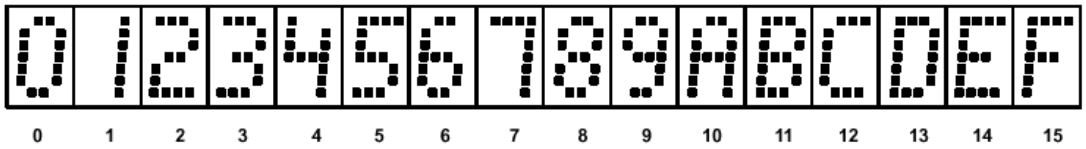
A19	RESET	B19	RSTOUT_N
A20	+5V	B20	+5V
A21	+5V	B21	+12V
A22	KEY	B22	KEY
A23	KEY	B23	KEY
A24	KEY	B24	KEY
A25	KEY	B25	KEY
A26	NC	B26	RESETP_N
A27	NC	B27	NC
A28	GND	B28	GND
A29	CS3_N	B29	DCS1_N
A30	NC	B30	NC
A31	NC	B31	BRDWR_N
A32	NC	B32	NC
A33	BWE1_N	B33	BWE0_N
A34	BWE_N	B34	BRD_N
A35	+3.3V	B35	+3.3V
A36	BA25	B36	BA24
A37	BA23	B37	BA22
A38	BA21	B38	BA20
A39	BA19	B39	BA18
A40	BA17	B40	BA16
A41	BA15	B41	BA14
A42	BA13	B42	BA12
A43	BA11	B43	BA10
A44	BA9	B44	BA8
A45	BA7	B45	BA6
A46	BA5	B46	BA4
A47	BA3	B47	BA2
A48	BA1	B48	BA0
A49	GND	B49	GND
A50	NC	B50	NC
A51	NC	B51	NC
A52	NC	B52	NC
A53	NC	B53	NC
A54	NC	B54	NC
A55	NC	B55	NC
A56	NC	B56	NC
A57	NC	B57	NC
A58	BD15	B58	BD14
A59	BD13	B59	BD12
A60	BD11	B60	BD10

A61	BD9	B61	BD8
A62	BD7	B62	BD6
A63	BD5	B63	BD4
A64	BD3	B64	BD2
A65	BD1	B65	BD0
A66	+3.3V	B66	+3.3V

2.19 System Status Display

The Libra provides four LED light diodes and two seven-segment hex display digits for system status display. GP96, GP97, GP98, GP99 are used to light four light diode (D5, D6, D7, D8). Two seven-segment hex display digits (U13, U14) can be operated by access the fixed static memory space.

The resultant displays for the values of the binary data in the latches are as shown below.



2.20 SD/MMC Socket (optional)

Default is unsupported.

2.21 16 bits PC CARD socket (optional)

Default is unsupported.

2.22 Logic Analyzer Probe Socket (optional)

Default is unsupported.

2.23 Adjustable CORE Voltage

The CORE Voltage of Jz4730 can be adjusted by SW3. The default is +1.8V. The custom should not adjust it usually.

Table 2-13 SW3 CORE Voltage Configuration

SW3 CODE(1,2,3,4)	Core 电压
0，1，1，1	1.30V
1，0，1，1	1.48V
0，0，1，1	1.54V
1，1，0，1	1.64V
0，1，0，1	1.70V
1，1，1，0	1.80V
1，0，0，1	1.88V
0，0，0，1	1.94V
1，0，1，0	2.04V
0，0，1，0	2.10V

1，1，0，0	2.20V
0，0，0，0	2.50V

3 Programming Reference Resources

3.1 Static Memory Mapping

Table 3-1 Static Memory Mapping (Boot from U8)

Start Address	End Address	Connectable Memory	Capacity
H'1C00 0000	H'1CFF FFFF	U8, 16MB Flash (Intel28F128J3A)	16MB
H'1800 0000	H'1BFF FFFF	U11, ROM/FLASH/DOC/Emulator	64MB
H'1400 0000	H'1403 FFFF	U9, NAND Flash (Data Space)	
H'1404 0000	H'1407 FFFF	U9, NAND Flash (Command Space)	
H'1408 0000	H'140B FFFF	U9, NAND Flash (Address Space)	
H'0E00 0000	H'0FFF FFFF	CPLD_CS0	32MB
H'0D80 0000	H'0DFF FFFF	CPLD_CS1	8MB
H'0C80 0000	H'0C80 0000	J9, 8X8 Matrix Keypad	
H'0C00 0000	H'0C00 0001	U13,U14, seven-segment display digits	

Table 3-2 Static Memory Mapping (Boot from U11)

Start Address	End Address	Connectable Memory	Capacity
H'1C00 0000	H'1FFF FFFF	U11, ROM/FLASH/DOC/Emulator	64MB
H'1800 0000	H'18FF FFFF	U8, 16MB Flash (Intel28F128J3A)	16MB
H'1400 0000	H'1403 FFFF	U9, NAND Flash (Data Space)	
H'1404 0000	H'1407 FFFF	U9, NAND Flash (Command Space)	
H'1408 0000	H'140B FFFF	U9, NAND Flash (Address Space)	
H'0E00 0000	H'0FFF FFFF	CPLD_CS0	32MB
H'0D80 0000	H'0DFF FFFF	CPLD_CS1	8MB
H'0C80 0000	H'0C80 0000	J9, 8X8 Matrix Keypad	
H'0C00 0000	H'0C00 0001	U13,U14, seven-segment display digits	

Table 3-3 Static Memory Mapping (Boot from U9)

Start Address	End Address	Connectable Memory	Capacity
H'1800 0000	H'18FF FFFF	U8, 16MB Flash (Intel28F128J3A)	16MB
H'1600 0000	H'17FF FFFF	U11, ROM/FLASH/DOC/Emulator	32MB
H'1400 0000	H'1403 FFFF	U9, NAND Flash (Data Space)	
H'1404 0000	H'1407 FFFF	U9, NAND Flash (Command Space)	
H'1408 0000	H'140B FFFF	U9, NAND Flash (Address Space)	
H'0E00 0000	H'0FFF FFFF	CPLD_CS0	32MB

H'0D80 0000	H'0DFF FFFF	CPLD_CS1	8MB
H'0C80 0000	H'0C80 0000	J9, 8X8 Matrix Keypad	
H'0C00 0000	H'0C00 0001	U13,U14, seven-segment display digits	

3.2 SDRAM Memory Mapping

Table 3-4 SDRAM Memory Mapping

Start Address	End Address	Connectable Memory	Capacity
H'2000 0000	H'23FF FFFF	64MB SDRAM	64MB

3.3 GPIO

Table 3-5 GPIO Mapping

GPIO	Direction	Active	Function
GP96	O	L	D5
GP97	O	L	D6
GP98	O	L	D7
GP99	O	L	D8
GP100	O	L	LCD Display OFF
GP101	O	X	LCD_GP1
GP102	O	X	LCD_GP2
GP103	I	L	RTC Interrupt
GP104	I	L	SD card insert detection signal
GP105	O	L	SD card power enable signal
GP107	O	L	Smart Card 0 Reset
GP110	O	L	Smart Card 1 Reset

4 Quick Start Guide

The Flash of Libra for the customer has been programmed boot loader, system kernel, and local file system. Please operate following the step below:

- Connect a serial cable to the UART0 (the upper DB9 of J6), set the data format to 115200-8N1.
- Connect a 10/100M Shielded Twisted Pair Cable.
- Connect USB keyboard and mouse.
- Plug +12V DC power.

Turn on the power switch, wait a moment, your UART Terminal will display command prompt. In order to keep cleanly output, we shield the debug information of LINUX Kernel.