

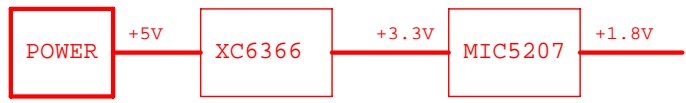
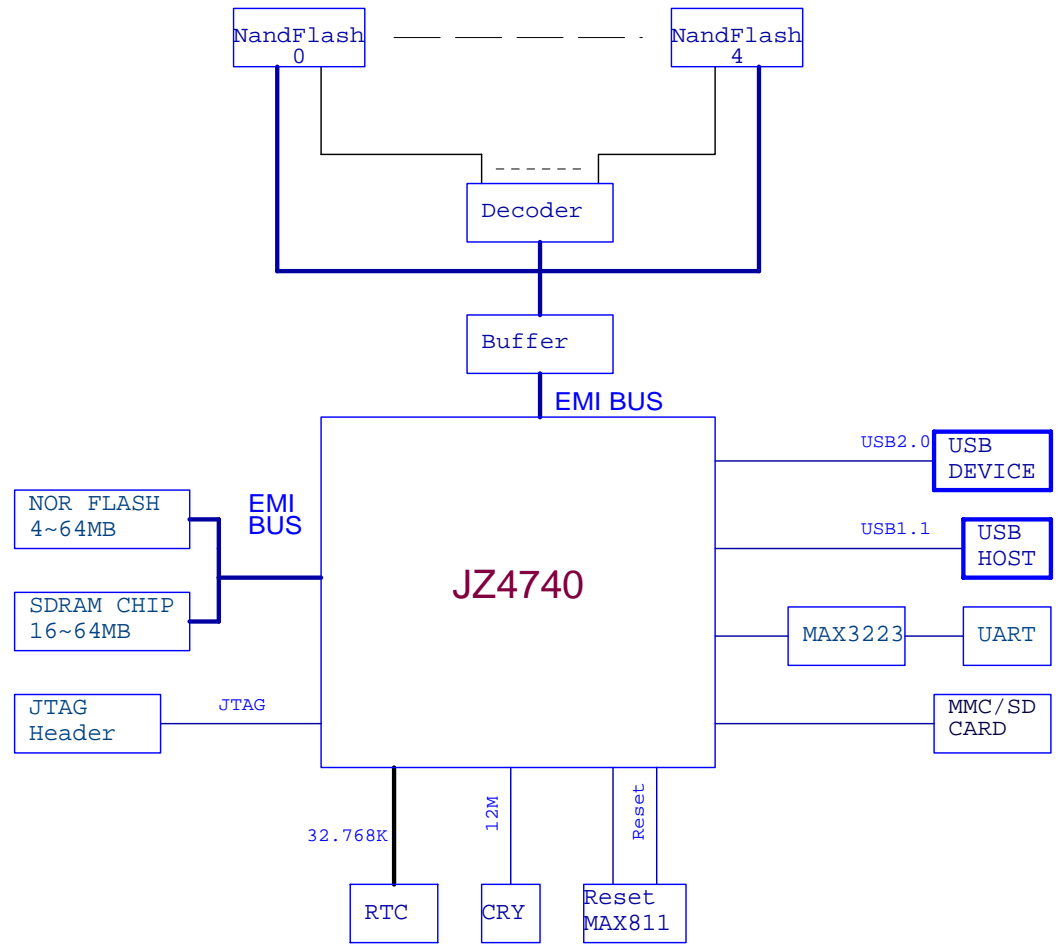


Jz4740 Nandprogrammer Schematic Revision 1.0

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INGENIC Semiconductor Corporation
System Technology Department
Release Data: 2007.11.13

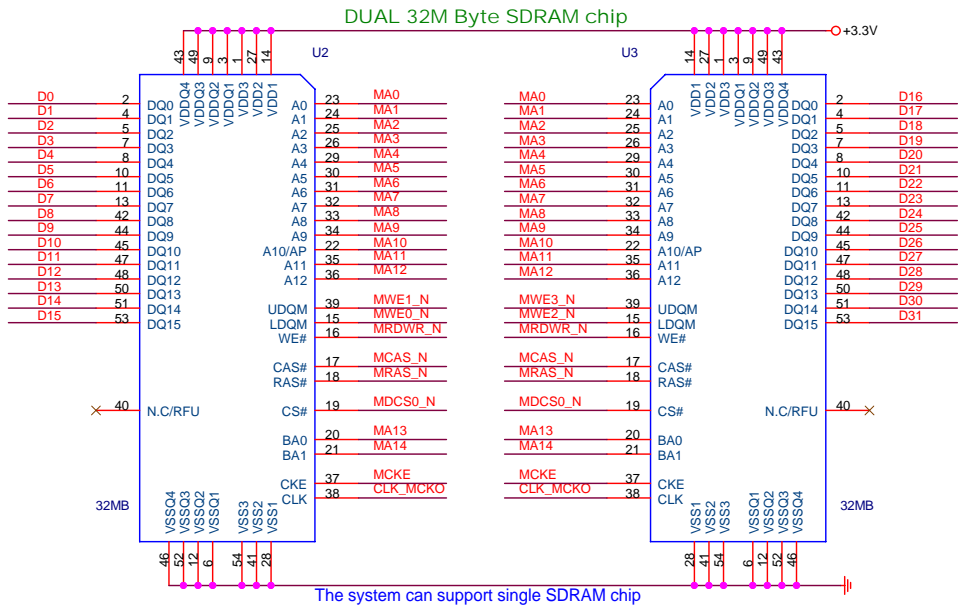
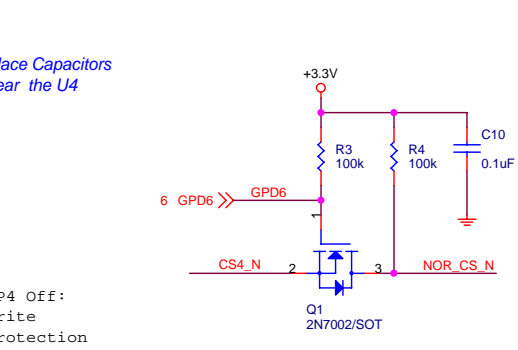
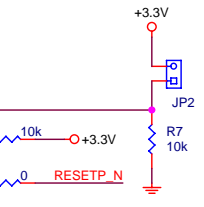
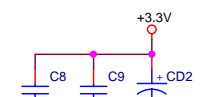
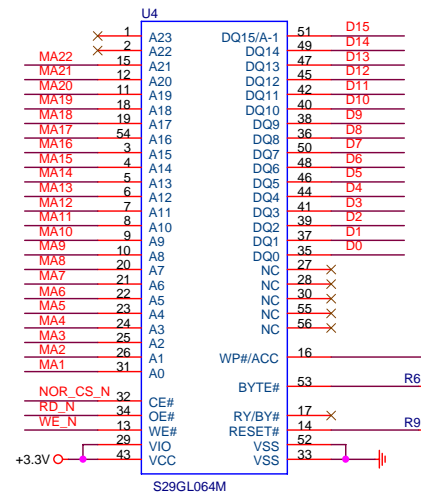
INGENIC Semiconductor Co.,Ltd.		
Title Jz4740 Nandprogrammer		
Size B	Document Number COVER	Rev 1.0
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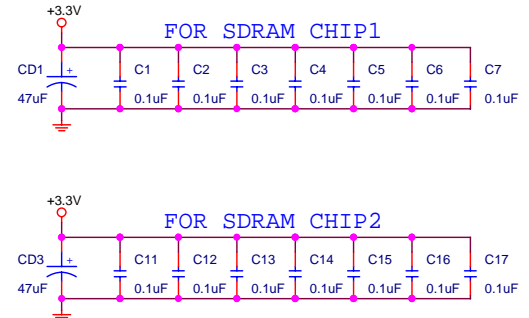
INGENIC Semiconductor Co.,Ltd.		
Title		
Jz4740 Nandprogrammer		
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B	SYSTEM ARCHITECTURE	1.0
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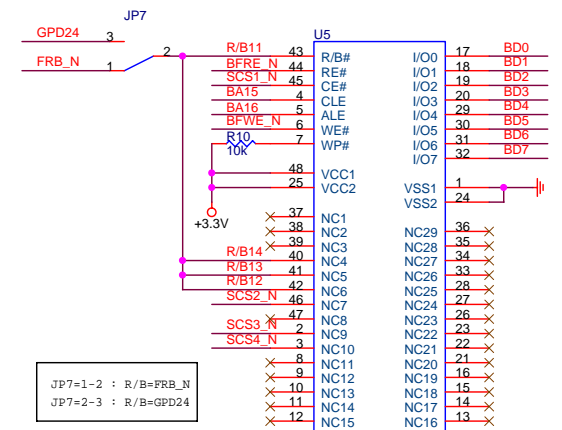
NOR Flash
SPANSION 4M-8M X 8 BIT
NOR FLASH MEMORY



The system can support single SDRAM chip

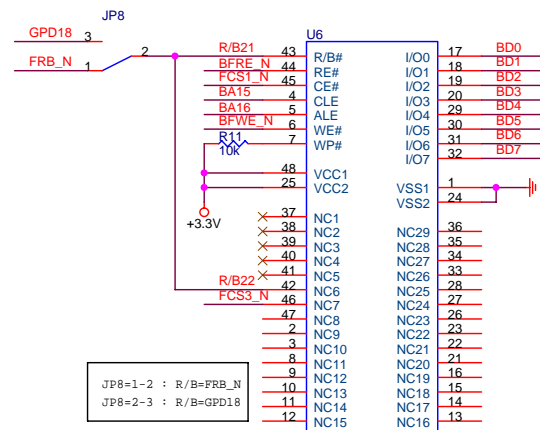


INGENIC Semiconductor Co. Ltd		
Title	Jz4740 Nandprogrammer	
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B	Jz4740_SDRAM & NOR FLASH	1.0
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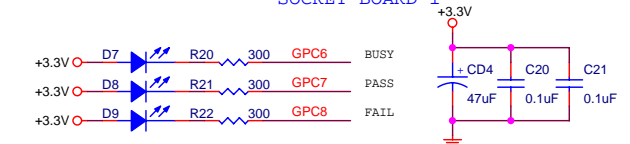
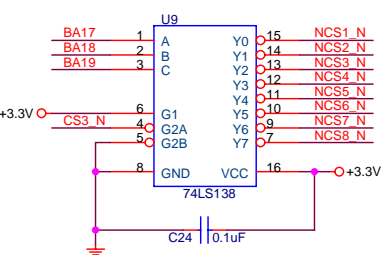
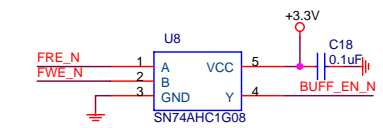
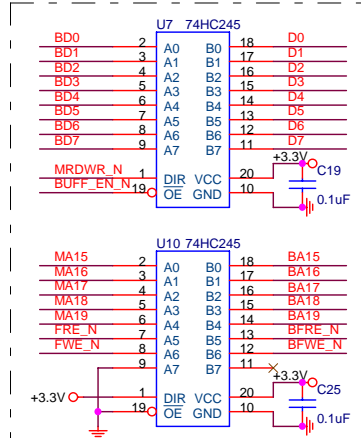
JP7=1-2 : R/B=FRB_N
JP7=2-3 : R/B=GPD24

SOCKET BOARD 1

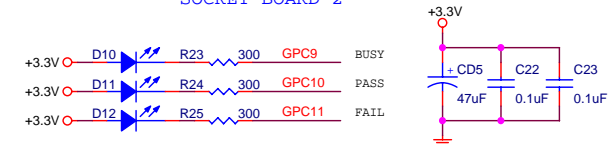


JP8=1-2 : R/B=FRB_N
JP8=2-3 : R/B=GPD18

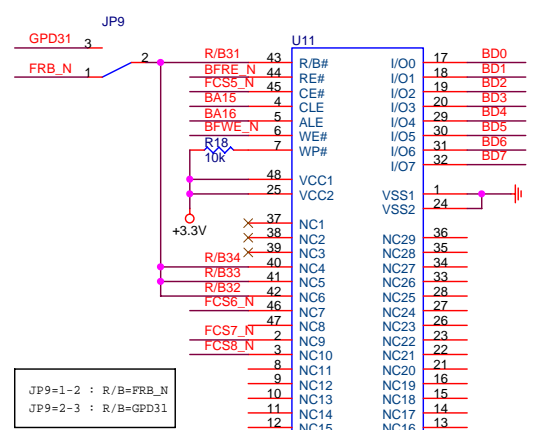
SOCKET BOARD 2



Place Capacitors near the U5

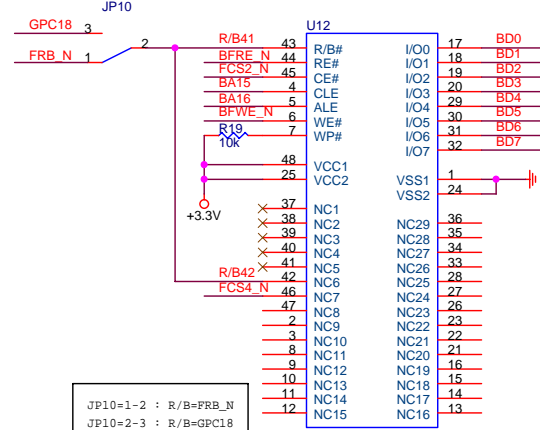


Place Capacitors near the U6



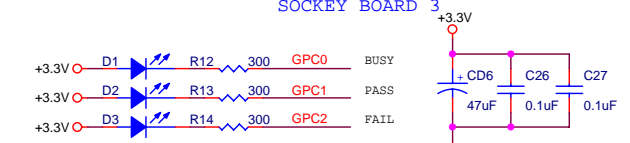
JP9=1-2 : R/B=FRB_N
JP9=2-3 : R/B=GPD31

SOCKET BOARD 3

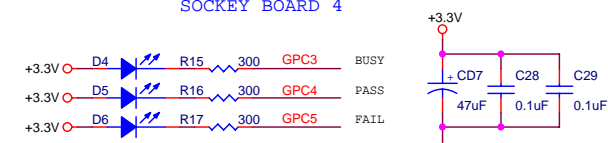


JP10=1-2 : R/B=FRB_N
JP10=2-3 : R/B=GPC18

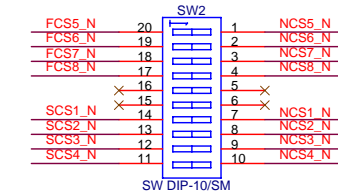
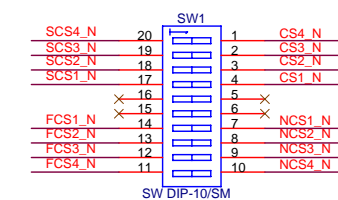
SOCKET BOARD 4



Place Capacitors near the U11



Place Capacitors near the U12

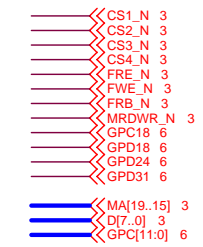


Only SOCKET 1 is 4-CS chip:
SW1.1-4= ON ;
SW1.5-10, SW2= OFF ;
socket 2-4 do not use

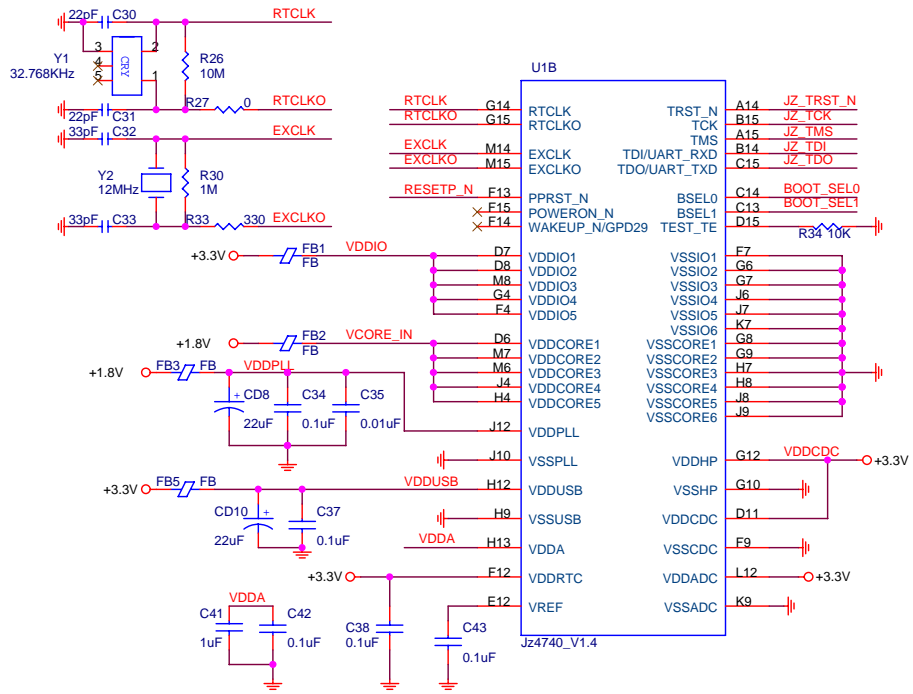
Both SOCKET 1 and SOCKET 3 are 4-CS chip:
SW2= ON ;
SW1= OFF ;
socket 2,4 do not use

All SOCKETs are 2-CS chip:
SW1.3-10, SW2.1-2= ON ;
SW1.1-2, SW2.3-10= OFF ;

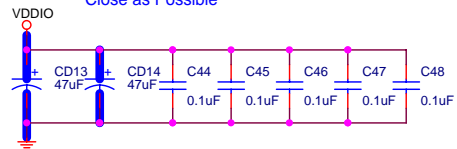
All SOCKETs are 1-CS chip:
SW1.4-8, SW2.1= ON ;
SW1.1-3, SW1.9-10, SW2.2-10= OFF ;



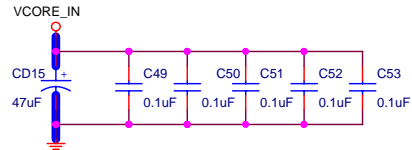
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Title Jz4740 Nandprogrammer		
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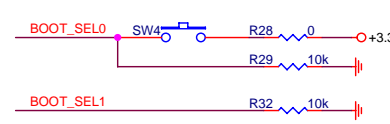
IO Power Decoupling Capacitors
Place near The Power Pins as
Close as Possible



Core Power Decoupling Capacitors
Place near The Power Pins as
Close as Possible

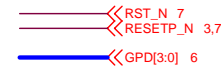
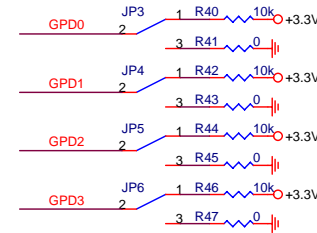
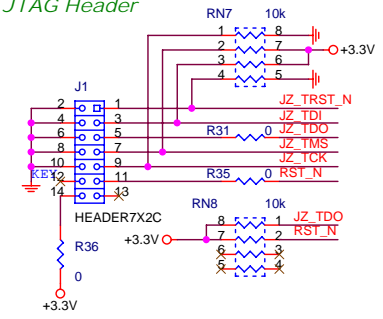


BOOT Configuration



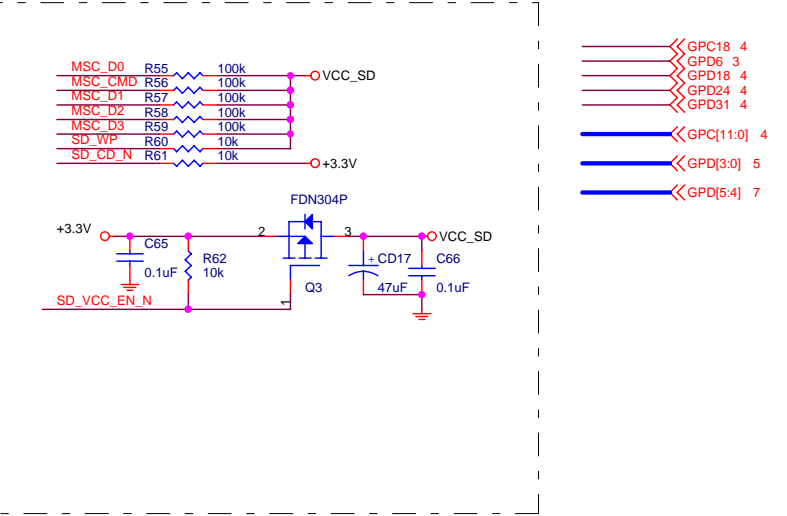
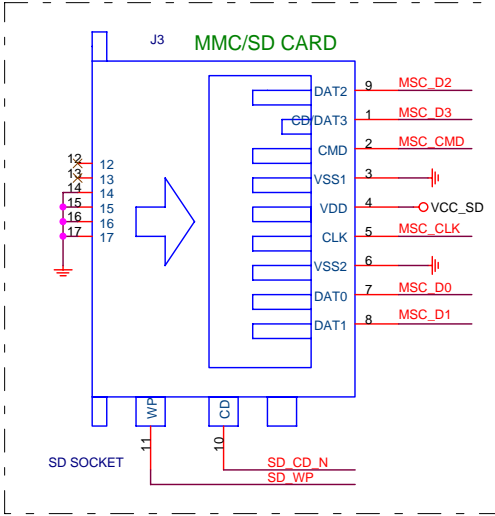
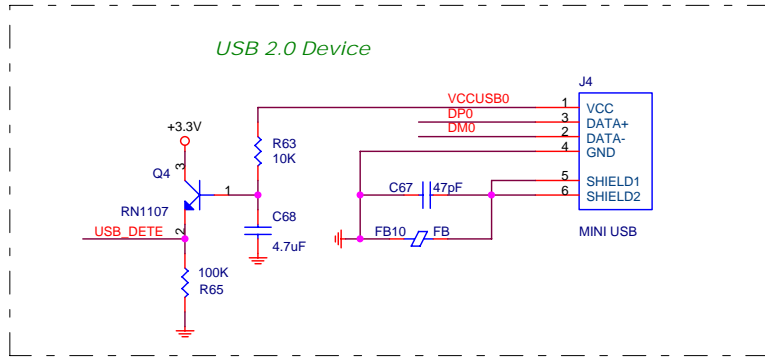
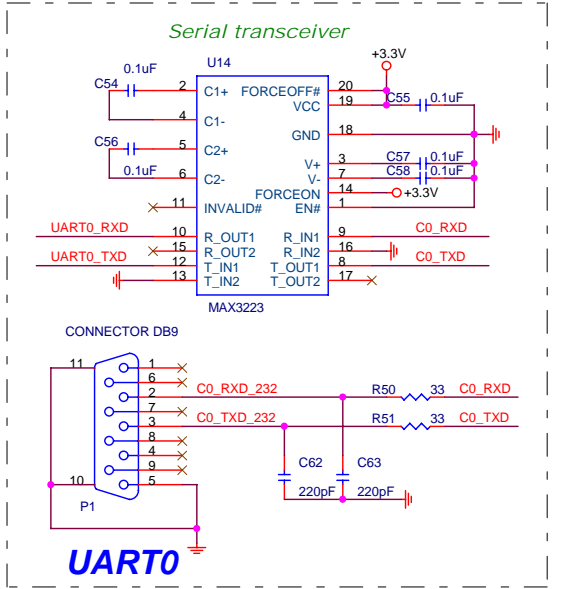
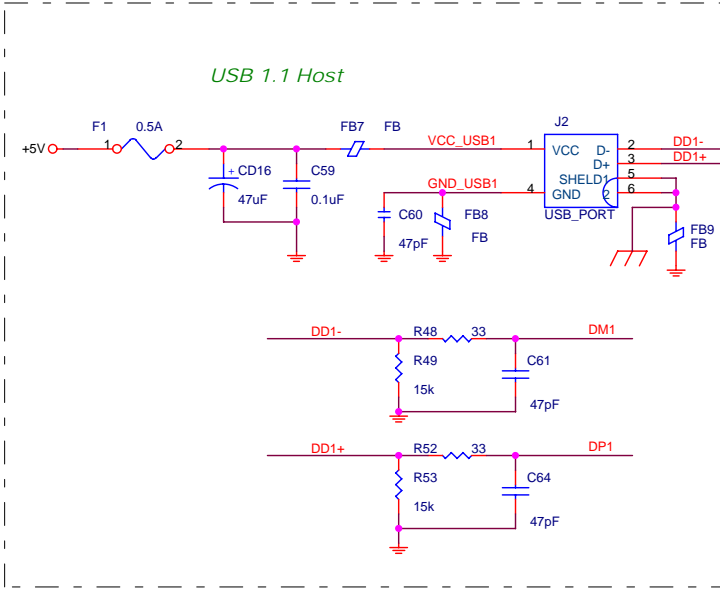
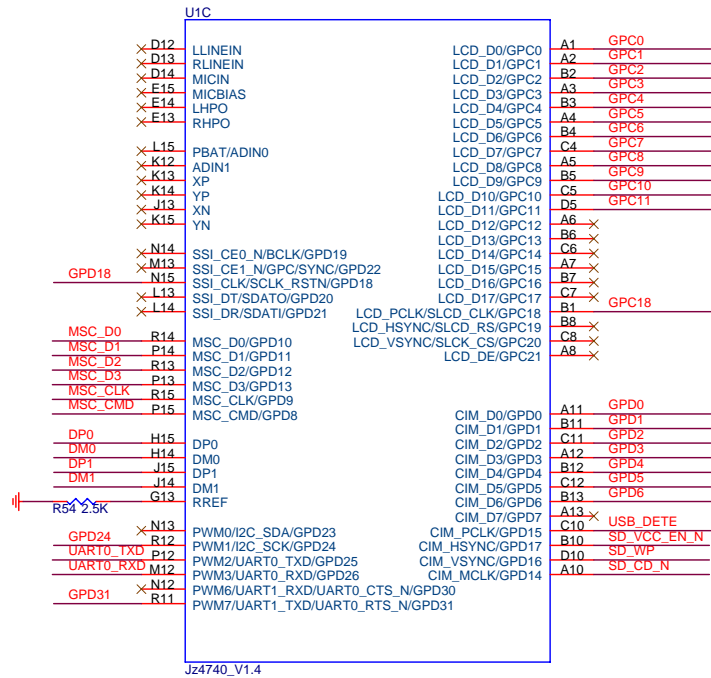
SW4	
OFF	Boot from external ROM at CS4
ON	Boot from USB device

JTAG Header

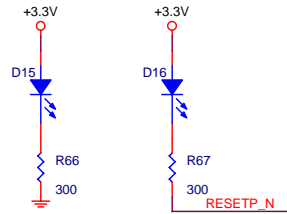


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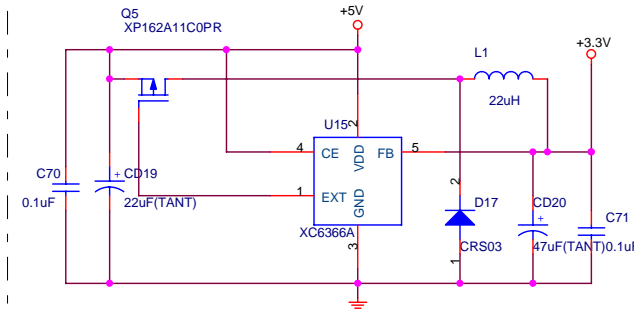
Title		
Jz4740 Nandprogrammer		
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B	Jz4740_POWER & RTC & JTAG	1.0
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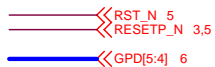
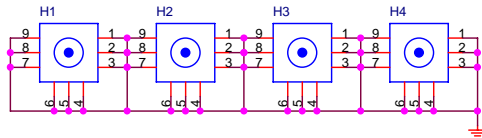
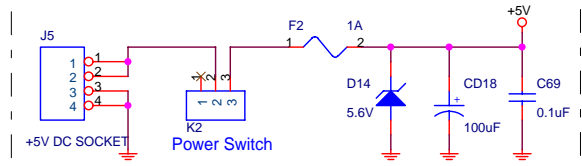
Power Supply Indicators



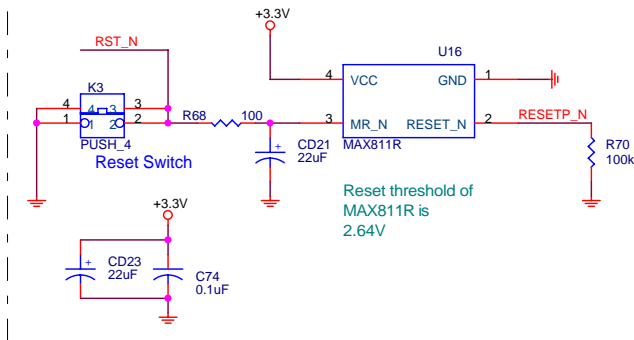
+3.3V Generator



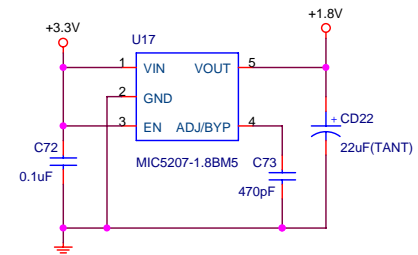
+5V DC-IN



Reset Circuits



VCORE Generator



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Jz4740 Nandprogrammer Schematics

Revision History

Data	Revision	Change
Nov 13 2007	Rev1.0	1. First Revision
Feb 22 2008	Rev1.1	1. Modified U5, U6, U11, U12. 2. Add JP11, JP12, JP13, JP14

INGENIC Semiconductor Co.,Ltd.		
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