Jz4730

Multimedia Application Processor

Data Sheet

Revision: 1.3
Date: Jul. 2007

北京君正集成电路有限公司
Ingenic Semiconductor Co. Ltd

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Data Sheet

Release history

Date	Revision	Change
Apr. 2006	1.0	First release
Aug. 2006	1.1	- Change ball assignment and some DC parameter tables - Add solder process description
Jun. 2007	1.2	PIN description format change
Jul. 2007	1.3	Eliminate DMA pins, GP12 replaced by CHIP_MODE

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1 Overview

Jz4730 is a multimedia application processor targeting for handheld devices like smart-phone, PMP. Incorporate the XBurst® CPU core based on leading micro-architecture technology, this processor provides high integration, high performance and low power consumption solution for embedded device.

XBurst® is a high performance and power-efficient 32-bit RISC core with 16K I-Cache and 16K D-Cache in this processor, operating at speeds up to 336MHz. The memory interface supports a variety of memory types that allow flexible design requirements, include the glueless connection to NAND Flash for cost sensitive applications. On-chip modules such as LCD controller, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. WLAN, Bluetooth and expansion options are provided through the PCMCIA/CF, USB, and MMC/SD host controllers. And the other peripherals such as UART, SPI, smart card controller and Ethernet controller as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

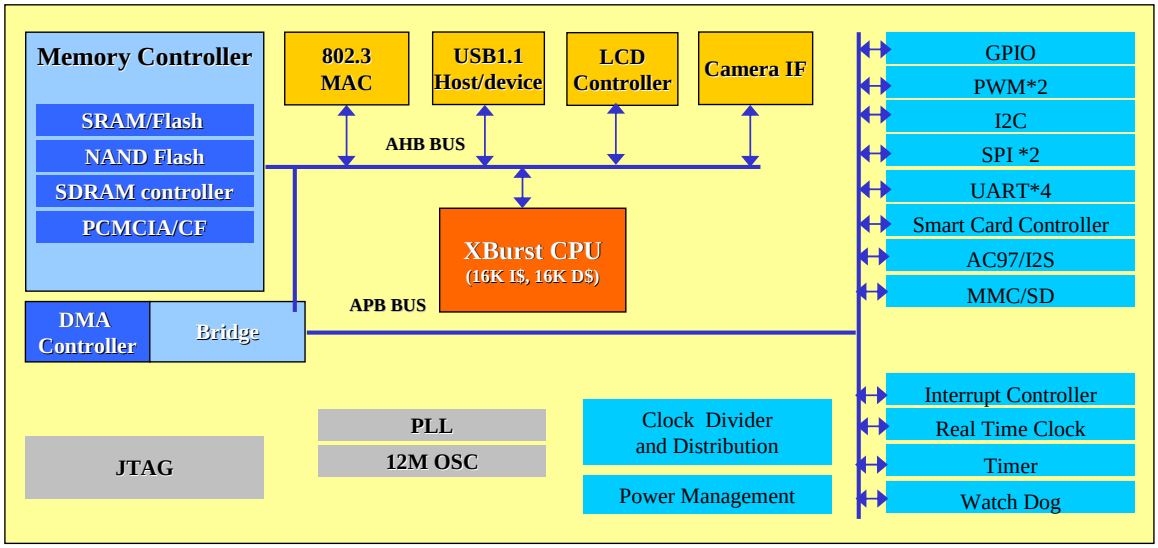


Figure 1-1 Jz4730 Diagram

1.2 Features

1.2.1 CPU core

- XBurst® RISC instruction set to support Linux and WinCE
- XBurst® 8-stage pipeline micro-architecture up to 336MHz
- 16K I-Cache, 16K D-Cache
- 32-entry dual-pages joint-TLB, 4 entry Instruction TLB and 4 entry data TLB
- Hardware Debug support via JTAG port

1.2.2 Memory sub-system

- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Six chip-select pin for static memory, each can be configured separately
  - Support 8, 16 or 32 bits data width
  - The size and base address of static memory banks are programmable
- NAND Flash interface
  - Support on CS3, sharing with static memory bank 3
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Hardware ECC generation
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM Interface
  - 2 banks with programmable size and base address
  - 32-bit and 16-bit data bus width is supported
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
- PC Card Interface
  - Fully compliant with the release of March 1997 of PC Card standard (16-bit PC Card)
  - DMA transfer support
  - Supports two PCMCIA or CF socket
- Direct Memory Access Controller
  - Eight independent DMA channels
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; on-chip peripheral module request; and external request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
- The Jz4730 processor system supports little endian only

1.2.3 Clock generation and power management

- On-chip oscillator circuit
- One On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
- PLL on/off is programmable by software
- ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
- Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function

1.2.4 On-chip peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is 128
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
- Interrupt controller
  - Total 28 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Operating system timer
  - Provide three separate channels
  - 32-bit counter with auto-reload function
  - Generate interrupt when the down counter underflows
  - Six counting clock sources: RTCCLK (real time clock), EXTAL (external clock input), ϕ/4, ϕ/16, ϕ/64 and ϕ/256. (ϕ is the internal clock for on-chip peripheral)
- Watchdog timer
  - 32-bit counter with RTC clock
  - Generate power-on reset
- Pulse Width Modulator (PWM)
  - Period control through a 6-bit clock divider and a 10-bit period counter
  - 10-bit pulse counter
- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - Up to 64K colors in active mode, and up to 4096 colors in passive mode
  - Display size up to 800×600 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
- Camera interface module
  - Input image size up to 2048×2048 pixels
  - Supports CCIR656 data format

- 32×32 image data receive FIFO with DMA support

- AC97/I2S controller
  - Supports 16, 18 and 20 bit sample for AC-link format, and 8, 16, 18, 20 and 24 bit for I2S/MSB-Justified format
  - DMA transfer mode support
  - Programmable Output channels and Input channels or Fixed mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support

- MMC/SD/SDIO controller
  - Compliant with "The MultiMediaCard System Specification version 3.3"
  - Compliant with "SD Memory Card Specification version 1.01" and "SDIO Card Specification version 1.0" with 1 command channel and 4 data channels
  - 20~80 Mbps maximum data rate
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status

- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition

- Synchronous serial interface
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 16-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode

- Four UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Programmable baud rate up to 230.4Kbps
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)

- Two smart card controller
  - Compliant with ISO/IEC standard 7816-3, supports both normal smart card and UIM card interface
  - Support asynchronous character (T = 0)/ block (T = 1) communication modes
  - 8-bit, 16-level FIFO, and programmable SCC_CLK output clock frequency
  - Interrupt support for data communication and error handling

- USB host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible

- USB device interface
  - Compliant with USB protocol revision 1.1
  - Supports suspend/resume and remote wakeup
  - Supports 8 physical endpoints and 9 logic endpoints
  - Supports bulk, isochronous, interrupt and control transaction

- Ethernet MAC interface
  - Compliant with IEEE802.3, 802.3u
  - 10/100 Mbps data transfer rates with full and half duplex modes
  - IEEE802.3 compliant MII interface to talk to an external PHY
  - VLAN support
  - 2K bytes Tx buffers, and 2K bytes Rx buffers
  - Supports DMA engine using burst mode
  - Supports remote wake-up frame and magic packet frame

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	256 BGA 17mm * 17mm
Operating frequency	336 MHz
Power consumption	200mw @ 336MHz

2 Packaging and Pinout Information

2.1 Overview

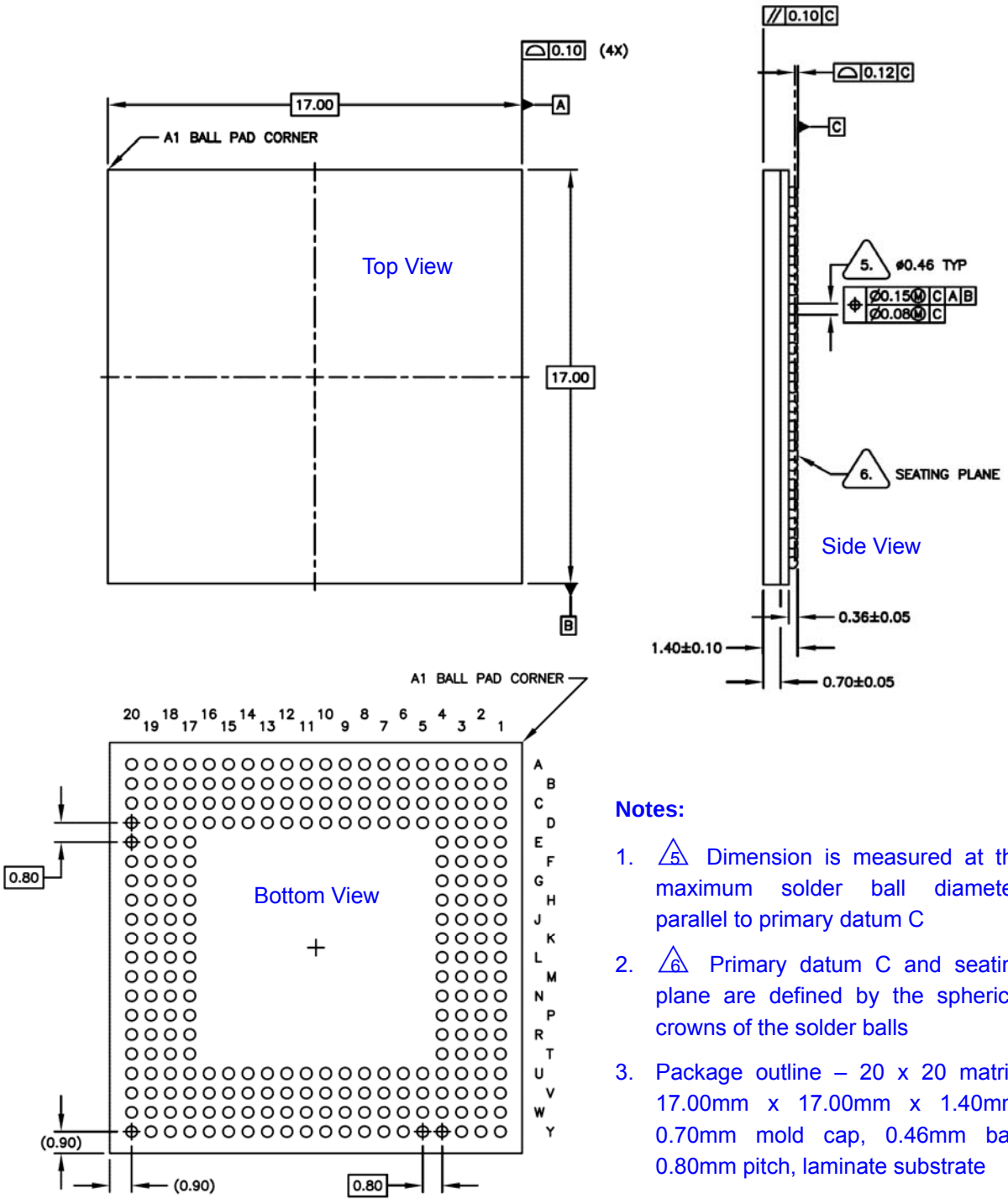
Jz4730 processor is offered in a 256-pin LFBGA package, which is 17mm x 17mm outline, 20 x 20 matrix ball grid array and 0.8mm pitch, show in Figure 2-1.

The Jz4730 pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1 ~ Table 2-20.

2.2 Solder Process

Jz4730 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Package

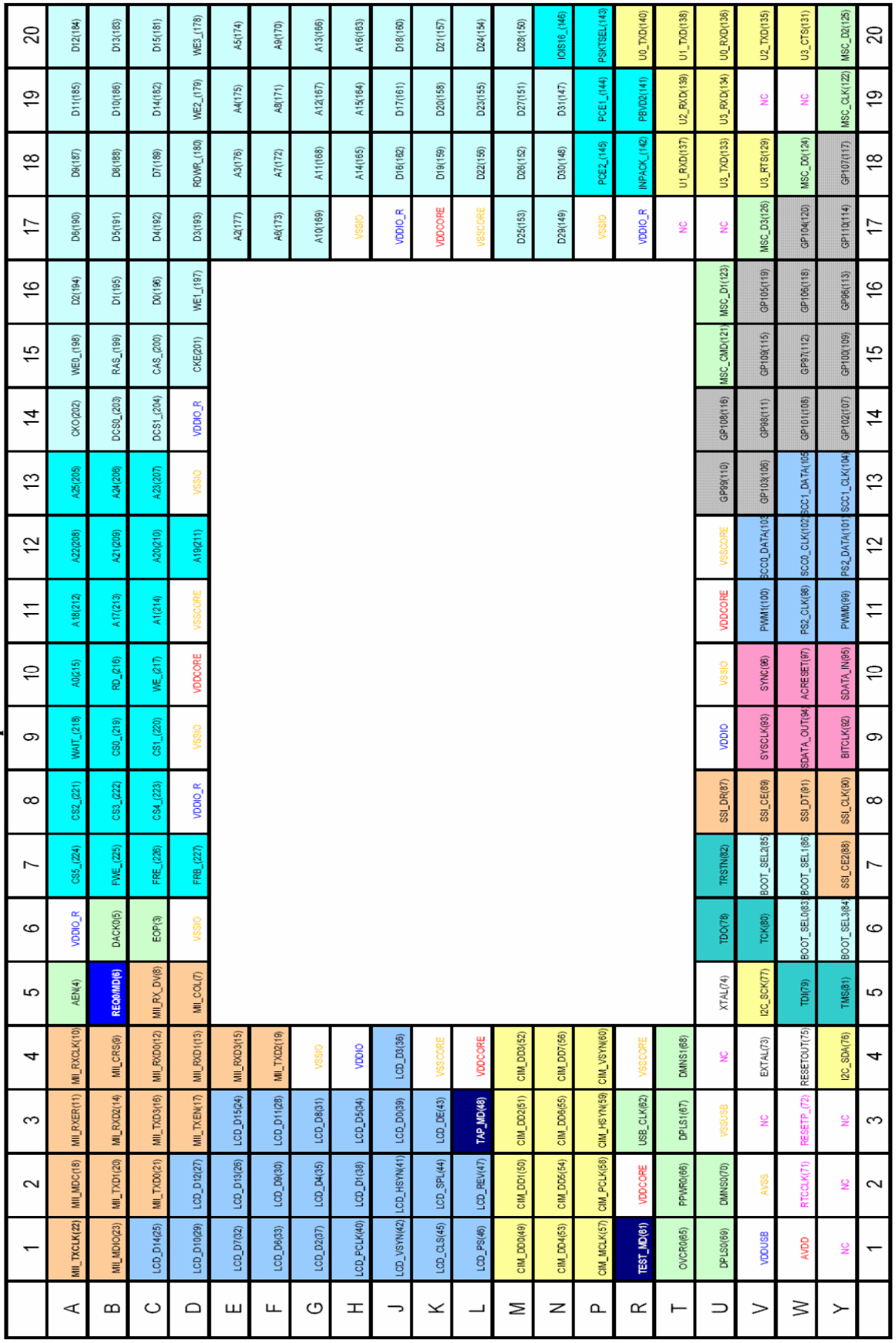


Notes:

1. ⚠5 Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
2. ⚠6 Primary datum C and seating plane are defined by the spherical crowns of the solder balls
3. Package outline – 20 x 20 matrix, 17.00mm x 17.00mm x 1.40mm, 0.70mm mold cap, 0.46mm ball, 0.80mm pitch, laminate substrate

Figure 2-1 Jz4730 package

Top View BGA256



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	MII_TXCLK(22)	MII_MDC(18)	MII_RXER(11)	MII_RXCLK(10)	AEN(4)	VDDIO_R	CS5_(224)	CS2_(221)	WAIT_(218)	A0(215)	A18(212)	A22(208)	A25(205)	CKO(202)	WE0_(198)	D2(194)	D6(190)	D9(187)	D11(185)	D12(184)
B	MII_MDIO(23)	MII_TXD1(20)	MII_RXD2(14)	MII_CRS(9)	REQ0/MD(6)	DACK0(5)	FWE_(225)	CS3_(222)	CS0_(219)	RD_(216)	A17(213)	A21(209)	A24(206)	DCS0_(203)	RAS_(199)	D1(195)	D5(191)	D8(188)	D10(186)	D13(183)
C	LCD_D14(25)	MII_TXD0(21)	MII_TXD3(16)	MII_RXD0(12)	MII_RX_DV(8)	EOP(3)	FRE_(226)	CS4_(223)	CS1_(220)	WE_(217)	A1(214)	A20(210)	A23(207)	DCS1_(204)	CAS_(200)	D0(196)	D4(192)	D7(189)	D14(182)	D15(181)
D	LCD_D10(29)	LCD_D12(27)	MII_TXEN(17)	MII_RXD1(13)	MII_COL(7)	VSSIO	FRB_(227)	VDDIO_R	VSSIO	VDDCORE	VSSCORE	A19(211)	VSSIO	VDDIO_R	CKE(201)	WE1_(197)	D3(193)	RDWR_(180)	WE2_(179)	WE3_(178)
E	LCD_D7(32)	LCD_D13(26)	LCD_D15(24)	MII_RXD3(15)													A2(177)	A3(176)	A4(175)	A5(174)
F	LCD_D6(33)	LCD_D9(30)	LCD_D11(28)	MII_TXD2(19)													A6(173)	A7(172)	A8(171)	A9(170)
G	LCD_D2(37)	LCD_D4(35)	LCD_D8(31)	VSSIO													A10(169)	A11(168)	A12(167)	A13(166)
H	LCD_PCLK(40)	LCD_D1(38)	LCD_D5(34)	VDDIO													VSSIO	A14(165)	A15(164)	A16(163)
J	LCD_VSYN(42)	LCD_HSYN(41)	LCD_D0(39)	LCD_D3(36)													VDDIO_R	D16(162)	D17(161)	D18(160)
K	LCD_CLS(45)	LCD_SPL(44)	LCD_DE(43)	VSSCORE													VDDCORE	D19(159)	D20(158)	D21(157)
L	LCD_PS(46)	LCD_REV(47)	TAP_MD(48)	VDDCORE													VSSCORE	D22(156)	D23(155)	D24(154)
M	CIM_DD0(49)	CIM_DD1(50)	CIM_DD2(51)	CIM_DD3(52)													D25(153)	D26(152)	D27(151)	D28(150)
N	CIM_DD4(53)	CIM_DD5(54)	CIM_DD6(55)	CIM_DD7(56)													D29(149)	D30(148)	D31(147)	IOIS16_(146)
P	CIM_MCLK(57)	CIM_PCLK(58)	CIM_HSYN(59)	CIM_VSYN(60)													VSSIO	PCE2_(145)	PCE1_(144)	PSKTSEL(143)
R	TEST_MD(61)	VDDCORE	USB_CLK(62)	VSSCORE													VDDIO_R	INPACK_(142)	PB|D2(141)	U0_TXD(140)
T	OVCR0(65)	PPWR0(66)	DPLS1(67)	DMNS1(68)													NC	U1_RXD(137)	U2_RXD(139)	U1_TXD(138)
U	DPLS0(69)	DMNS0(70)	VSSUSB	NC	XTAL(74)	TDO(78)	TRSTN(82)	SSI_DR(87)	VDDIO	VSSIO	VDDCORE	VSSCORE	GP99(110)	GP108(116)	MSC_CMD(121)	MSC_D1(123)	NC	U3_TXD(133)	U3_RXD(134)	U0_RXD(136)
V	VDDUSB	AVSS	NC	EXTAL(73)	I2C_SCK(77)	TCK(80)	BOOT_SEL2(85)	SSI_CE(89)	SYSCLK(93)	SYNC(95)	PWM1(100)	SCC0_DATA(103)	GP103(106)	GP99(111)	GP103(115)	GP105(119)	MSC_D3(126)	U3_RTS(129)	NC	U2_TXD(135)
W	AVDD	RTCCLK(71)	RESETP_(72)	RESETOUT(75)	TDI(79)	BOOT_SEL0(83)	BOOT_SEL1(86)	SSI_DT(91)	SDATA_OUT(94)	ACRESET(97)	PS2_CLK(98)	SCC0_CLK(102)	SCC1_DATA(105)	GP101(108)	GP97(112)	GP106(118)	GP104(120)	MSC_D0(124)	NC	U3_CTS(131)
Y	NC	NC	NC	I2C_SDA(76)	TMS(81)	BOOT_SEL3(84)	SSI_CE2(88)	SSI_CLK(90)	BITCLK(92)	SDATA_IN(96)	PWM0(99)	PS2_DATA(101)	SCC1_CLK(104)	GP102(107)	GP100(109)	GP96(113)	GP110(114)	GP107(117)	MSC_CLK(122)	MSC_D2(125)
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Figure 2-2 Jz4730 pin to ball assignment

2.4 Pin Description[1, 2, 3, 4]

Table 2-1 EMC Pins (81; 9 GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0	IO	C16	8mA	D0: Memory data bus bit 0	VDDIO1
D1	IO	B16	8mA	D1: Memory data bus bit 1	VDDIO1
D2	IO	A16	8mA	D2: Memory data bus bit 2	VDDIO1
D3	IO	D17	8mA	D3: Memory data bus bit 3	VDDIO1
D4	IO	C17	8mA	D4: Memory data bus bit 4	VDDIO1
D5	IO	B17	8mA	D5: Memory data bus bit 5	VDDIO1
D6	IO	A17	8mA	D6: Memory data bus bit 6	VDDIO1
D7	IO	C18	8mA	D7: Memory data bus bit 7	VDDIO1
D8	IO	B18	8mA	D8: Memory data bus bit 8	VDDIO1
D9	IO	A18	8mA	D9: Memory data bus bit 9	VDDIO1
D10	IO	B19	8mA	D10: Memory data bus bit 10	VDDIO1
D11	IO	A19	8mA	D11: Memory data bus bit 11	VDDIO1
D12	IO	A20	8mA	D12: Memory data bus bit 12	VDDIO1
D13	IO	B20	8mA	D13: Memory data bus bit 13	VDDIO1
D14	IO	C19	8mA	D14: Memory data bus bit 14	VDDIO1
D15	IO	C20	8mA	D15: Memory data bus bit 15	VDDIO1
D16	IO	J18	8mA	D16: Memory data bus bit 16	VDDIO1
D17	IO	J19	8mA	D17: Memory data bus bit 17	VDDIO1
D18	IO	J20	8mA	D18: Memory data bus bit 18	VDDIO1
D19	IO	K18	8mA	D19: Memory data bus bit 19	VDDIO1
D20	IO	K19	8mA	D20: Memory data bus bit 20	VDDIO1
D21	IO	K20	8mA	D21: Memory data bus bit 21	VDDIO1
D22	IO	L18	8mA	D22: Memory data bus bit 22	VDDIO1
D23	IO	L19	8mA	D23: Memory data bus bit 23	VDDIO1
D24	IO	L20	8mA	D24: Memory data bus bit 24	VDDIO1
D25	IO	M17	8mA	D25: Memory data bus bit 25	VDDIO1
D26	IO	M18	8mA	D26: Memory data bus bit 26	VDDIO1
D27	IO	M19	8mA	D27: Memory data bus bit 27	VDDIO1
D28	IO	M20	8mA	D28: Memory data bus bit 28	VDDIO1
D29	IO	N17	8mA	D29: Memory data bus bit 29	VDDIO1
D30	IO	N18	8mA	D30: Memory data bus bit 30	VDDIO1
D31	IO	N19	8mA	D31: Memory data bus bit 31	VDDIO1
A0	O	A10	2mA	A0: Static memory address bit 0	VDDIO1
A1	O	C11	2mA	A1: Static memory address bit 1	VDDIO1
A2	O	E17	12mA	A2: Static/SDRAM memory address bit 2	VDDIO1
A3	O	E18	12mA	A3: Static/SDRAM memory address bit 3	VDDIO1
A4	O	E19	12mA	A4: Static/SDRAM memory address bit 4	VDDIO1
A5	O	E20	12mA	A5: Static/SDRAM memory address bit 5	VDDIO1
A6	O	F17	12mA	A6: Static/SDRAM memory address bit 6	VDDIO1
A7	O	F18	12mA	A7: Static/SDRAM memory address bit 7	VDDIO1
A8	O	F19	12mA	A8: Static/SDRAM memory address bit 8	VDDIO1
A9	O	F20	12mA	A9: Static/SDRAM memory address bit 9	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A10	O	G17	12mA	A10: Static/SDRAM memory address bit 10	VDDIO1
A11	O	G18	12mA	A11: Static/SDRAM memory address bit 11	VDDIO1
A12	O	G19	12mA	A12: Static/SDRAM memory address bit 12	VDDIO1
A13	O	G20	12mA	A13: Static/SDRAM memory address bit 13	VDDIO1
A14	O	H18	12mA	A14: Static/SDRAM memory address bit 14	VDDIO1
A15	O	H19	12mA	A15: Static/SDRAM memory address bit 15	VDDIO1
A16	O	H20	12mA	A16: Static/SDRAM memory address bit 16	VDDIO1
A17	O	B11	2mA	A17: Static memory address bit 17	VDDIO1
A18	O	A11	2mA	A18: Static memory address bit 18	VDDIO1
A19	O	D12	2mA	A19: Static memory address bit 19	VDDIO1
A20	O	C12	2mA	A20: Static memory address bit 20	VDDIO1
A21	O	B12	2mA	A21: Static memory address bit 21	VDDIO1
A22	O	A12	2mA	A22: Static memory address bit 22	VDDIO1
A23	O	C13	2mA	A23: Static memory address bit 23	VDDIO1
A24	O	B13	2mA	A24: Static memory address bit 24	VDDIO1
A25	O	A13	2mA	A25: Static memory address bit 25	VDDIO1
DCS0_	O	B14	8mA	DCS0_: SDRAM chip select 0	VDDIO1
DCS1_ GP82	O IO	C14	8mA, pullup-pe	DCS1_: SDRAM chip select 1 GP82: GPIO 82	VDDIO1
RAS_	O	B15	8mA	RAS_: SDRAM row address strobe	VDDIO1
CAS_	O	C15	8mA	CAS_: SDRAM column address strobe	VDDIO1
CKE	O	D15	8mA	CKE: SDRAM clock enable	VDDIO1
RDWR_	O	D18	12mA	RDWR_: SDRAM write enable, 1 – read; 0 – write	VDDIO1
CKO	O	A14	12mA	CKO: SDRAM clock	VDDIO1
CS0_	O	B9	2mA	CS0_: Static memory chip select 0	VDDIO1
CS1_ GP83	O IO	C9	2mA, pullup-pe	CS1_: Static memory chip select 1 GP83: GPIO 83	VDDIO1
CS2_ GP84	O IO	A8	2mA, pullup-pe	CS2_: Static memory chip select 2 GP84: GPIO 84	VDDIO1
CS3_ GP85	O IO	B8	2mA, pullup-pe	CS3_: Static memory chip select 3 GP85: GPIO 85	VDDIO1
CS4_ GP86	O IO	C8	2mA, pullup-pe	CS4_: Static memory chip select 4 GP86: GPIO 86	VDDIO1
CS5_ GP87	O IO	A7	2mA, pullup-pe	CS5_: Static memory chip select 5 GP87: GPIO 87	VDDIO1
RD_ POE_	O O	B10	2mA	RD_: Static memory read strobe POE_: PCMCIA memory read strobe	VDDIO1
WE_ PWE_	O O	C10	2mA	WE_: Static memory write strobe PWE_: PCMCIA memory write strobe	VDDIO1
WE0_ PIOW_	O O	A15	8mA	WE0_: SDRAM/Static memory byte 0 write enable PIOW_: PCMCIA IO write strobe	VDDIO1
WE1_ PIOR_	O O	D16	8mA	WE1_: SDRAM/Static memory byte 1 write enable PIOR_: PCMCIA IO read strobe	VDDIO1
WE2_ PREG_	O O	D19	8mA	WE2_: SDRAM/Static memory byte 2 write enable PREG_: PCMCIA register select	VDDIO1
WE3_	O	D20	8mA	WE3_: SDRAM/Static memory byte 3 write enable	VDDIO1
WAIT_ PWAIT_	I I	A9	pull-up, Schmitt	WAIT_: Slow static memory/device wait signal PWAIT_: PCMCIA wait signal	VDDIO1
FRE_ GP79	O IO	C7	2mA, pullup-pe	FRE_: NAND flash read enable GP79: GPIO 79	VDDIO1
FWE_ GP80	O IO	B7	2mA, pullup-pe	FWE_: NAND flash write enable GP80: GPIO 80	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
FRB_ GP81	I IO	D7	4mA, pullup-pe	FRB_: NAND flash ready/busy GP81: GPIO 81	VDDIO1

Table 2-2 PCMCIA/CF Pins (6; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
IOIS16_ GP92	O IO	N20	4mA, pullup-pe	OIS16_: PCMCIA IO address 16 bit select GP92: GPIO 92	VDDIO1
PSKTSEL GP91	O IO	P20	4mA, pullup-pe	PSKTSEL: PCMCIA socket select GP91: GPIO 91	VDDIO1
PCE1_ GP90	O IO	P19	4mA, pullup-pe	PCE1_: PCMCIA card enable 1 GP90: GPIO 90	VDDIO1
PCE2_ GP93	O IO	P18	4mA, pullup-pe	PCE2_: PCMCIA card enable 2 GP93: GPIO 93	VDDIO1
INPACK_ GP88	I IO	R18	2mA, pullup-pe	INPACK_: PCMCIA INPACK_ signal GP88: GPIO 88	VDDIO1
PBVD2 GP89	I IO	R19	2mA, pullup-pe	PBVD2: PCMCIA BVD2 signal GP89: GPIO 89	VDDIO1

Table 2-3 LCDC Pins (24; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_D0 GP40	O IO	J3	4mA, pullup-pe	LCD_D0: LCD data bit 0 GP40: GPIO 40	VDDIO2
LCD_D1 GP41	O IO	H2	4mA, pullup-pe	LCD_D1: LCD data bit 1 GP41: GPIO 41	VDDIO2
LCD_D2 GP42	O IO	G1	4mA, pullup-pe	LCD_D2: LCD data bit 2 GP42: GPIO 42	VDDIO2
LCD_D3 GP43	O IO	J4	4mA, pullup-pe	LCD_D3: LCD data bit 3 GP43: GPIO 43	VDDIO2
LCD_D4 GP44	O IO	G2	4mA, pulldown-pe	LCD_D4: LCD data bit 4 GP44: GPIO 44	VDDIO2
LCD_D5 GP45	O IO	H3	4mA, pulldown-pe	LCD_D5: LCD data bit 5 GP45: GPIO 45	VDDIO2
LCD_D6 GP46	O IO	F1	4mA, pulldown-pe	LCD_D6: LCD data bit 6 GP46: GPIO 46	VDDIO2
LCD_D7 GP47	O IO	E1	4mA, pulldown-pe	LCD_D7: LCD data bit 7 GP47: GPIO 47	VDDIO2
LCD_D8 GP48	O IO	G3	4mA, pulldown-pe	LCD_D8: LCD data bit 8 GP48: GPIO 48	VDDIO2
LCD_D9 GP49	O IO	F2	4mA, pulldown-pe	LCD_D9: LCD data bit 9 GP49: GPIO 49	VDDIO2
LCD_D10 GP50	O IO	D1	4mA, pulldown-pe	LCD_D10: LCD data bit 10 GP50: GPIO 50	VDDIO2
LCD_D11 GP51	O IO	F3	4mA, pulldown-pe	LCD_D11: LCD data bit 11 GP51: GPIO 51	VDDIO2

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_D12 GP52	O IO	D2	4mA, pulldown-pe	LCD_D12: LCD data bit 12 GP52: GPIO 52	VDDIO2
LCD_D13 GP53	O IO	E2	4mA, pulldown-pe	LCD_D13: LCD data bit 13 GP53: GPIO 53	VDDIO2
LCD_D14 GP54	O IO	C1	4mA, pulldown-pe	LCD_D14: LCD data bit 14 GP54: GPIO 54	VDDIO2
LCD_D15 GP55	O IO	E3	4mA, pulldown-pe	LCD_D15: LCD data bit 15 GP55: GPIO 55	VDDIO2
LCD_VSYNC GP56	IO IO	J1	4mA, pulldown-pe	LCD_VSYNC: LCD frame clock/vertical sync GP56: GPIO 56	VDDIO2
LCD_HSYNC GP57	IO IO	J2	4mA, pullup-pe	LCD_HSYNC: LCD line clock/horizonal sync GP57: GPIO 57	VDDIO2
LCD_PCLK GP58	IO IO	H1	4mA, pulldown-pe	LCD_PCLK: LCD pixel clock GP58: GPIO 58	VDDIO2
LCD_DE GP59	O IO	K3	4mA, pulldown-pe	LCD_DE: STN AC bias drive/non-STN data enable GP59: GPIO 59	VDDIO2
LCD_SPL GP60	O IO	K2	4mA, pullup-pe	LCD_SPL: LCD SPL output for special TFT panel GP60: GPIO 60	VDDIO2
LCD_CLS GP61	O IO	K1	4mA, pullup-pe	LCD_CLS: LCD CLS output for special TFT panel GP61: GPIO 61	VDDIO2
LCD_PS GP62	O IO	L1	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT panel GP62: GPIO 62	VDDIO2
LCD_REV GP63	O IO	L2	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT panel GP63: GPIO 63	VDDIO2

Table 2-4 I2C Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
I2C_SDA	IO	Y4	4mA, open-drain	I2C_SDA: I2C serial data	VDDIO2
I2C_SCK	IO	V5	4mA, open-drain	I2C_SCK: I2C serial clock	VDDIO2

Table 2-5 SCC Pins (4; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SCC0_DATA GP64	IO IO	V12	4mA, pullup-pe	SCC0_DATA: SCC 0 data GP64: GPIO 64	VDDIO2
SCC0_CLK GP66	O IO	W12	4mA, pullup-pe	SCC0_CLK: SCC 0 clock GP66: GPIO 66	VDDIO2
SCC1_DATA GP65	IO IO	W13	4mA, pullup-pe	SCC1_DATA: SCC 1 data GP65: GPIO 65	VDDIO2
SCC1_CLK GP67	O IO	Y13	4mA, pullup-pe	SCC1_CLK: SCC 1 clock GP67: GPIO 67	VDDIO2

Table 2-6 UART Pins (10; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_TXD GP127	O IO	R20	2mA, pullup-pe	UART0_TXD: UART 0 transmitting data GP127: GPIO 127	VDDIO2
UART0_RXD GP126	I IO	U20	2mA, pullup-pe	UART0_RXD: UART 0 receiving data GP126: GPIO 126	VDDIO2
UART1_TXD GP25	O IO	T20	2mA, pullup-pe	UART1_TXD: UART 1 transmitting data GP25: GPIO 25	VDDIO2
UART1_RXD GP24	I IO	T18	2mA, pullup-pe	UART1_RXD: UART 1 receiving data GP24: GPIO 24	VDDIO2
UART2_TXD GP125	O IO	V20	2mA, pullup-pe	UART2_TXD: UART 2 transmitting data GP125: GPIO 125	VDDIO2
UART2_RXD GP111	I IO	T19	2mA, pullup-pe	UART2_RXD: UART 2 receiving data GP111: GPIO 111	VDDIO2
UART3_TXD GP21	O IO	U18	2mA, pullup-pe	UART3_TXD: UART 3 transmitting data GP21: GPIO 21	VDDIO2
UART3_RXD GP16	I IO	U19	2mA, pullup-pe	UART3_RXD: UART 3 receiving data GP16: GPIO 16	VDDIO2
UART3_RTS_ GP23	O IO	V18	2mA, pullup-pe	UART3_RTS_: UART 3 RTS_ (request to send) signal GP23: GPIO 23	VDDIO2
UART3_CTS_ GP17	I IO	W20	2mA, pullup-pe	UART3_CTS_: UART 3 CTS_ (clear to send) signal GP17: GPIO 17	VDDIO2

Table 2-7 SSI Pins (5; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI_CLK GP72	O IO	Y8	2mA, pullup-pe	SSI_CLK: SSI clock output GP72: GPIO 72	VDDIO2
SSI_CE1_ GP73	O IO	V8	2mA, pullup-pe	SSI_CE1_: SSI chip enable 1 GP73: GPIO 73	VDDIO2
SSI_DT GP74	O IO	W8	2mA, pullup-pe	SSI_DT: SSI data output GP74: GPIO 74	VDDIO2
SSI_DR GP75	I IO	U8	2mA, pullup-pe	SSI_DR: SSI data input GP75: GPIO 75	VDDIO2
SSI_CE2_ SPI_GPC GP76	O O IO	Y7	2mA, pullup-pe	SSI_CE2_: SSI chip enable 2 SSI_GPC: SSI general-purpose control signal GP76: GPIO 76	VDDIO2

Table 2-8 DMA Pins ()

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
					VDDIO2
					VDDIO2
					VDDIO2
					VDDIO2

Table 2-9 PWM Pins (2; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 GP94	O IO	Y11	4mA, pullup-pe	PWM0: PWM 0 output GP94: GPIO 94	VDDIO2
PWM1 GP95	O IO	V11	2mA, pullup-pe	PWM1: PWM 1 output GP95: GPIO 95	VDDIO2

Table 2-10 UHC Pins (7; 2 GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB_CLK GP28	I IO	R3	2mA, pullup-pe	USB_CLK: USB 48MHz clock input GP28: GPIO 28	VDDIO2
OVC0	I	T1	Schmitt	OVC0: overcurrent for USB port 0	VDDIO2
PPWR0 GP29	O IO	T2	2mA, pullup-pe	PPWR0: power enable for USB port 0 GP29: GPIO 29	VDDIO2
DPLS0	AIO	U1	USB 1.1 PHY	DPLS0: USB 1.1 data plus port 0	VDDusb
DMNS0	AIO	U2	USB 1.1 PHY	DMNS0: USB 1.1 data minus port 0	VDDusb
DPLS1	AIO	T3	USB 1.1 PHY	DPLS0: USB 1.1 data plus port 1	VDDusb
DMNS1	AIO	T4	USB 1.1 PHY	DMNS0: USB 1.1 data minus port 1	VDDusb

Table 2-11 MAC Pins (17; 13 GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MII_COL GP115	I IO	D5	2mA, pullup-pe	MII_COL: Ethernet collision GP115: GPIO 115	VDDIO2
MII_CRS GP116	I IO	B4	2mA, pullup-pe	MII_ CRS: Ethernet carrier sense GP116: GPIO 116	VDDIO2
MII_TX_CLK	I	A1		MII_TX_CLK: Ethernet transmit clock	VDDIO2
MII_TX_EN GP112	O IO	D3	2mA, pullup-pe	MII_TX_EN: Ethernet transmit enable GP121: GPIO 121	VDDIO2
MII_TXD0 GP117	O IO	C2	2mA, pullup-pe	MII_TXD0: Ethernet transmit data bit 0 GP117: GPIO 117	VDDIO2
MII_TXD1 GP118	O IO	B2	2mA, pullup-pe	MII_TXD1: Ethernet transmit data bit 1 GP118: GPIO 118	VDDIO2
MII_TXD2 GP119	O IO	F4	2mA, pullup-pe	MII_TXD2: Ethernet transmit data bit 2 GP119: GPIO 119	VDDIO2
MII_TXD3 GP120	O IO	C3	2mA, pullup-pe	MII_TXD3: Ethernet transmit data bit 3 GP120: GPIO 120	VDDIO2
MII_RX_CLK	I	A4		MII_RX_CLK: Ethernet receive clock	VDDIO2
MII_RX_DV GP113	I IO	C5	2mA, pullup-pe	MII_RX_DV: Ethernet receive data valid GP113: GPIO 113	VDDIO2
MII_RX_ER GP114	I IO	A3	2mA, pullup-pe	MII_RX_ER: Ethernet receive error GP114: GPIO 114	VDDIO2
MII_RXD0 GP121	I IO	C4	2mA, pullup-pe	MII_RXD0: Ethernet receive data bit 0 GP121: GPIO 121	VDDIO2
MII_RXD1 GP122	I IO	D4	2mA, pullup-pe	MII_RXD1: Ethernet receive data bit 1 GP122: GPIO 122	VDDIO2
MII_RXD2 GP123	I IO	B3	2mA, pullup-pe	MII_RXD2: Ethernet receive data bit 2 GP123: GPIO 123	VDDIO2

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MII_RXD3 GP124	I IO	E4	2mA, pullup-pe	MII_RXD3: Ethernet receive data bit 3 GP124: GPIO 124	VDDIO2
MII_MDC	O	A2	2mA	MII_MDC: Ethernet management clock	VDDIO2
MII_MDIO	IO	B1	2mA	MII_MDIO: Ethernet management data	VDDIO2

Table 2-12 CIM Pins (12; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_D0 GP0	I IO	M1	4mA, pullup-pe	CIM_D0: CIM data input bit 0 GP0: GPIO 0	VDDIO2
CIM_D1 GP1	I IO	M2	4mA, pullup-pe	CIM_D1: CIM data input bit 1 GP1: GPIO 1	VDDIO2
CIM_D2 GP2	I IO	M3	4mA, pullup-pe	CIM_D2: CIM data input bit 2 GP2: GPIO 2	VDDIO2
CIM_D3 GP3	I IO	M4	4mA, pullup-pe	CIM_D3: CIM data input bit 3 GP3: GPIO 3	VDDIO2
CIM_D4 GP4	I IO	N1	4mA, pulldown-pe	CIM_D4: CIM data input bit 4 GP4: GPIO 4	VDDIO2
CIM_D5 GP5	I IO	N2	4mA, pulldown-pe	CIM_D5: CIM data input bit 5 GP5: GPIO 5	VDDIO2
CIM_D6 GP6	I IO	N3	4mA, pulldown-pe	CIM_D6: CIM data input bit 6 GP6: GPIO 6	VDDIO2
CIM_D7 GP7	I IO	N4	4mA, pulldown-pe	CIM_D7: CIM data input bit 7 GP7: GPIO 7	VDDIO2
CIM_VSYNC GP8	I IO	P4	4mA, pulldown-pe	CIM_VSYNC: CIM VSYNC input GP8: GPIO 8	VDDIO2
CIM_HSYNC GP9	I IO	P3	4mA, pullup-pe	CIM_HSYNC: CIM HSYNC input GP9: GPIO 9	VDDIO2
CIM_PCLK GP10	I IO	P2	4mA, pullup-pe	CIM_PCLK: CIM pixel clock input GP10: GPIO 10	VDDIO2
CIM_MCLK GP11	O IO	P1	4mA, pullup-pe	CIM_MCLK: CIM master clock output GP11: GPIO 11	VDDIO2

Table 2-13 PS2 Keyboard Pins (2; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PS2_KCLK GP32	IO IO	W11	2mA, pullup-pe	PS2_CLK: PS/2 keyboard clock GP32: GPIO 32	VDDIO2
PS2_KDATA GP33	IO IO	Y12	2mA, pullup-pe	PS2_KDATA: PS/2 keyboard data GP33: GPIO 33	VDDIO2

Table 2-14 AC97/I2S Pins (6; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
BITCLK GP77	IO IO	Y9	2mA, pullup-pe	BITCLK: AC97/I2S bit clock GP77: GPIO 77	VDDIO2
SDATA_OUT GP70	O IO	W9	2mA, pullup-pe	SDATA_OUT: AC97/I2S serial data output GP70: GPIO 70	VDDIO2

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SDATA_IN GP71	I IO	Y10	2mA, pullup-pe	SDATA_IN: AC97/I2S serial data input GP71: GPIO 71	VDDIO2
SYNC GP78	IO IO	V10	2mA, pullup-pe	SYNC: AC97 frame SYNC or I2S Left/Right GP78: GPIO 78	VDDIO2
SYSCLK GP68	O IO	V9	2mA, pullup-pe	SYSCLK: I2S system clock output GP68: GPIO 68	VDDIO2
ACRESET_ GP69	O IO	W10	2mA, pullup-pe	ACRESET_: AC97 reset output GP69: GPIO 69	VDDIO2

Table 2-15 MSC Pins (6; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC_DAT0 GP34	IO IO	W18	4mA, pullup-pe	MSC_DAT0: MSC data bit 0 GP34: GPIO 34	VDDIO2
MSC_DAT1 GP35	IO IO	U16	4mA, pullup-pe	MSC_DAT1: MSC data bit 1 GP35: GPIO 35	VDDIO2
MSC_DAT2 GP36	IO IO	Y20	4mA, pullup-pe	MSC_DAT2: MSC data bit 2 GP36: GPIO 36	VDDIO2
MSC_DAT3 GP37	IO IO	V17	4mA, pullup-pe	MSC_DAT3: MSC data bit 3 GP37: GPIO 37	VDDIO2
MSC_CMD GP38	IO IO	U15	4mA, pullup-pe	MSC_CMD: MSC command GP38: GPIO 38	VDDIO2
MSC_CLK GP39	O IO	Y19	4mA, pullup-pe	MSC_CLK: MSC clock output GP39: GPIO 39	VDDIO2

Table 2-16 GPIO Pins (15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GP13	IO	B6	2mA, pullup-pe	GP13: GPIO 13	VDDIO2
GP26	IO	A5	2mA, pullup-pe	GP26: GPIO 26	VDDIO2
GP27	IO	C6	2mA, pullup-pe	GP27: GPIO 27	VDDIO2
GP96	IO	Y16	2mA, pullup-pe	GP96: GPIO 96	VDDIO2
GP97	IO	W15	2mA, pullup-pe	GP97: GPIO 97	VDDIO2
GP98	IO	V14	2mA, pullup-pe	GP98: GPIO 98	VDDIO2
GP99	IO	U13	2mA, pullup-pe	GP99: GPIO 99	VDDIO2
GP100	IO	Y15	2mA, pullup-pe	GP100: GPIO 100	VDDIO2
GP101	IO	W14	2mA, pullup-pe	GP101: GPIO 101	VDDIO2
GP102	IO	Y14	2mA, pullup-pe	GP102: GPIO 102	VDDIO2
GP103	IO	V13	2mA, pullup-pe	GP103: GPIO 103	VDDIO2
GP104	IO	W17	2mA, pullup-pe	GP104: GPIO 104	VDDIO2

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GP105	IO	V16	2mA, pullup-pe	GP105: GPIO 105	VDDIO2
GP106	IO	W16	2mA, pullup-pe	GP106: GPIO 106	VDDIO2
GP107	IO	Y18	2mA, pullup-pe	GP107: GPIO 107	VDDIO2
GP108	IO	U14	2mA, pullup-pe	GP108: GPIO 108	VDDIO2
GP109	IO	V15	2mA, pullup-pe	GP109: GPIO 109	VDDIO2
GP110	IO	Y17	2mA, pullup-pe	GP110: GPIO 110	VDDIO2

Table 2-17 JTAG Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	U7	Schmitt, pull-down	TRST_: JTAG reset	VDDIO2
TCK	I	V6	Schmitt, pull-down	TCK: JTAG clock	VDDIO2
TMS	I	Y5	Schmitt, pull-up	TMS: JTAG mode select	VDDIO2
TDI	I	W5	Schmitt, pull-up	TDI: JTAG serial data input	VDDIO2
TDO	O	U6	4mA	TDO: JTAG serial data output	VDDIO2

Table 2-18 System Pins (11)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXTAL	AI	V4	3~20 MHz Oscillator, OSC on/off	EXTAL: OSC input or external clock input	VDDIO2
XTAL	AO	U5		XTAL: OSC output	VDDIO2
RTCLK	I	W2	pulldown-pe	RTCLK: 32768Hz clock input	VDDIO2
RESETP_	I	W3	Schmitt	RESETP_: power on reset and RESET-KEY reset input	VDDIO2
RESETOUT_	O	W4	4mA	RESETOUT_: Reset output	VDDIO2
BOOT_SEL0	I	W6		BOOT_SEL0: Boot select bit 0	VDDIO2
BOOT_SEL1	I	W7		BOOT_SEL1: Boot select bit 1	VDDIO2
BOOT_SEL2	I	V7		BOOT_SEL2: Boot select bit 2	VDDIO2
BOOT_SEL3	I	Y6		BOOT_SEL3: Boot select bit 3	VDDIO2
TEST_MODE	I	R1	Schmitt, pull-down	TEST_MODE: Manufacture test enable	VDDIO2
TAP_MD	I	L3	Schmitt, pull-down	TAP_MD: TAP select. 1: CPU EJTAG TAP; 0: boundary scan JTAG TAP	VDDIO2
CHIP_MODE	I	B5	Schmitt, pull-down	CHIP_MODE: this pin must be inputted 0 or is left not-connected 0 – chip works for handset/mobile multi-media applications 1 – chip works for fiscal applications	VDDIO2

Table 2-19 Not connected Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
NC	-	T17 U4 U17 V3 V19 W19 Y1 Y2 Y3		NC: 9 not connected pins	-

Table 2-20 IO/Core/PLL/USB power supplies (28)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO1	P	A6 D8 D14 J17 R17		VDDIO1: 5 IO digital power, 1.8V ~ 3.3V	-
VDDIO2	P	H4 U9		VDDIO2: 2 IO digital power, 3.3V	-
VSSIO	P	D9 D13 H17 D6 G4 P17 U10		VSSIO: 7 IO digital ground	-
VDDcore	P	D10 K17 L4 R2 U11		VDDcore: 5 CORE digital power, 1.8V	-
VSScore	P	D11 K4 L17 R4 U12		VSScore: 5 CORE digital ground	-
VDDPLL	P	W1		VDDPLL: 1 PLL analog power, 1.8V	-
VSSPLL	P	V2		VSSPLL: 1 PLL analog ground	-
VDDUSB	P	V1		VDDUSB: 1 USB analog power, 3.3V	-
VSSUSB	P	U3		VSSUSB: 1 USB analog ground	-

Notes:

1. IO cells power supplied by VDDIO1 are regular IO cells. DC specification of them is described in Table 3-3 and Table 3-4
2. IO cells power supplied by VDDIO2 are standard IO cells. DC specification of them is described in Table 3-5
3. The meaning of phases in IO cell characteristics are
   a) 2/4/8/12mA: The IO cell's output driving strength is about 2/4/8/12mA
   b) Pull-up: The IO cell contains a pull-up resistor
   c) Pull-down: The IO cell contains a pull-down resistor
   d) Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register
   e) Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register
   f) Schmitt: The IO cell is Schmitt trigged input
4. For any GPIO shared pin, the reset state is GPIO input with internal pull-up or pull-down.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
T_{stg}	Storage Temperature	-65	125	°C
T_{opt}	Operation Temperature	-40	125	°C
	VDDIO1 power supplies voltage	-0.5	4.6	V
	VDDIO2 power supplies voltage	-0.5	4.6	V
	VDDUSB power supplies voltage	-0.5	4.6	V
	VDDcore power supplies voltage	-0.5	2.5	V
	VDDPLL power supplies voltage	-0.5	2.5	V
VI_{IO1}	Input voltage to VDDIO1 supplied non-supply pins	-0.5	4.6	V
VI_{IO2}	Input voltage to VDDIO2 supplied non-supply pins	-0.5	6.0	V
VI_{USB}	Input voltage to VDDUSB supplied non-supply pins	-0.5	6.0	V
VO_{IO1}	Output voltage from VDDIO1 supplied non-supply pins	-0.5	4.6	V
VO_{IO2}	Output voltage from VDDIO2 supplied non-supply pins	-0.5	4.6	V
VO_{USB}	Output voltage from VDDUSB supplied non-supply pins	-0.5	4.6	V
V_{ESD}	Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO1}	VDDIO1 voltage for 3.3V applications	2.97	3.3	3.63	V
V_{IO1}	VDDIO1 voltage for 1.8V applications	1.62	1.8	1.98	V

V_{IO2}	VDDIO2 voltage	2.97	3.3	3.63	V
V_{USB}	VDDUSB voltage	2.97	3.3	3.63	V
V_{CORE}	Core voltage	1.62	1.8	1.98	V
V_{PLL}	PLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO1 supplied pins in 3.3V application

Symbol	Description	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for VDDIO1 supplied pins in 1.8V application

Symbol	Description	Min	Typical	Max	Unit
V_{IH}	Input high voltage	0.65 * V_{IO1}		V_{IO1} + 0.3	V
V_{IL}	Input low voltage	-0.3		0.35 * V_{IO1}	V

Table 3-5 Recommended operating conditions for VDDIO2 supplied pins

Symbol	Description	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		5.5	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-6 Recommended operating conditions for VDDUSB pins

Symbol	Description	Min	Typical	Max	Unit
V_{ILH}	Input voltage range	0		V_{USB}	V

Table 3-7 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		70	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-8 DC characteristics for VDDIO1 supplied pins in 3.3V application

Symbol	Description	Min	Typical	Max	Unit
V_T	Threshold point	1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	50	65	100	kΩ
R_{PD}	Pull-down Resistor	40	56	107	kΩ
C	Capacitance of the pins	4	5	7	pF
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.2	3.7	4.6	
	4mA	4.4	7.4	9.2	
	8mA	8.9	14.7	18.4	
	12mA	13.3	22.1	27.5	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.5	5.1	7.9	
	4mA	5.0	10.2	15.9	
	8mA	10.0	20.4	31.7	
	12mA	15.0	30.6	47.6	

Table 3-9 DC characteristics for VDDIO1 supplied pins in 1.8V application

Symbol	Description	Min	Typical	Max	Unit
V_T	Threshold point	0.87	0.92	0.98	V
V_{T+}	Schmitt trig low to high threshold point	0.95	0.99	1.00	V
V_{T-}	Schmitt trig high to low threshold point	0.56	0.58	0.60	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	94	148	261	kΩ
R_{PD}	Pull-down Resistor	77	135	312	kΩ
C	Capacitance of the pins	4	5	7	pF
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.45	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	V_{IO1} – 0.45			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	0.9	1.9	3.0	
	4mA	1.8	3.8	6.0	
	8mA	3.6	7.6	12.0	
	12mA	5.4	11.4	18.0	

I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	0.9	1.6	2.2	
	4mA	1.8	3.1	4.5	
	8mA	3.7	6.2	9.0	
	12mA	5.5	9.3	13.4	

Table 3-10 DC characteristics for VDDIO2 supplied pins

Symbol	Description	Min	Typical	Max	Unit
V_T	Threshold point	1.45	1.58	1.74	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	39	65	116	kΩ
R_{PD}	Pull-down Resistor	40	56	108	kΩ
C	Capacitance of the pins	6	7.5	10	pF
V_{OL}	Output low voltage @I_{OL}=2, 4mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.4	4.0	5.0	
	4mA	4.7	8.0	10.0	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.8	5.9	9.5	
	4mA	5.6	11.9	19	

Table 3-11 DC characteristics for VDDUSB pins

Symbol	Description	Min	Typical	Max	Unit
V_{OLH}	Output voltage range	0		V_{USB}	V
V_{DI}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V
I_{OZ}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL}	Static output low voltage			0.3	V
V_{OH}	Static output high voltage	2.8			V

3.4 Power Consumption Specifications

Power consumption depends on the operating frequency, operating voltage, program used which determines internal and external switching activities, external loading and even environment

ambient. The typical power consumption of both dynamic and static for the Jz4730 processor are provided here.

Table 3-12 Dynamic Power Consumption Specifications

Symbol	Description	Conditions	Typical	Unit
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1 = VDDIO2 = VDDUSB = 3.3V, Temp = room, CPU clock = 360MHz, AHB/APB/SDRAM clock = 120MHz, Program = run GCC to compile a C file in Linux, 12MHz crystal used for EXCLK, Without 48MHz USB clock input, ETH CIM are not in use, LCD is in use		mA
I_{IO}	VDDIO1 + VDDIO2 current			mA
I_{PLL}	VDDPLL current			mA
I_{USB}	VDDUSB current			mA

Table 3-13 Static Power Consumption Specifications

Symbol	Description	Conditions	Typical	Unit
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1=VDDIO2=VDDUSB=3.3V, Chip enters hibernating mode, Temp = room,		uA
I_{IO}	VDDIO1 + VDDIO2 current			uA
I_{PLL}	VDDPLL current			uA
I_{USB}	VDDUSB current			uA
I_{CORE}	VDDcore current	Same as above except chip enters sleep mode, The difference between sleep mode and hibernating mode is that 12MHz crystal running in sleep mode.		uA
I_{IO}	VDDIO1 + VDDIO2 current			uA
I_{PLL}	VDDPLL current			uA
I_{USB}	VDDUSB current			uA

3.5 Reset and Power AC Timing Specifications

The Jz4730 processor asserts the RESETOUT_ pin in one of several modes:

- Power On Reset (RESETP_)
- Watch Dog Reset (internal controlled)

The following sections provide the timing and specifications for the entry and exit of these modes.

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the Jz4730 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-14.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VDDIO1 & VDDIO2 & VDDUSB
2. VDDCORE & VDDPLL

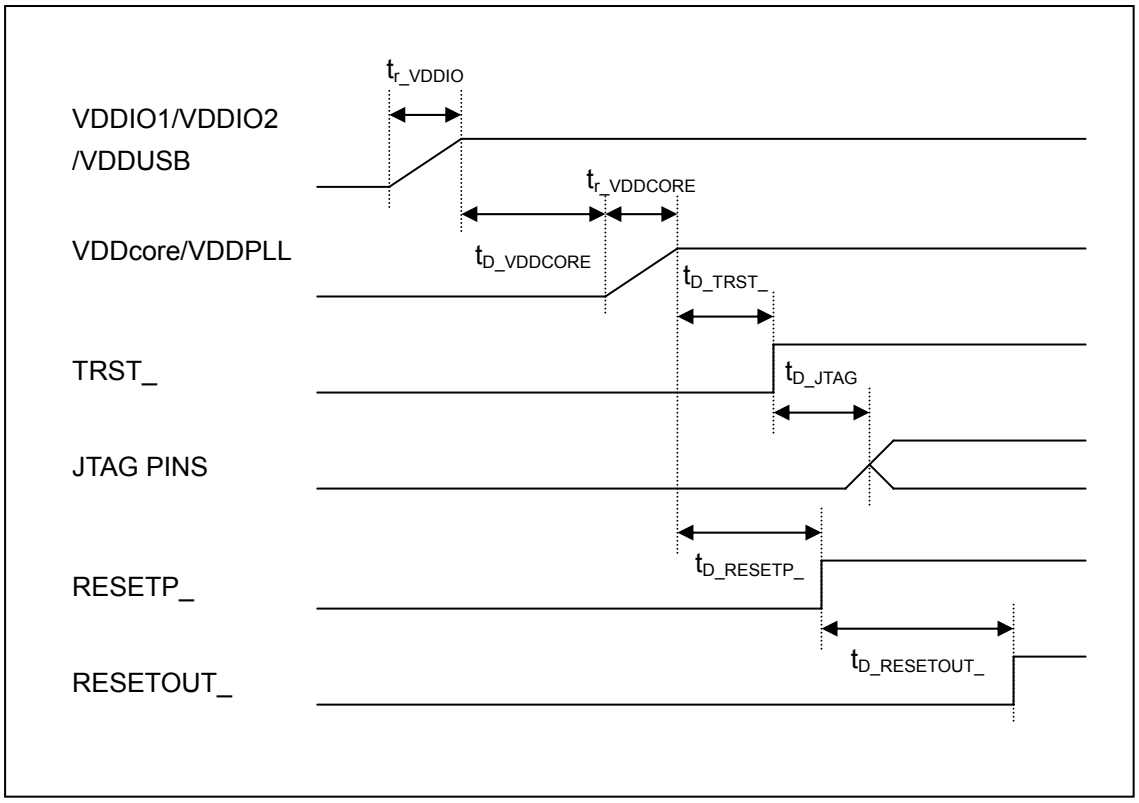


Figure 3-1 Power-On Timing Diagram

Table 3-14 Power-On Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
t_{r_VDDIO}	VDDIO1/VDDIO2/VDDUSB Rise / Stabilization time	0.01	–	100	ms
$t_{D\_VDDCORE}$	Delay between VDDIO1/VDDIO2/VDDUSB stable and VDDCORE/VDDPLL applied	0	–	–	ms
$t_{r\_VDDOCRE}$	VDDOCRE/VDDPLL Rise / Stabilization time	0.01	–	100	ms
$t_{D\_TRST\_}$	Delay between VDDCORE, VDDPLL stable and JTAG reset TRST_ deasserted	10	–	–	ns
t_{D_JTAG}	Delay between TRST_ deasserted and other JATG pins active	10	–	–	ns
$t_{D\_RESETP\_}$	Delay between VDDCORE, VDDPLL stable and RESETP_ deasserted	0.2	–	–	ms
$t_{D\_RESETOUT\_}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	117.2	–	117.3	ms

3.5.2 Hardware Reset Timing

The timing sequences for input signals RESETP_ and output signals RESETOUT_, are shown in Figure 3-2 and Table 3-15, assumes the power supplies are stable at the assertion of RESETP_.

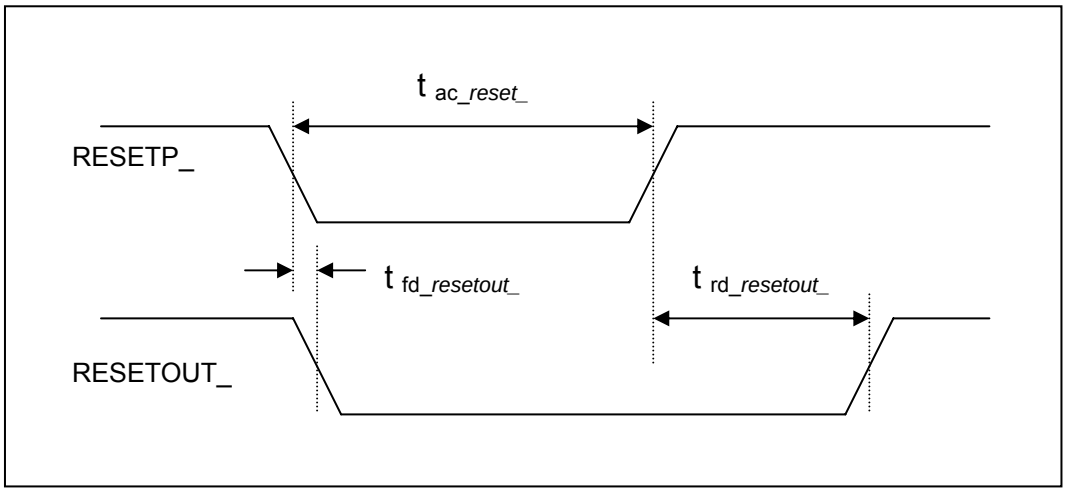


Figure 3-2 Hardware Reset Timing Diagram

Table 3-15 RESETP_ to RESETOUT_ Timing Parameters

Symbol	Description	Min	Typical	Max	Unit
$t_{ac\_RESETP\_}$	Minimum assertion time of RESETP_	0.2(1)	–	–	ms
$t_{fd\_RESETOUT\_}$	Delay between RESETP_ Asserted and RESETOUT_ Asserted	3	7	20	ns
$t_{rd\_RESETOUT\_}$	Delay between RESETP_ deasserted and RESETOUT_ deasserted	117.2	–	117.3	ms