Jz4725

Multimedia Application Processor

Data Sheet

Release Date: Jun. 2008

北京君正集成电路有限公司
Ingenic Semiconductor Co. Ltd

Jz4725 Multimedia Application Processor

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Release history

Date	Revision	Change
Jun. 2008	1.0	First version, pre-release

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Content

1 Overview

Jz4725 is a cost effective SOC solution for multimedia rich and mobile devices like video MP3, MP4 and PMP like products.

At the heart of Jz4725 is XBurst CPU core. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption.

The SIMD instruction set implemented by XBurst core, in together with the video post processing unit, provides RMVB, MPEG-1/2/4 decoding capability up to D1 resolution.

The memory interface of Jz4725 supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit ECC MLC NAND flash memory for cost sensitive applications.

On-chip modules such as LCD controller, audio CODEC, 2-channel SAR-ADC and AC97/I2S controller offer designers a rich suite of peripherals for multimedia application.

1.1 Block Diagram

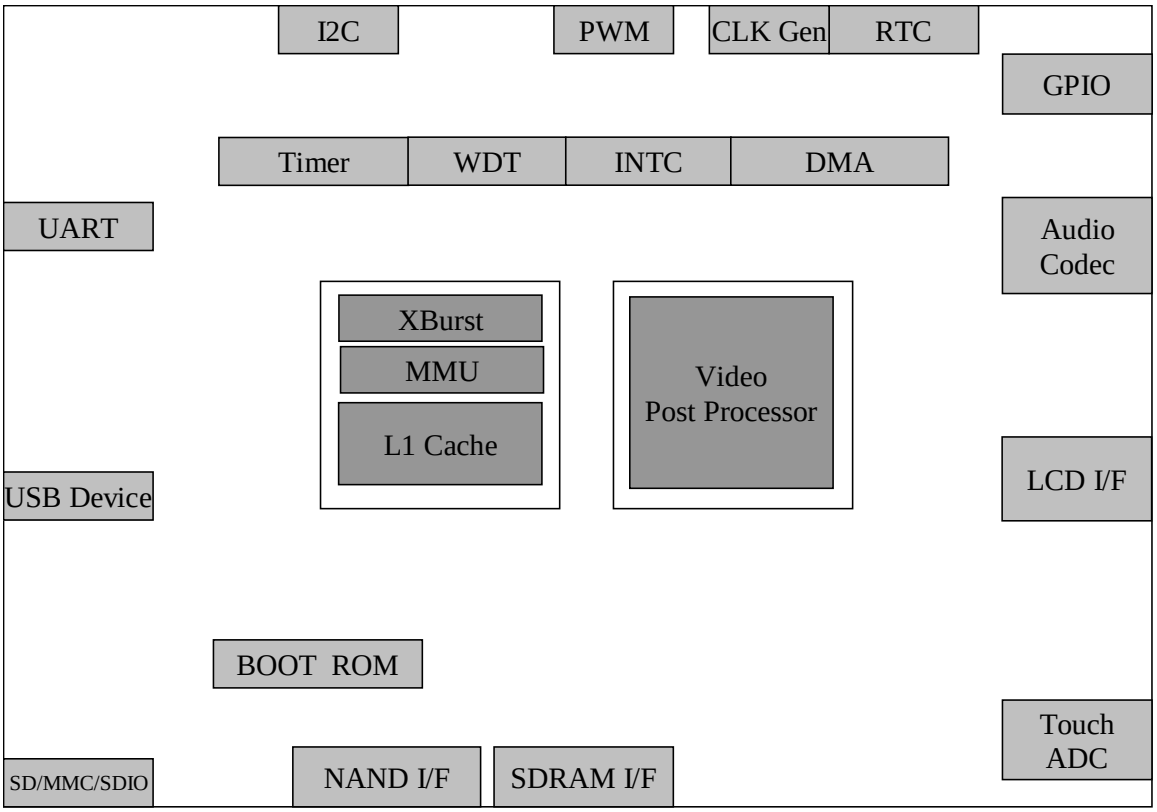


Figure 1-1 Jz4725 Diagram

1.2 Features

1.2.1 CPU core

- XBurst CPU
  - XBurst® RISC instruction set to support Linux and WinCE
  - XBurst® SIMD instruction set to support multimedia acceleration
  - XBurst® 8-stage pipeline micro-architecture up to 360MHz
- MMU
  - 32-entry dual-pages joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- Cache
  - 16K instruction cache
  - 16K data cache
- Hardware debug support

1.2.2 Multimedia support

- Video post processor
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert

1.2.3 Memory sub-system

- NAND Flash interface
  - Support MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Hamming Hardware ECC for 2 bit errors detection and 1 bit error correction
  - Reed-Solomon Hardware ECC for 4 9-bit-symbol errors detection and correction
  - Support automatic boot up from NAND Flash devices
  - Two chip select
- Synchronous DRAM Interface
  - 1 banks with programmable size and base address
  - 16-bit data bus width
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
- Direct Memory Access Controller
  - Six independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte

- Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
- Interrupt on transfer completion or transfer error
- Supports two transfer modes: single mode or block mode

- The Jz4725 processor system supports little endian only

1.2.4 Clock generation and power management

- On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
- On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
- PLL on/off is programmable by software
- ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
- Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.

1.2.5 Audio/Video Interface

- On-chip audio CODEC
  - 18-bit DAC, SNR: 88dB
  - 16-bit ADC, SNR: 85dB
  - Sample rate: 8/11.025/12/16/22.05/24/32/44.1/48kHz
  - L/R channels line input
  - MIC input
  - L/R channels headphone output amplifier support up to 32ohm load
- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 18 bit data bus support 1,2,4,8 pins STN panel, 16bit and 18bit TFT and 8bit I/F TFT
  - Display size up to 800×600 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)

1.2.6 On-chip peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is 81
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently

- Each pin can be configured as open-drain when output
- Each pin can be configured as internal resistor pull-up

- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
  - Total 28 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output
  - Provide five separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - PWM output supported
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset
- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 921.6Kbps baudrate
- USB 2.0 device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported
  - Embedded USB 2.0 PHY
- MMC/SD/SDIO controller
  - Compliant with “The MultiMediaCard System Specification version 3.3”

- Compliant with “SD Memory Card Specification version 1.01” and “SDIO Card Specification version 1.0” with 1 command channel and 1 data channels
- 5~20 Mbps maximum data rate
- Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status

- SADC
  - 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
  - Battery voltage input
  - 1 generic input Channel

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	LQFP 128 14mm * 14mm
Operating frequency	360MHz

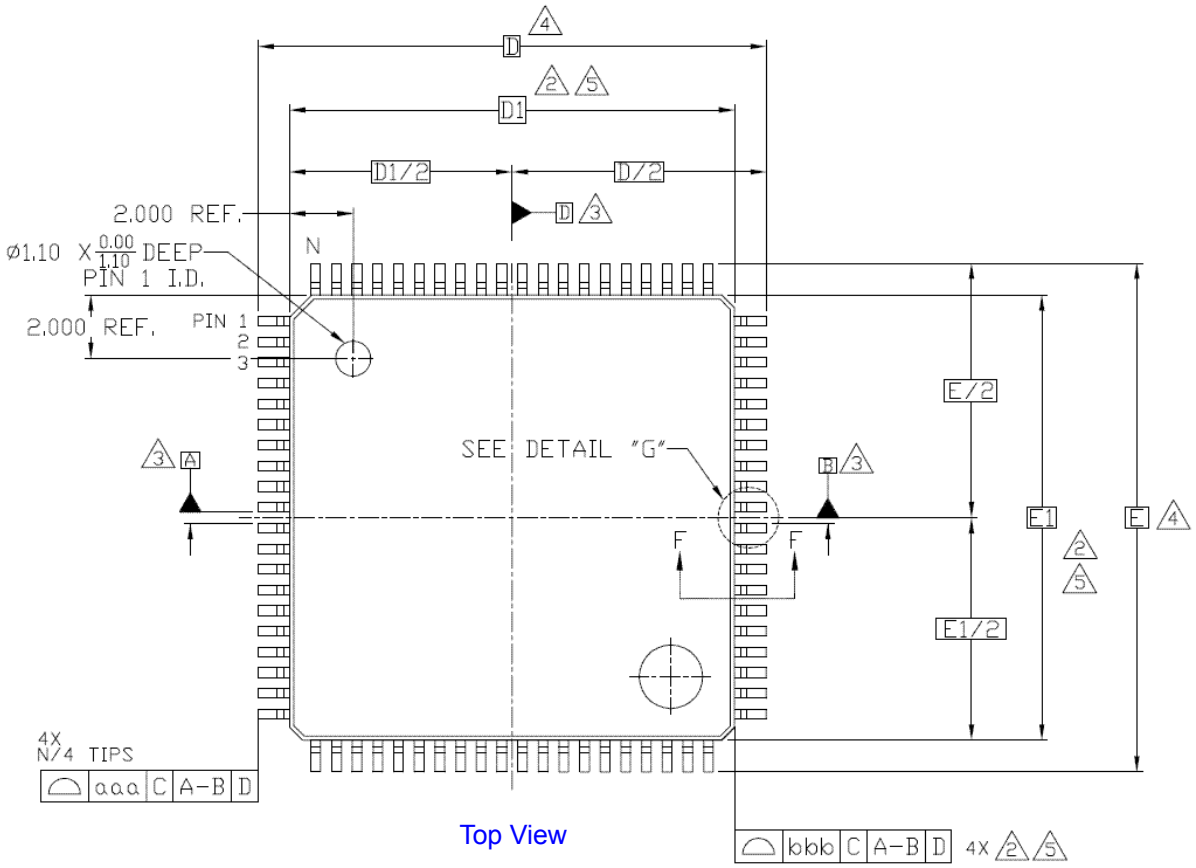
2 Packaging and Pinout Information

2.1 Overview

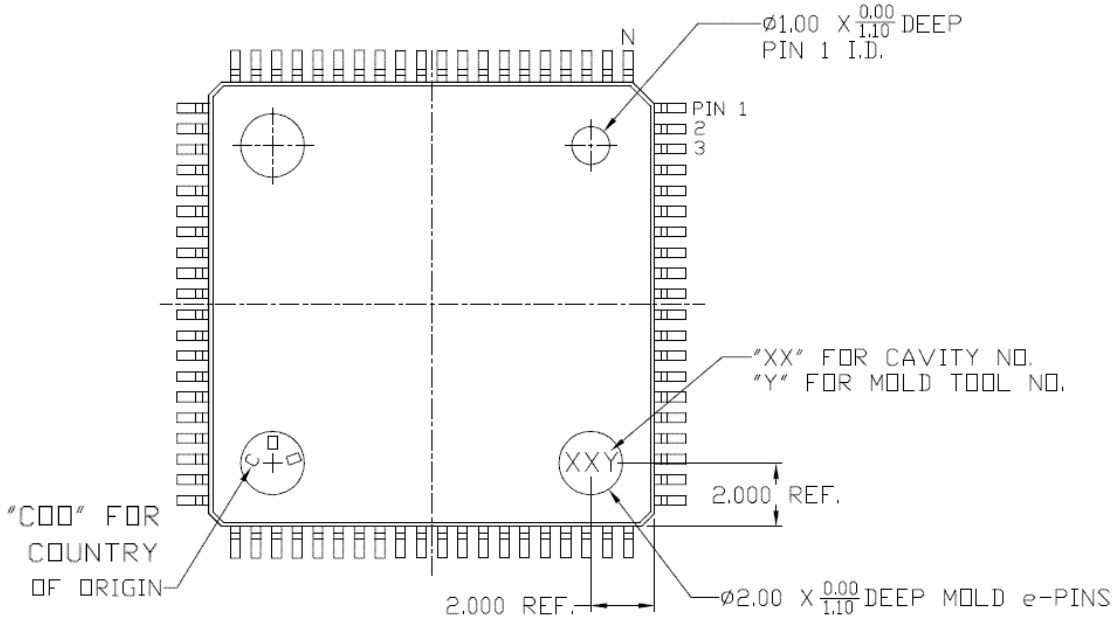
Jz4725 processor is offered in a LQFP128 package, which is 14mm x 14mm x 1.4mm outline 0.4mm pitch, show in “2.2 Package”.

The Jz4725 pin description is listed in Table 2-1 ~ Table 2-11.

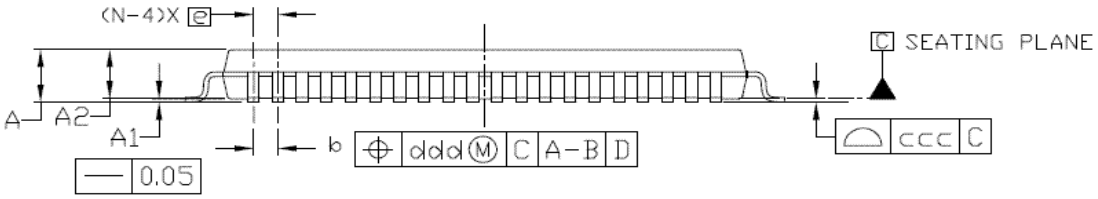
2.2 Package

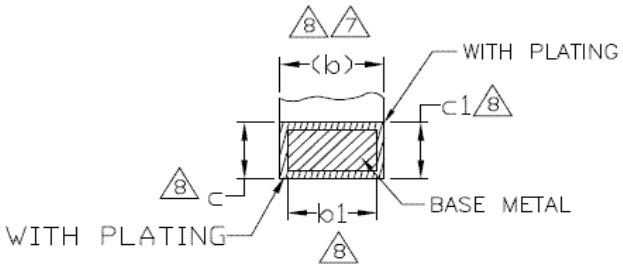


Top View

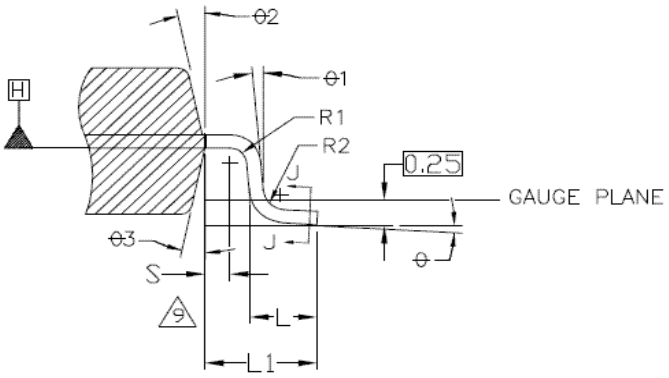


Bottom View

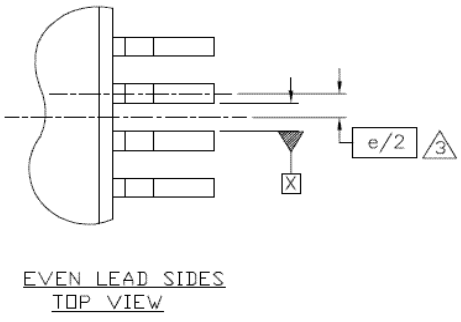




SECTION "J-J"
SCALE: NONE



SECTION "F-F"
SCALE: 3/1



EVEN LEAD SIDES
TOP VIEW

DETAIL "G"
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5-1994.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15 mm.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING DATUM PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 AND 0.5 mm PITCH PACKAGES.
8. THESE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
10. N IS THE MAXIMUM NUMBER OF LEADS.
11. THIS PRODUCT CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026 ISSUE D, VARIATIONS BEC AND BED..

SYMBOL		JEDEC VARIATIONS			NOTE
		BEC	BED		
b	MIN	0.22	0.17	0.13	
	NOM	0.32	0.22	0.18	
	MAX	0.38	0.27	0.23	
b1	MIN	0.22	0.17	0.13	
	NOM	0.30	0.20	0.16	8
	MAX	0.33	0.23	0.19	8
e		0.65 BSC	0.50 BSC	0.40 BSC	
N		80	100	128	
TOLERANCES OF FORM AND POSITION					
ccc		0.08	0.08	0.08	
ddd		0.13	0.08	0.07	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	--	--	1.60	
A1	0.05	--	0.15	9
A2	1.35	1.40	1.45	
D	16.00 BSC			
D1	14.00 BSC			
E	16.00 BSC			
E1	14.00 BSC			
θ	0°	3.5°	7°	
θ1	0°	5°	--	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
c	0.09	--	0.20	8
c1	0.09	0.127	0.16	8
L	0.45	0.60	0.75	
L1	1.00 REF.			
R1	0.08	--	--	
R2	0.08	--	0.20	
S	0.20	--	--	
TOLERANCES OF FORM AND POSITION				
aaa	0.20			
bbb	0.20			

2.3 Pin Description [1][2]

Table 2-1 EMC Pins (47; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	40	8mA, pullup-pe	D0: Memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO
D1 PA1	IO IO	41	8mA, pullup-pe	D1: Memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO
D2 PA2	IO IO	42	8mA, pullup-pe	D2: Memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO
D3 PA3	IO IO	43	8mA, pullup-pe	D3: Memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO
D4 PA4	IO IO	44	8mA, pullup-pe	D4: Memory data bus bit 4 PA4: GPIO group A bit 4	VDDIO
D5 PA5	IO IO	45	8mA, pullup-pe	D5: Memory data bus bit 5 PA5: GPIO group A bit 5	VDDIO
D6 PA6	IO IO	46	8mA, pullup-pe	D6: Memory data bus bit 6 PA6: GPIO group A bit 6	VDDIO
D7 PA7	IO IO	47	8mA, pullup-pe	D7: Memory data bus bit 7 PA7: GPIO group A bit 7	VDDIO
D8 PA8	IO IO	32	8mA, pullup-pe	D8: Memory data bus bit 8 PA8: GPIO group A bit 8	VDDIO
D9 PA9	IO IO	33	8mA, pullup-pe	D9: Memory data bus bit 9 PA9: GPIO group A bit 9	VDDIO
D10 PA10	IO IO	34	8mA, pullup-pe	D10: Memory data bus bit 10 PA10: GPIO group A bit 10	VDDIO
D11 PA11	IO IO	35	8mA, pullup-pe	D11: Memory data bus bit 11 PA11: GPIO group A bit 11	VDDIO
D12 PA12	IO IO	36	8mA, pullup-pe	D12: Memory data bus bit 12 PA12: GPIO group A bit 12	VDDIO
D13 PA13	IO IO	37	8mA, pullup-pe	D13: Memory data bus bit 13 PA13: GPIO group A bit 13	VDDIO
D14 PA14	IO IO	38	8mA, pullup-pe	D14: Memory data bus bit 14 PA14: GPIO group A bit 14	VDDIO
D15 PA15	IO IO	39	8mA, pullup-pe	D15: Memory data bus bit 15 PA15: GPIO group A bit 15	VDDIO
A0 PB0	O IO	8	12mA, pullup-pe	A0: Static/SDRAM memory address bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	7	12mA, pullup-pe	A1: Static/SDRAM memory address bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	6	12mA, pullup-pe	A2: Static/SDRAM memory address bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	5	12mA, pullup-pe	A3: Static/SDRAM memory address bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	29	12mA, pullup-pe	A4: Static/SDRAM memory address bit 4 PB4: GPIO group B bit 4	VDDIO
A5 PB5	O IO	28	12mA, pullup-pe	A5: Static/SDRAM memory address bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	27	12mA, pullup-pe	A6: Static/SDRAM memory address bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	26	12mA, pullup-pe	A7: Static/SDRAM memory address bit 7 PB7: GPIO group B bit 7	VDDIO
A8 PB8	O IO	23	12mA, pullup-pe	A8: Static/SDRAM memory address bit 8 PB8: GPIO group B bit 8	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A9 PB9	O IO	22	12mA, pullup-pe	A9: Static/SDRAM memory address bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	9	12mA, pullup-pe	A10: Static/SDRAM memory address bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	19	12mA, pullup-pe	A11: Static/SDRAM memory address bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	18	12mA, pullup-pe	A12: Static/SDRAM memory address bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	30	12mA, pullup-pe	A13: Static/SDRAM memory address bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	31	12mA, pullup-pe	A14: Static/SDRAM memory address bit 14 PB14: GPIO group B bit 14	VDDIO
A15 CL PB15	O O IO	50	2mA, pullup-pe	A15: Static memory address bit 15 CL: NAND flash command latch PB15: GPIO group B bit 15	VDDIO
A16 AL PB16	O O IO	49	2mA, pullup-pe	A16: Static memory address bit 16 AL: NAND flash address latch PB16: GPIO group B bit 16	VDDIO
DCS_ PB19	O IO	10	8mA, pullup-pe	DCS_: SDRAM chip select PB19: GPIO group B bit 19	VDDIO
RAS_ PB20	O IO	11	8mA, pullup-pe	RAS_: SDRAM row address strobe PB20: GPIO group B bit 20	VDDIO
CAS_ PB21	O IO	12	8mA, pullup-pe	CAS_: SDRAM column address strobe PB21: GPIO group B bit 21	VDDIO
SDWE_ & BUFD_ PB22	O IO	13	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB22: GPIO group B bit 22	VDDIO
CKE PB23	O IO	17	8mA, pullup-pe	CKE: SDRAM clock enable PB23: GPIO group B bit 23	VDDIO
CKO PB24	O IO	16	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CS1_ PB25	O IO	56	2mA, pullup-pe	CS1_: Static memory chip select 1 PB25: GPIO group B bit 25	VDDIO
CS2_ PB26	O IO	55	2mA, pullup-pe	CS2_: Static memory chip select 2 PB26: GPIO group B bit 26	VDDIO
WE0_ PB31	O IO	14	8mA, pullup-pe	WE0_: SDR/Static memory byte 0 write enable PB31: GPIO group B bit 31	VDDIO
WE1_ PC24	O IO	15	8mA, pullup-pe	WE1_: SDR/Static memory byte 1 write enable PC24: GPIO group C bit 24	VDDIO
WAIT_ PC27	I IO	54	2mA, Schmitt, pullup-pe	WAIT_: Slow static memory/device wait signal PC27: GPIO group C bit 27	VDDIO
FRE_ PC28	O IO	52	2mA, pullup-pe	FRE_: NAND flash read enable PC28: GPIO group C bit 28	VDDIO
FWE_ PC29	O IO	51	2mA, pullup-pe	FWE_: NAND flash write enable PC29: GPIO group C bit 29	VDDIO
PC30 (FRB)	IO	53	2mA, pullup-pe	PC30: GPIO group C bit 30. If NAND flash is used, it should connect to NAND FRB (NAND flash ready/busy)	VDDIO

Table 2-2 LCDC Pins (26; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_CLS A21 PB17	O O IO	103	4mA, pullup-pe	LCD_CLS: LCD CLS output A21: Static memory address bit 21 PB17: GPIO group B bit 17	VDDIO
LCD_SPL A22 PB18	O O IO	102	4mA, pullup-pe	LCD_SPL: LCD SPL output A22: Static memory address bit 22 PB18: GPIO group B bit 18	VDDIO
LCD_D0 PC0	O IO	1	4mA, pullup-pe	LCD_D0: LCD data bit 0 PC0: GPIO group C bit 0	VDDIO
LCD_D1 PC1	O IO	128	4mA, pullup-pe	LCD_D1: LCD data bit 1 PC1: GPIO group C bit 1	VDDIO
LCD_D2 PC2	O IO	127	4mA, pullup-pe	LCD_D2: LCD data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_D3 PC3	O IO	126	4mA, pullup-pe	LCD_D3: LCD data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_D4 PC4	O IO	124	4mA, pullup-pe	LCD_D4: LCD data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_D5 PC5	O IO	123	4mA, pullup-pe	LCD_D5: LCD data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_D6 PC6	O IO	122	4mA, pullup-pe	LCD_D6: LCD data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_D7 PC7	O IO	121	4mA, pullup-pe	LCD_D7: LCD data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_D8 PC8	O IO	120	4mA, pullup-pe	LCD_D8: LCD data bit 8 PC8: GPIO group C bit 8	VDDIO
LCD_D9 PC9	O IO	119	4mA, pullup-pe	LCD_D9: LCD data bit 9 PC9: GPIO group C bit 9	VDDIO
LCD_D10 PC10	O IO	118	4mA, pullup-pe	LCD_D10: LCD data bit 10 PC10: GPIO group C bit 10	VDDIO
LCD_D11 PC11	O IO	117	4mA, pullup-pe	LCD_D11: LCD data bit 11 PC11: GPIO group C bit 11	VDDIO
LCD_D12 PC12	O IO	116	4mA, pullup-pe	LCD_D12: LCD data bit 12 PC12: GPIO group C bit 12	VDDIO
LCD_D13 PC13	O IO	115	4mA, pullup-pe	LCD_D13: LCD data bit 13 PC13: GPIO group C bit 13	VDDIO
LCD_D14 PC14	O IO	114	4mA, pullup-pe	LCD_D14: LCD data bit 14 PC14: GPIO group C bit 14	VDDIO
LCD_D15 PC15	O IO	113	4mA, pullup-pe	LCD_D15: LCD data bit 15 PC15: GPIO group C bit 15	VDDIO
LCD_D16 PC16	O IO	112	4mA, pullup-pe	LCD_D16: LCD data bit 16 PC20: GPIO group C bit 16	VDDIO
LCD_D17 PC17	O IO	111	4mA, pullup-pe	LCD_D17: LCD data bit 17 PC17: GPIO group C bit 17	VDDIO
LCD_PCLK PC18	IO IO	2	4mA, pullup-pe	LCD_PCLK: LCD pixel clock PC18: GPIO group C bit 18	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_HSYNC PC19	IO IO	109	4mA, pullup-pe	LCD_HSYNC: LCD line clock/horizonal sync PC19: GPIO group C bit 19	VDDIO
LCD_VSYNC PC20	IO IO	108	4mA, pullup-pe	LCD_VSYNC: LCD frame clock/vertical sync PC20: GPIO group C bit 20	VDDIO
LCD_DE PC21	O IO	110	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC21: GPIO group C bit 21	VDDIO
LCD_PS A19 PC22	O O IO	107	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT A19: Static memory address bit 19 PC22: GPIO group C bit 22	VDDIO
LCD_REV A20 PC23	O O IO	105	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT A20: Static memory address bit 20 PC23: GPIO group C bit 23	VDDIO

Table 2-3 USB device 2.0 and host 1.1 Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DP0	AIO	79		DP0: USB 2.0 device data plus	VDD_{USB}
DM0	AIO	78		DM0: USB 2.0 device data minus	VDD_{USB}
RREF	AIO	76		RREF: External Reference for USB 2.0 device. Connect a 2.5kΩ external reference resistor, with 5% tolerance to analog ground VSSUSB	VDD_{USB}
VDDA	AIO	75		VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground VSSUSB	VDD_{USB}
VDDUSB	P	77		VDDUSB: USB analog power, 3.3V	-
VSSUSB	P	80		VSSUSB: USB analog ground	-

Table 2-4 TCU/I2C/UART Pins (5; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 I2C_SDA PD23	O IO IO	60	4mA, pullup-pe	PWM0: PWM 0 output I2C_SDA: I2C serial data PD23: GPIO group D bit 23	VDDIO
PWM1 I2C_SCK PD24	O IO IO	59	4mA, pullup-pe	PWM1: PWM 1 output I2C_SCK: I2C serial clock PD24: GPIO group D bit 24	VDDIO
PWM2 UART0_TxD PD25	O O IO	58	2mA, pullup-pe	PWM2: PWM 2 output UART0_TxD: UART 0 transmitting data PD25: GPIO group D bit 25	VDDIO
PWM3 UART0_RxD PD26	O I IO	57	2mA, pullup-pe	PWM3: PWM 3 output UART0_RxD: UART 0 Receiving data PD26: GPIO group D bit 26	VDDIO
PWM5 A18 PD28	O O IO	48	2mA, pullup-pe	PWM5: PWM 5 output A18: Static memory address bit 18 PD28: GPIO group D bit 28	VDDIO

Table 2-5 SAR ADC Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PBAT/ADIN0	AI	67		ADIN0: Battery voltage input or ADC general purpose input 0	VDD_{ADC}
ADIN1	AI	68		ADIN1: ADC general purpose input 1	VDD_{ADC}
VDDADC	P	70		VDDADC: ADC analog power, 3.3 V	-
VSSADC	P	69		VDDADC: ADC analog ground	-

Table 2-6 Audio CODEC Pins (13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LHPO	AO	90		LHPO: Left headphone out	VDD_{CDC}
RHPO	AO	88		RHPO: Right headphone out	VDD_{CDC}
MICIN	AI	99		MICIN: Microphone input	VDD_{CDC}
LLINEIN	AI	97		LLINEIN: Left line input	VDD_{CDC}
RLINEIN	AI	98		RLINEIN: Right line input	VDD_{CDC}
VREF	AO	94		VREF: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to VSSCDC eliminates the effects of high frequency noise	VDD_{CDC}
VDDHP	P	87		VDDHP: Headphone amplifier power, 3.3V	-
VSSHP	P	89		VSSHP: Headphone amplifier ground	-
VDDLHP	P	91		VDDLHP: Headphone amplifier power, 3.3V	-
VDDCDC	P	93		VDDCDC: CODEC analog power, 3.3V	-
VSSCDC	P	92		VSSCDC: CODEC analog ground	-
VDDCDC2	P	95		VDDCDC: CODEC analog power, 3.3V	-
VSSCDC2	P	96		VSSCDC: CODEC analog ground	-

Table 2-7 MSC (MMC/SD) Pins (3; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC_D0 PD10	IO IO	61	4mA, pullup-pe	MSC_D0: MSC data bit 0 PD10: GPIO group D bit 10	VDDIO
MSC_CMD PD08	IO IO	63	4mA, pullup-pe	MSC_CMD: MSC command PD08: GPIO group D bit 8	VDDIO
MSC_CLK PD09	O IO	62	4mA, pullup-pe	MSC_CLK: MSC clock output PD09: GPIO group D bit 9	VDDIO

Table 2-8 CPM Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	64	10~20 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	65		EXCLKO: OSC output	VDDIO
VDDPLL	P	73		VDDPLL: PLL digital power, 1.8V	-
VSSPLL	P	74		VSSPLL: PLL digital ground	-
AVDDPLL	P	71		AVDDPLL: PLL analog power, 1.8V	
AVSSPLL	P	72		AVSSPLL: PLL analog ground	

Table 2-9 RTC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	81	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	82		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	AO	86	~2mA, open-drain	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PD29	AI AI	85	Schmitt	WKUP_: Wake signal after main power down PD29: GPIO group D bit 29, input/interrupt only	VDD_{RTC}
PPRST_	AI	84	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	83		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

Table 2-10 System Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
BOOT_SEL0	I	101	Schmitt	BOOT_SEL0: Boot select bit 0	VDDIO
BOOT_SEL1	I	100	Schmitt	BOOT_SEL1: Boot select bit 1	VDDIO

Table 2-11 IO/Core power supplies (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO	P	24, 66, 104		VDDIO: 3+1 IO digital power, 3.3V	-
VSS	P	3, 20, 25, 106, 125		VSS: 5+4 IO/CORE digital ground	-
VDDCORE	P	4, 21		VDDCORE: 2+2 CORE digital power, 1.8V	-

Notes:

[1]. The meaning of phrases in IO cell characteristics are

a) 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12mA
b) Pull-up: The IO cell contains a pull-up resistor
c) Pull-down: The IO cell contains a pull-down resistor
d) Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
e) Schmitt: The IO cell is Schmitt trig input

[2]. For any GPIO shared pin except WAIT_/PC27 and CKO/PB24, the reset state is GPIO input with internal pull-up. The WAIT_/PC27 and CKO/PB24 are initialed to WAIT_ and CKO functions with internal pull-up.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
VDDUSB power supplies voltage	-0.3	3.9	V
VDDCDC power supplies voltage	-0.3	4.0	V
VDDHP power supplies voltage	-0.3	4.0	V
VDDADC power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to VDDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to VDDADC supplied non-supply pins except PBAT	-0.5	4.0	V
Input voltage of PBAT	-0.5	6.0	V
Input voltage to VDDCDC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from VDDADC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDCDC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{USB}	VDDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	VDDCDC voltage	3.0	3.3	3.6	V
V_{HP}	VDDHP voltage	3.0	3.3	3.6	V
V_{ADC}	VDDADC voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-IO}	Input high voltage	2.0		3.6	V
V_{IL-IO}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-UF}	Input voltage range for full speed applications	0		V_{USB}	V
V_{I-UH}	Input voltage range for high speed applications	120		400	mV

Table 3-5 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{I-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V
V_{I-TSC}	XN/XP/YN/YP input voltage range	0		V_{ADC}	

Table 3-6 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-RTC}	Input high voltage	2.0		3.6	V
V_{IL-RTC}	Input low voltage	-0.3		0.8	V

Table 3-7 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-8 DC characteristics for VDDIO supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point		1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point		0.88	0.94	0.99	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		50	65	100	kΩ
R_{PD}	Pull-down Resistor		40	56	107	kΩ
C_{IO}	Capacitance of the pins		4	5	10	pF
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.4V for cells of	2mA	2.2	3.7	4.6	mA
		4mA	4.4	7.4	9.2	mA
		8mA	8.9	14.7	18.4	mA
		12mA	13.3	22.1	27.5	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = 2.4V for cells of	2mA	2.5	5.1	7.9	mA
		4mA	5.0	10.2	15.9	mA
		8mA	10.0	20.4	31.7	mA
		12mA	15.0	30.6	47.6	mA

Table 3-9 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-U20}	Output high voltage	1.5		V_{USB}	V
V_{OL-U20}	Output low voltage	0		0.4	V

Table 3-10 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
R_{BAT}	BAT input resister		9.3		kΩ

Table 3-11 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit

V_{OH-RTC}	Output high voltage	2.0		3.6	V
V_{OL-RTC}	Output low voltage	-0.3		0.8	V

3.4 Characteristics of CODEC

Table 3-12 CODEC characteristics

Parameter	Conditions	Min	Typical	Max	Unit
S/N (A-weighted)-DAC	Note 1		90		dB
S/N (A-weighted)-ADC	Note 1		85		dB
Dynamic range (A-weighted) @-60dB	Fin@1kHz		90		dB
THD+N (A-weighted) @-6dB-DAC	Note 2				dB
THD+N (A-weighted) @-6dB-ADC	Note 3	70			dB
Inter-channel isolation	Fin@1kHz		60		dB
Inter-channel gain mismatch			0.1	0.2	dB
Closed loop gain			0		dB
Load resistance for HPOUTL & HPOUTR		32			Ω
Power supply rejection @ 200Hz			60		dB
Passband		0		0.42	fs
Passband ripple				±0.1	dB
Stopband		0.58			fs
Stopband attenuation		76			dB
LLINEIN/MIC resistance			40		KΩ
LLINEIN/MIC input range			1.6		Vp-p
MICBIAS voltage			2/3Avd		V
MICBIAS drive current			2		mA
HPOUT output peak value			1.8		Vp-p
Analog supply voltage		3.0	3.3	3.6	V
Digital supply voltage		1.62	1.8	1.98	V
Standby current			3		uA
Power Consumption (no tone)	DAC enable		28		mW
	ADC enable		34		mW
	ADC/DAC enable		62		mW

Note:

1. The ratio of the rms output level with 1KHz full-scale input to the rms output noise level. Measured “A-weighted” over a 20Hz to 0.44Fs bandwidth.
2. The ratio of the rms value of the signal to the rms sum of all the spectral components less than 0.44Fs bandwidth, including distortion components, tested at -6dB input. The headphone output THD+N>= 70dB under 32Ohm/16Ohm loading.

3.5 Power Consumption Specifications

Power consumption depends on the operating frequency, operating voltage, program used which determines internal and external switching activities, external loading and even environment ambient. The typical power consumption of both dynamic and static for the Jz4725 processor are provided here.

Table 3-13 PLL (VDD_{PLL}) Dynamic Power Consumption

Conditions	PLL out	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL input clock = 12MHz	240MHz	6.1	mA
	360MHz	9.1	mA

Table 3-14 PLL (VDD_{PLL}) Static Power Consumption

Conditions	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL is in suspend mode	0.1	uA

Table 3-15 RTC (VDD_{RTC}) Dynamic Power Consumption

Conditions	Typical	Unit
VDDRTC = 3.3V, RTCLK = 32768Hz oscillator, Temperature = room	1.8	uA

Table 3-16 IO (VDD_{IO}) Dynamic Power Consumption

Conditions	SDRAM Clock	Typical	Unit
VDDIO = 3.3V, VDDcore = 1.8V, Temperature = room, 16-bit SDRAM, LCD run in 320 x 240 x 60, EXCLK = 12MHz oscillator, CPU clock is 3 times of SDRAM clock, run media program in Linux	80MHz	TBD	mA
	120MHz	TBD	mA

Note: IO dynamic power is greatly depends on the software environment and the hardware (board and other components) environment.

Table 3-17 IO (VDD_{IO}) Static Power Consumption

Conditions	Typical	Unit
VDDIO = 3.3V, VDDcore = 1.8V, Temperature = room, oscillator stopped, No input floating, the pull-up/down is in same direction as the driving	0.05	uA

Table 3-18 CORE (VDD_{CORE}) Dynamic Power Consumption

Conditions	CPU Clock	Typical	Unit
VDDcore = 1.8V, Temperature = room, 16-bit SDRAM, LCD	240MHz	TBD	mA

run in 320 x 240 x 60, EXCLK = 12MHz oscillator, SDRAM clock is 1/3 of CPU clock, run GCC or media program in Linux	360MHz	TBD	mA

Note: CORE dynamic power is greatly depends on the software environment.

Table 3-19 CORE (VDD_{CORE}) Static Power Consumption

Conditions	Typical	Unit
VDDcore = 1.8V, Temperature = room, EXCLK oscillator stopped, all clocks exception RTCLK are stopped	75	uA

Table 3-20 CODEC (VDD_{CDC} + VDD_{HP}) Dynamic Power Consumption

Conditions		Typical	Unit
VDDCDC = VDDHP = 3.3V, Temperature = room, 220uF capacitors, 32Ω headphone load, 48k sample rate, stereo	Replay all zero samples	11.8	mA
	Replay full scale 1k sine wave	36.3	mA
	Typical replay	17.7	mA
	Typical record	11.4	mA

Table 3-21 CODEC (VDD_{CDC} + VDD_{HP}) Static Power Consumption

Conditions	Typical	Unit
VDDCDC = VDDHP = 3.3V, Temperature = room, CODEC is in suspend mode	0.03	uA

Table 3-22 USB (VDD_{USB}) Dynamic Power Consumption

Conditions	Typical	Unit
TBD	TBD	mA

Table 3-23 USB (VDD_{USB}) Static Power Consumption

Conditions	Typical	Unit
VDDUSB = 3.3V, Temperature = room, USB 2.0 device and USB 1.1 host are in suspend mode	0.03	uA

Table 3-24 ADC (VDD_{ADC}) Dynamic Power Consumption

Conditions	Typical	Unit
TBD	TBD	mA

Table 3-25 ADC (VDD_{ADC}) Static Power Consumption

Conditions	Typical	Unit
VDDADC = 3.3V, Temperature = room, ADC is in suspend mode	0.03	uA

3.6 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768KHz oscillator and a EXCLK oscillator. When choosing a crystal, match the crystal parameters as closely as possible.

3.7 Power On, Reset and BOOT

3.7.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the Jz4725 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-26.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VDDRTC
2. VDDA: VDDCDC, VDDHP
3. All other 3.3V VDDs (VDD33): VDDIO, VDDADC, VDDUSB
4. All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

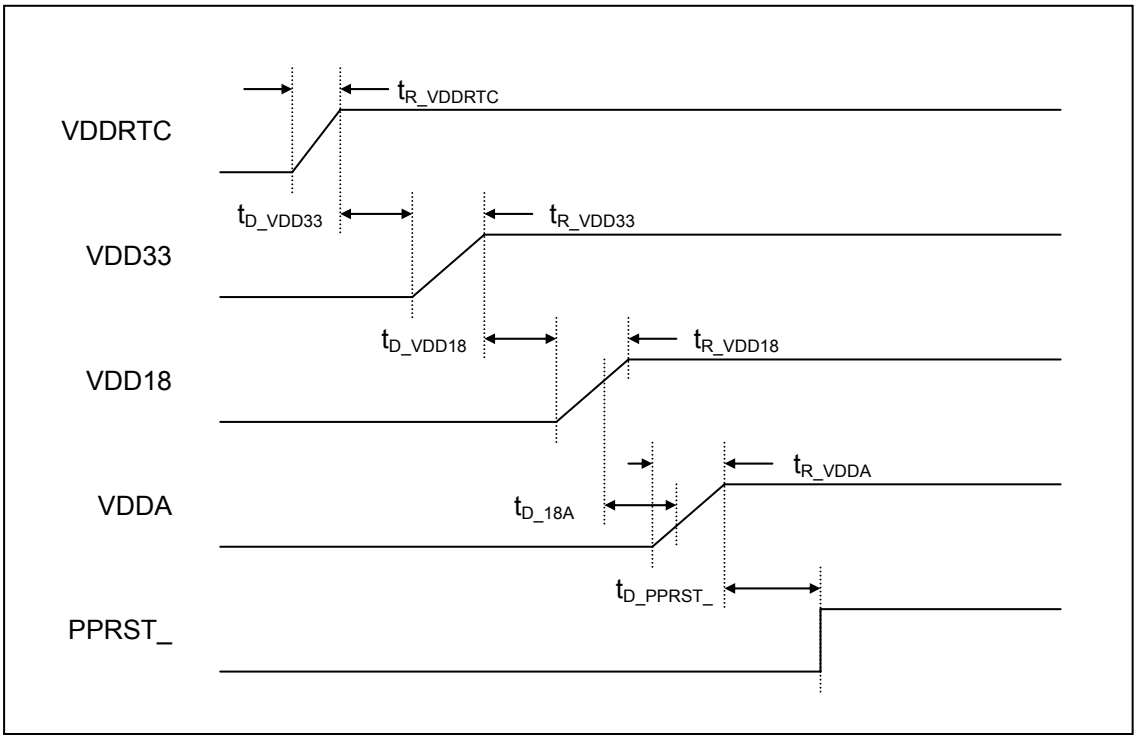


Figure 3-1 Power-On Timing Diagram

Table 3-26 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33 applies	$-t_{R\_VDDRTC}$	–	–	ms[1]

t_{R_VDD33}	VDD33 rise/stabilization time	0	–	100	ms
t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	$-t_{R\_VDD33}/2$	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0	–	100	ms
t_{D_18A}	Delay between VDD18 (actually VDDcore) arriving 1.5V and VDDA arriving 1V	0.01	–	10	ms
t_{R_VDDA}	VDDA rise/stabilization time	0	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDDA stable and PPRST_ deasserted	20	–	–	ms

Note:

1. VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.
2. VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.7.2 Reset procedure

There 3 reset sources: (1) PPRST_ pin reset; (2) WDT timeout reset; and (3) hibernating reset when exiting hibernating mode. After reset, program start from boot.

(1) PPRST_ pin reset

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is a few RTCLK cycles after rising edge of PPRST_.

(2) WDT reset

This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

(3) Hibernating reset

This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except WAIT_ pin, are put to GPIO input function with the internal pull-up set to on. The WAIT_ pin is set to wait function with the internal pull-up set to on. The PWRON_ is output 0. The 32768Hz/12MHz oscillators are on. The JTAG/UART is put to JTAG function and the TDO is output high-Z (suppose TRST_ is 0). The analog devices, the USB 2.0 PHY, USB 1.1 PHY, the CODEC DAC/ADC and the SAR-ADCs, are put in suspend mode.

3.7.3 BOOT

Jz4725 support 2 different boot sources depending on BOOT_SEL0 and BOOT_SEL1 pin values. Table 3-27 lists them.

Table 3-27 Boot from 2 boot sources

BOOT_SEL1	BOOT_SEL0	Boot Source
0	0	Not used
0	1	Boot from USB device
1	0	Boot from 512 page NAND flash at CS1
1	1	Boot from 2k page NAND flash at CS1

When Jz4725 BOOT from NAND at CS1_, some of the memory interface pins are set to function pin from the default GPIO pin and are used in executing BOOT ROM instructions. When BOOT from USB, none of any pins are used. Table 3-28 lists the cases.

Table 3-28 Pins are used and are set to function pins during BOOT

Boot Source Condition	GPIO pin state changed from RESET
USB	None
8-bits NAND flash at CS1_	CLE(PB15); ALE(PB16); CS1_(PB25); FRE(PC28); FEW(PC29); FRB(PC30); SDWE_/BUFD_ (PB22); D0~D7(PA0~PA7)
16-bits NAND flash at CS1_	CLE(PB15); ALE(PB16); CS1_(PB25); FRE(PC28); FEW(PC29); FRB(PC30); SDWE_/BUFD_ (PB22); D0~D15(PA0~PA15)