V2➔V3 Change notes (remove 2 GPIO pins and add PWRON_/WKUP_ pins to enable RTC):

Remove 2 pins: PD20 (SSI_DT), PD21 (SSI_DR)

Add 2 pins: PWRON_, WKUP_(PD29)

Pin number between 64~86 changed

1 Packaging and Pinout Information

1.1 Pin Description [1][2]

Table 1-1 EMC Pins (47; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	40	8mA, pullup-pe	D0: Memory data bus bit 0 PA0: GPIO group A bit 0	VDDIO
D1 PA1	IO IO	41	8mA, pullup-pe	D1: Memory data bus bit 1 PA1: GPIO group A bit 1	VDDIO
D2 PA2	IO IO	42	8mA, pullup-pe	D2: Memory data bus bit 2 PA2: GPIO group A bit 2	VDDIO
D3 PA3	IO IO	43	8mA, pullup-pe	D3: Memory data bus bit 3 PA3: GPIO group A bit 3	VDDIO
D4 PA4	IO IO	44	8mA, pullup-pe	D4: Memory data bus bit 4 PA4: GPIO group A bit 4	VDDIO
D5 PA5	IO IO	45	8mA, pullup-pe	D5: Memory data bus bit 5 PA5: GPIO group A bit 5	VDDIO
D6 PA6	IO IO	46	8mA, pullup-pe	D6: Memory data bus bit 6 PA6: GPIO group A bit 6	VDDIO
D7 PA7	IO IO	47	8mA, pullup-pe	D7: Memory data bus bit 7 PA7: GPIO group A bit 7	VDDIO
D8 PA8	IO IO	32	8mA, pullup-pe	D8: Memory data bus bit 8 PA8: GPIO group A bit 8	VDDIO
D9 PA9	IO IO	33	8mA, pullup-pe	D9: Memory data bus bit 9 PA9: GPIO group A bit 9	VDDIO
D10 PA10	IO IO	34	8mA, pullup-pe	D10: Memory data bus bit 10 PA10: GPIO group A bit 10	VDDIO
D11 PA11	IO IO	35	8mA, pullup-pe	D11: Memory data bus bit 11 PA11: GPIO group A bit 11	VDDIO
D12 PA12	IO IO	36	8mA, pullup-pe	D12: Memory data bus bit 12 PA12: GPIO group A bit 12	VDDIO
D13 PA13	IO IO	37	8mA, pullup-pe	D13: Memory data bus bit 13 PA13: GPIO group A bit 13	VDDIO
D14 PA14	IO IO	38	8mA, pullup-pe	D14: Memory data bus bit 14 PA14: GPIO group A bit 14	VDDIO
D15 PA15	IO IO	39	8mA, pullup-pe	D15: Memory data bus bit 15 PA15: GPIO group A bit 15	VDDIO
A0 PB0	O IO	8	12mA, pullup-pe	A0: Static/SDRAM memory address bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	7	12mA, pullup-pe	A1: Static/SDRAM memory address bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	6	12mA, pullup-pe	A2: Static/SDRAM memory address bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	5	12mA, pullup-pe	A3: Static/SDRAM memory address bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	29	12mA, pullup-pe	A4: Static/SDRAM memory address bit 4 PB4: GPIO group B bit 4	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A5 PB5	O IO	28	12mA, pullup-pe	A5: Static/SDRAM memory address bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	27	12mA, pullup-pe	A6: Static/SDRAM memory address bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	26	12mA, pullup-pe	A7: Static/SDRAM memory address bit 7 PB7: GPIO group B bit 7	VDDIO
A8 PB8	O IO	23	12mA, pullup-pe	A8: Static/SDRAM memory address bit 8 PB8: GPIO group B bit 8	VDDIO
A9 PB9	O IO	22	12mA, pullup-pe	A9: Static/SDRAM memory address bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	9	12mA, pullup-pe	A10: Static/SDRAM memory address bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	19	12mA, pullup-pe	A11: Static/SDRAM memory address bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	18	12mA, pullup-pe	A12: Static/SDRAM memory address bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	30	12mA, pullup-pe	A13: Static/SDRAM memory address bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	31	12mA, pullup-pe	A14: Static/SDRAM memory address bit 14 PB14: GPIO group B bit 14	VDDIO
A15 CL PB15	O O IO	50	2mA, pullup-pe	A15: Static memory address bit 15 CL: NAND flash command latch PB15: GPIO group B bit 15	VDDIO
A16 AL PB16	O O IO	49	2mA, pullup-pe	A16: Static memory address bit 16 AL: NAND flash address latch PB16: GPIO group B bit 16	VDDIO
DCS_ PB19	O IO	10	8mA, pullup-pe	DCS_: SDRAM chip select PB19: GPIO group B bit 19	VDDIO
RAS_ PB20	O IO	11	8mA, pullup-pe	RAS_: SDRAM row address strobe PB20: GPIO group B bit 20	VDDIO
CAS_ PB21	O IO	12	8mA, pullup-pe	CAS_: SDRAM column address strobe PB21: GPIO group B bit 21	VDDIO
SDWE_ & BUFD_ PB22	O IO	13	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB22: GPIO group B bit 22	VDDIO
CKE PB23	O IO	17	8mA, pullup-pe	CKE: SDRAM clock enable PB23: GPIO group B bit 23	VDDIO
CKO PB24	O IO	16	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CS1_ PB25	O IO	56	2mA, pullup-pe	CS1_: Static memory chip select 1 PB25: GPIO group B bit 25	VDDIO
CS2_ PB26	O IO	55	2mA, pullup-pe	CS2_: Static memory chip select 2 PB26: GPIO group B bit 26	VDDIO
WE0_ PB31	O IO	14	8mA, pullup-pe	WE0_: SDR/Static memory byte 0 write enable PB31: GPIO group B bit 31	VDDIO
WE1_ PC24	O IO	15	8mA, pullup-pe	WE1_: SDR/Static memory byte 1 write enable PC24: GPIO group C bit 24	VDDIO
WAIT_ PC27	I IO	54	2mA, Schmitt, pullup-pe	WAIT_: Slow static memory/device wait signal PC27: GPIO group C bit 27	VDDIO
FRE_ PC28	O IO	52	2mA, pullup-pe	FRE_: NAND flash read enable PC28: GPIO group C bit 28	VDDIO
FWE_ PC29	O IO	51	2mA, pullup-pe	FWE_: NAND flash write enable PC29: GPIO group C bit 29	VDDIO
PC30 (FRB)	IO	53	2mA, pullup-pe	PC30: GPIO group C bit 30. If NAND flash is used, it should connect to NAND FRB (NAND flash ready/busy)	VDDIO

Table 1-2 LCDC Pins (26; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_CLS A21 PB17	O O IO	103	4mA, pullup-pe	LCD_CLS: LCD CLS output A21: Static memory address bit 21 PB17: GPIO group B bit 17	VDDIO
LCD_SPL A22 PB18	O O IO	102	4mA, pullup-pe	LCD_SPL: LCD SPL output A22: Static memory address bit 22 PB18: GPIO group B bit 18	VDDIO
LCD_D0 PC0	O IO	1	4mA, pullup-pe	LCD_D0: LCD data bit 0 PC0: GPIO group C bit 0	VDDIO
LCD_D1 PC1	O IO	128	4mA, pullup-pe	LCD_D1: LCD data bit 1 PC1: GPIO group C bit 1	VDDIO
LCD_D2 PC2	O IO	127	4mA, pullup-pe	LCD_D2: LCD data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_D3 PC3	O IO	126	4mA, pullup-pe	LCD_D3: LCD data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_D4 PC4	O IO	124	4mA, pullup-pe	LCD_D4: LCD data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_D5 PC5	O IO	123	4mA, pullup-pe	LCD_D5: LCD data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_D6 PC6	O IO	122	4mA, pullup-pe	LCD_D6: LCD data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_D7 PC7	O IO	121	4mA, pullup-pe	LCD_D7: LCD data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_D8 PC8	O IO	120	4mA, pullup-pe	LCD_D8: LCD data bit 8 PC8: GPIO group C bit 8	VDDIO
LCD_D9 PC9	O IO	119	4mA, pullup-pe	LCD_D9: LCD data bit 9 PC9: GPIO group C bit 9	VDDIO
LCD_D10 PC10	O IO	118	4mA, pullup-pe	LCD_D10: LCD data bit 10 PC10: GPIO group C bit 10	VDDIO
LCD_D11 PC11	O IO	117	4mA, pullup-pe	LCD_D11: LCD data bit 11 PC11: GPIO group C bit 11	VDDIO
LCD_D12 PC12	O IO	116	4mA, pullup-pe	LCD_D12: LCD data bit 12 PC12: GPIO group C bit 12	VDDIO
LCD_D13 PC13	O IO	115	4mA, pullup-pe	LCD_D13: LCD data bit 13 PC13: GPIO group C bit 13	VDDIO
LCD_D14 PC14	O IO	114	4mA, pullup-pe	LCD_D14: LCD data bit 14 PC14: GPIO group C bit 14	VDDIO
LCD_D15 PC15	O IO	113	4mA, pullup-pe	LCD_D15: LCD data bit 15 PC15: GPIO group C bit 15	VDDIO
LCD_D16 PC16	O IO	112	4mA, pullup-pe	LCD_D16: LCD data bit 16 PC20: GPIO group C bit 16	VDDIO
LCD_D17 PC17	O IO	111	4mA, pullup-pe	LCD_D17: LCD data bit 17 PC17: GPIO group C bit 17	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_PCLK PC18	IO IO	2	4mA, pullup-pe	LCD_PCLK: LCD pixel clock PC18: GPIO group C bit 18	VDDIO
LCD_HSYNC PC19	IO IO	109	4mA, pullup-pe	LCD_HSYNC: LCD line clock/horizonal sync PC19: GPIO group C bit 19	VDDIO
LCD_VSYNC PC20	IO IO	108	4mA, pullup-pe	LCD_VSYNC: LCD frame clock/vertical sync PC20: GPIO group C bit 20	VDDIO
LCD_DE PC21	O IO	110	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC21: GPIO group C bit 21	VDDIO
LCD_PS A19 PC22	O O IO	107	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT A19: Static memory address bit 19 PC22: GPIO group C bit 22	VDDIO
LCD_REV A20 PC23	O O IO	105	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT A20: Static memory address bit 20 PC23: GPIO group C bit 23	VDDIO

Table 1-3 USB device 2.0 and host 1.1 Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DP0	AIO	79		DP0: USB 2.0 device data plus	VDD_{USB}
DM0	AIO	78		DM0: USB 2.0 device data minus	VDD_{USB}
RREF	AIO	76		RREF: External Reference for USB 2.0 device. Connect a 2.5kΩ external reference resistor, with 5% tolerance to analog ground VSSUSB	VDD_{USB}
VDDA	AIO	75		VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground VSSUSB	VDD_{USB}
VDDUSB	P	77		VDDUSB: USB analog power, 3.3V	-
VSSUSB	P	80		VSSUSB: USB analog ground	-

Table 1-4 TCU/I2C/UART Pins (5; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 I2C_SDA PD23	O IO IO	60	4mA, pullup-pe	PWM0: PWM 0 output I2C_SDA: I2C serial data PD23: GPIO group D bit 23	VDDIO
PWM1 I2C_SCK PD24	O IO IO	59	4mA, pullup-pe	PWM1: PWM 1 output I2C_SCK: I2C serial clock PD24: GPIO group D bit 24	VDDIO
PWM2 UART0_TxD PD25	O O IO	58	2mA, pullup-pe	PWM2: PWM 2 output UART0_TxD: UART 0 transmitting data PD25: GPIO group D bit 25	VDDIO
PWM3 UART0_RxD PD26	O I IO	57	2mA, pullup-pe	PWM3: PWM 3 output UART0_RxD: UART 0 Receiving data PD26: GPIO group D bit 26	VDDIO
PWM5 A18 PD28	O O IO	48	2mA, pullup-pe	PWM5: PWM 5 output A18: Static memory address bit 18 PD28: GPIO group D bit 28	VDDIO

Table 1-5 SAR ADC Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PBAT/ADIN0	AI	67		ADIN0: Battery voltage input or ADC general purpose input 0	VDD_{ADC}
ADIN1	AI	68		ADIN1: ADC general purpose input 1	VDD_{ADC}
VDDADC	P	70		VDDADC: ADC analog power, 3.3 V	-
VSSADC	P	69		VDDADC: ADC analog ground	-

Table 1-6 Audio CODEC Pins (13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LHPO	AO	90		LHPO: Left headphone out	VDD_{CDC}
RHPO	AO	88		RHPO: Right headphone out	VDD_{CDC}
MICIN	AI	99		MICIN: Microphone input	VDD_{CDC}
LLINEIN	AI	97		LLINEIN: Left line input	VDD_{CDC}
RLINEIN	AI	98		RLINEIN: Right line input	VDD_{CDC}
VREF	AO	94		VREF: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to VSSCDC eliminates the effects of high frequency noise	VDD_{CDC}
VDDHP	P	87		VDDHP: Headphone amplifier power, 3.3V	-
VSSHP	P	89		VSSHP: Headphone amplifier ground	-
VDDLHP	P	91		VDDLHP: Headphone amplifier power, 3.3V	-
VDDCDC	P	93		VDDCDC: CODEC analog power, 3.3V	-
VSSCDC	P	92		VSSCDC: CODEC analog ground	-
VDDCDC2	P	95		VDDCDC: CODEC analog power, 3.3V	-
VSSCDC2	P	96		VSSCDC: CODEC analog ground	-

Table 1-7 MSC (MMC/SD) Pins (3; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC_D0 PD10	IO IO	61	4mA, pullup-pe	MSC_D0: MSC data bit 0 PD10: GPIO group D bit 10	VDDIO
MSC_CMD PD08	IO IO	63	4mA, pullup-pe	MSC_CMD: MSC command PD08: GPIO group D bit 8	VDDIO
MSC_CLK PD09	O IO	62	4mA, pullup-pe	MSC_CLK: MSC clock output PD09: GPIO group D bit 9	VDDIO

Table 1-8 CPM Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	64	10~20 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	65		EXCLKO: OSC output	VDDIO
VDDPLL	P	73		VDDPLL: PLL digital power, 1.8V	-
VSSPLL	P	74		VSSPLL: PLL digital ground	-
AVDDPLL	P	71		AVDDPLL: PLL analog power, 1.8V	
AVSSPLL	P	72		AVSSPLL: PLL analog ground	

Table 1-9 RTC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	81	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	82		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	AO	86	~2mA, open-drain	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PD29	AI AI	85	Schmitt	WKUP_: Wake signal after main power down PD29: GPIO group D bit 29, input/interrupt only	VDD_{RTC}
PPRST_	AI	84	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	83		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

Table 1-10 System Pins (2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
BOOT_SEL0	I	101	Schmitt	BOOT_SEL0: Boot select bit 0	VDDIO
BOOT_SEL1	I	100	Schmitt	BOOT_SEL1: Boot select bit 1	VDDIO

Table 1-11 IO/Core power supplies (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO	P	24*2 66 104		VDDIO: 3+1 IO digital power, 3.3V	-
VSS	P	3*3 20*2 25*2 106 125		VSS: 5+4 IO/CORE digital ground	-
VDDCORE	P	4*2 21*2		VDDCORE: 2+2 CORE digital power, 1.8V	-

Connected device

- One SDRAM chip
- 1~2 NAND chips
- Use USB2.0 device connect to USB host
- Use CODEC to connect to headphone/speeker-amp/MIC/FM-radio
- SD card
- Use I2C to control FM-radio
- Power supply/charging
- SLCD
- Use PWM to support beeper
- Use PWM to support SLCD back-light
- Keypad
- RTC function enabled

GPIO needed

Device	GPIO Num	Function which needs GPIO	Comments
USB	1	Recognize connect to USB host	
CODEC	1	Speaker amplify control	
Power	1	Charging status	
	1	Charging current control	Optional
SD card	1	Card existing recognition	
	1	Write protection	Optional
	1	Power supply control	Optional
SLCD	1	Reset	
NAND	1	Write protection	Optional
Keypad	?		

GPIO available

Pin	GPIO Num	GPIO available condition
WAIT_	1	Unconditional
CS2_	1	When only one NAND chip needed
LCD_CLS, LCD_SPL, LCD_PS, LCD_REV	4	If SLCD or normal LCD panel used
LCD_DE	1	If SLCD panel used
LCD_D17~16	2	If SLCD/LCD bus width is 16- or 8-bit
LCD_D15~8	8	If SLCD/LCD bus width is 8-bit
PD26 /UART0_RxD	1	Unconditional
WKUP_ /PD29	1	Input only. Unconditional
ADIN1	N	ADC can be used to support keypad