Jz4720

Multimedia Application Processor

Data Sheet

Revision: 0.3
Date: Nov. 2007

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Ingenic Semiconductor Co. Ltd

Jz4720 32 Bits Microprocessor

Data Sheet

Release history

Date	Revision	Change
Aug. 2007	0.1	
Oct. 2007	0.2	- Add 4 LCD pins to support special LCD panel - Add ADIN1 - Add some CIM pins which can be used as GPIO
Nov. 2007	0.3	- Add bonding PAD location figures in “Jz4720 PAD Diagram” - Add note 11 for “Pin Description [1][2]”

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Content

1 Overview

Jz4720 is a low cost multimedia application processor targeting for mobie devices like MP4, electronic dictionary. Incorporate the XBurst® CPU core based on leading micro-architecture technology, this processor provides high integration, high performance and low power consumption solution for embedded device.

XBurst® is a high performance and power-efficient 32-bit RISC core with 16K instruction cache and 16K data cache, operating at speed up to 240MHz. The SIMD instruction set implemented by XBurst® core, in together with the on chip Image Processing Unit, provides MPEG-4 decoding capability up to CIF resolution at 25 frames per second. The memory interface supports a variety of memory types that allow flexible design requirements, include the glueless connection to SLC/MLC NAND Flash for cost sensitive applications. On-chip modules such as LCD controller, audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. WLAN, Bluetooth and expansion options are supported through the USB 1.1 and MMC/SD/SDIO host controllers. And the other peripherals such as USB 2.0 device, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

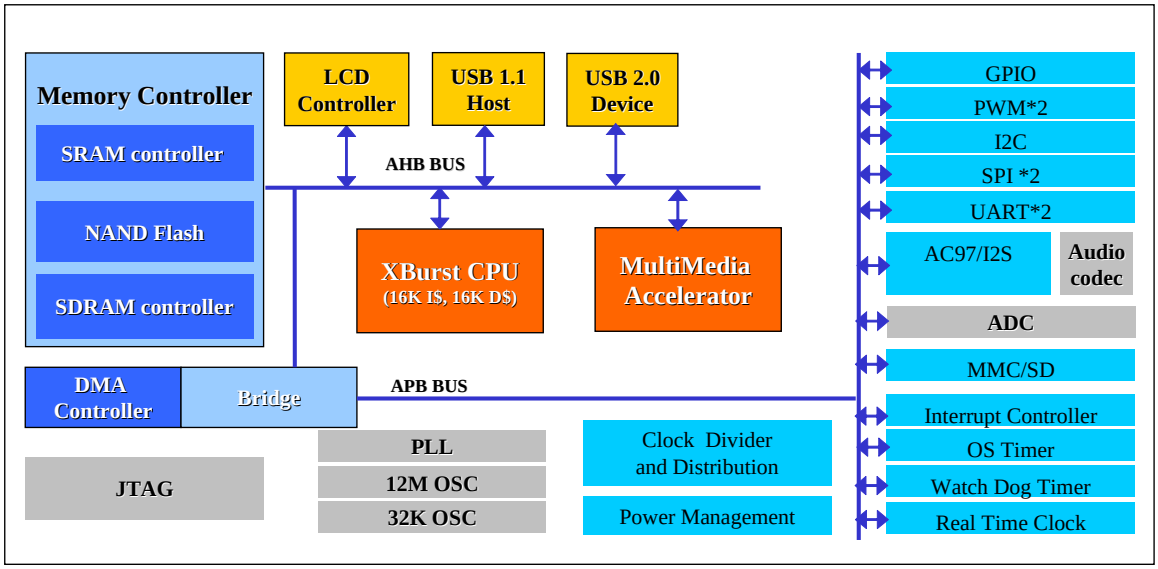

Figure 1-1 Jz4720 Diagram

1.2 Features

1.2.1 CPU core

- XBurst® RISC instruction set to support Linux and WinCE
- XBurst® SIMD instruction set to support multimedia acceleration
- XBurst® 8-stage pipeline micro-architecture up to 240MHz
- 16K I-Cache, 16K D-Cache
- 32-entry dual-pages joint-TLB, 4 entry Instruction TLB and 4 entry data TLB
- Hardware Debug support via JTAG port
- Smart prefetch to accelerate multimedia applications

1.2.2 Multimedia support

- IPU (Image Processing Unit)
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert

1.2.3 Memory sub-system

- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Six chip-select pin for static memory, each can be configured separately
  - Support 8 or 16 bits data width
  - The size and base address of static memory banks are programmable
- NAND Flash interface
  - Support MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Hamming and Reed-Solomon Hardware ECC for error detection and correction
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM Interface
  - 1 banks with programmable size and base address
  - 16-bit data bus width is supported
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
- Direct Memory Access Controller
  - Six independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
  - Interrupt on transfer completion or transfer error

  - Supports two transfer modes: single mode or block mode
- The Jz4720 processor system supports little endian only

1.2.4 Clock generation and power management

  - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
  - One On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.

1.2.5 On-chip peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is 90
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up
- Interrupt controller
  - Total 28 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output
  - Provide eight separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - PWM output supported
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power

- A 32-bits scratch register used to indicate whether power down happens for RTC power

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 18 bit data bus support 1,2,4,8 pins STN panel, 16bit and 18bit TFT and 8bit I/F TFT
  - Display size up to 800×600 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)

- AC97/I2S controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the embedded CODEC

- Embedded Audio CODEC
  - 18-bit DAC, SNR: 88dB
  - 16-bit ADC, SNR: 85dB
  - Sample rate: 8/11.025/12/16/22.05/24/32/44.1/48kHz
  - MIC input
  - L/R channels headphone output amplifier support up to 32ohm load

- SADC
  - 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage input

- MMC/SD/SDIO controller
  - Compliant with “The MultiMediaCard System Specification version 3.3”
  - Compliant with “SD Memory Card Specification version 1.01” and “SDIO Card Specification version 1.0” with 1 command channel and 4 data channels
  - 20~80 Mbps maximum data rate
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status

- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz

- Double-buffered for receiver and transmitter
- Supports general call address and START byte format after START condition

- Synchronous serial interface
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode
  - Up to 60M bps

- Two UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 921.6Kbps baudrate

- USB 1.1 host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible

- USB 2.0 device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported
  - Embedded USB 2.0 PHY

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	COB
Operating frequency	336MHz
Power consumption	150mw @ 240MHz

2 PAD/Pinout and bonding Information

2.1 Overview

Jz4720 processor is offered in good dies. The die size is 4560um x 4960um, include scribble line. COB (Chip On Board) bonding can be applied to it.

The bonding PADs are located at four sides of the die. Figure 2-1 shows the PAD placement.

The PAD width is 60um and PAD opening window is 50um x 50um for top/left/bottom sides PADs. For right side, they are 76um and 67um x 61um. Figure 2-2 shows the PAD diagram and the size.

The PAD coordinate is listed in Table 2-1. The coordinate origin is near to die left-bottom corner. There is a logo of “J4xxx” at the left-top corner. The first “4” letter can be used to calibrate the coordinate. The coordinate of the center point of the cross at this “4” is x=11.07um, y=4810.43um. Please see Figure 2-1 for the illustration.

The detailed pin descriptions are listed in Table 2-2 ~ Table 2-14.

2.2 Jz4720 PAD Diagram

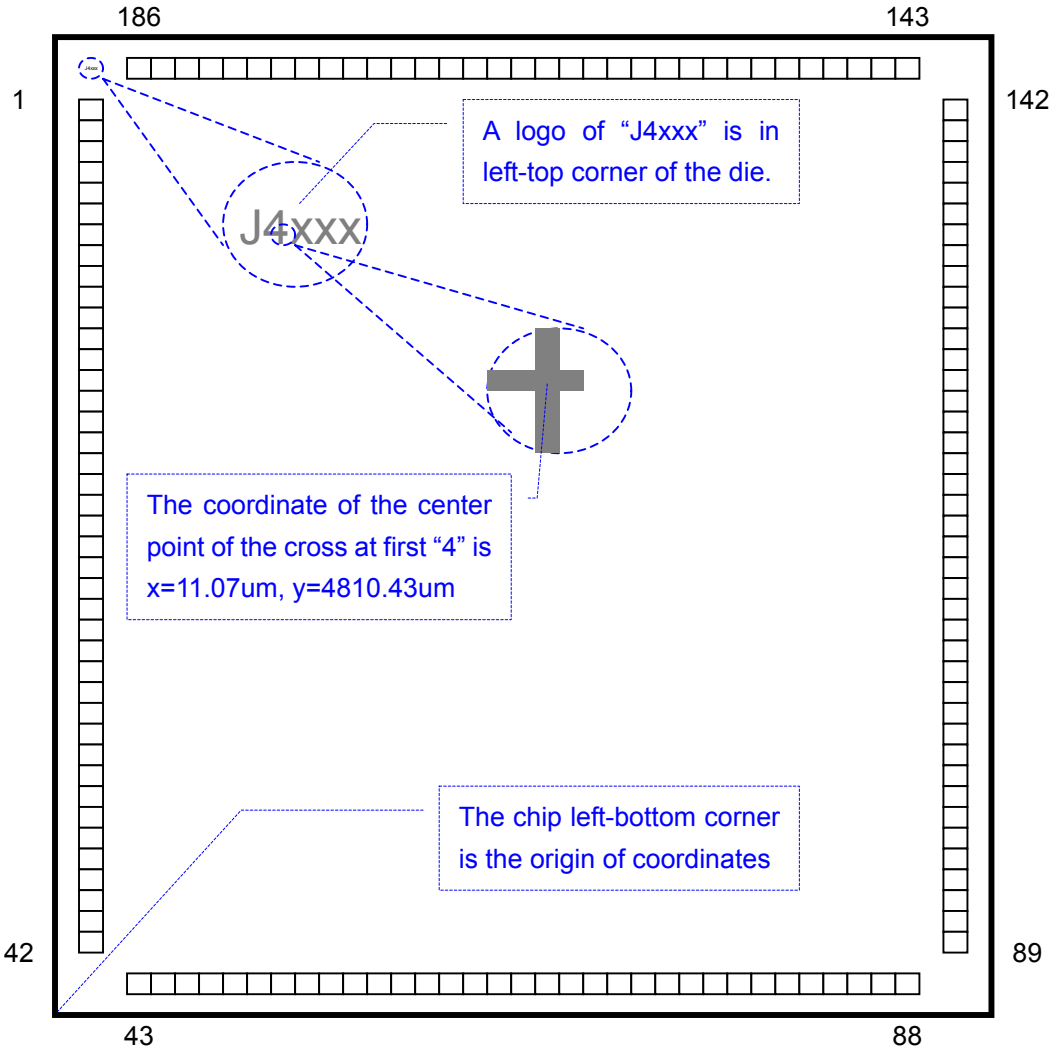

Figure 2-1 Jz4720 PAD Placement Diagram

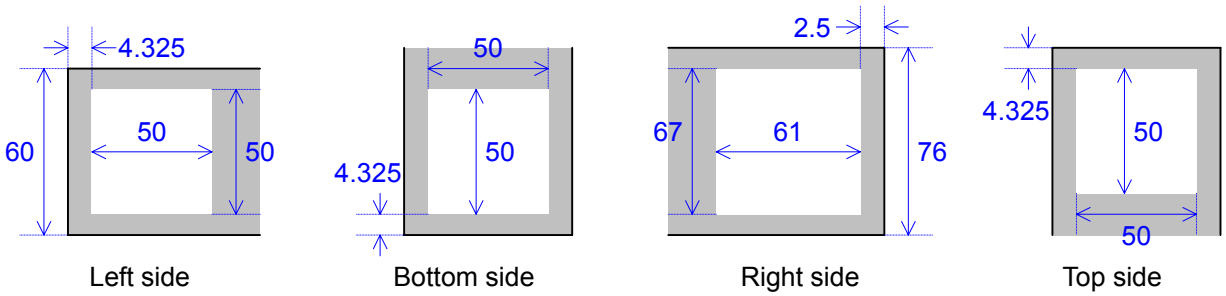

Figure 2-2 Jz4720 PAD and PAD Opening Window Size (um)

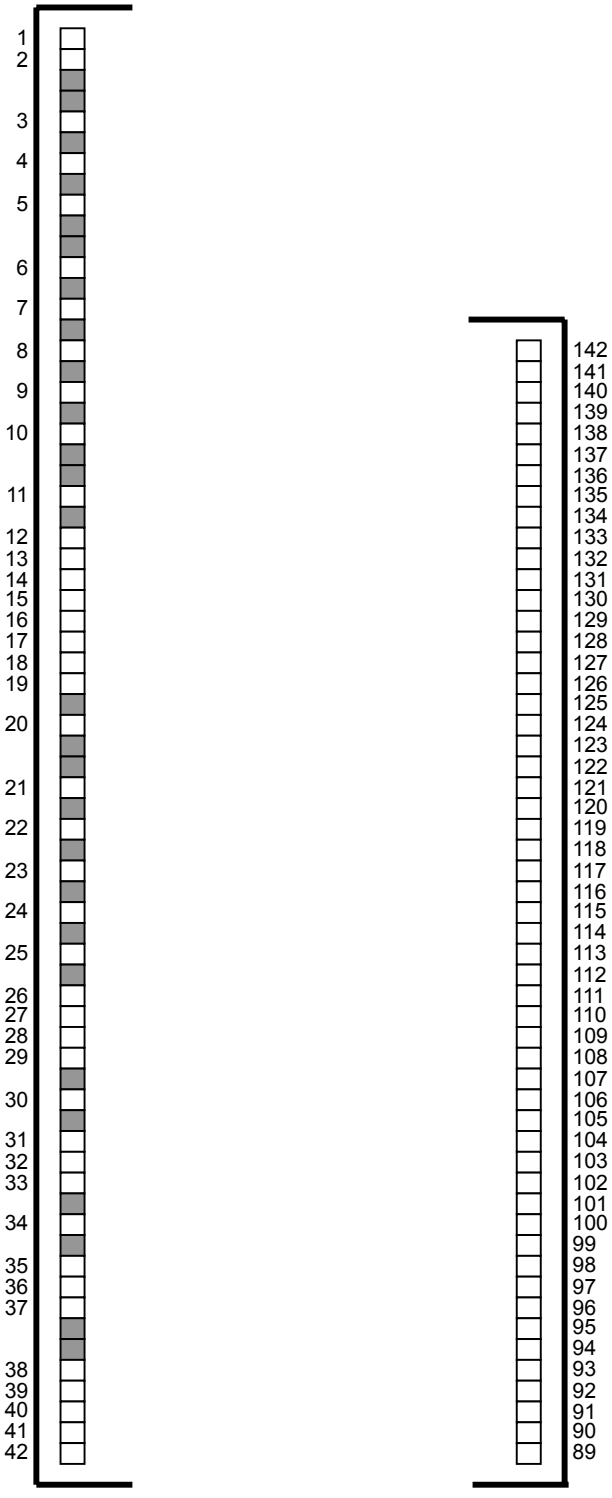

Figure 2-3 Jz4720 Left and Right sides bounding PAD location

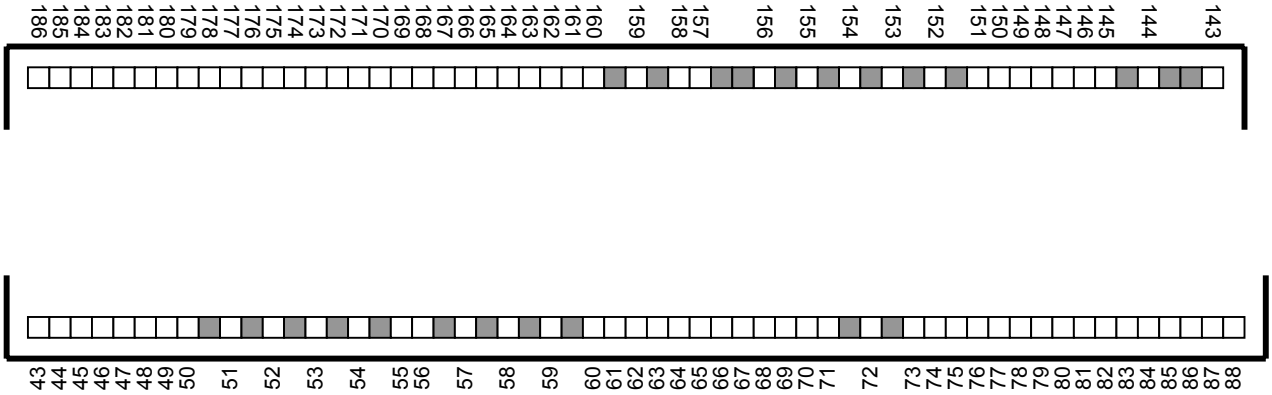

Figure 2-4 Jz4720 Top and Bottom sides bounding PAD location

2.3 PAD coordinate

For every PAD, the PAD opening window center coordinate is provided in Table 2-1. The PADs continued marked by same color (light blue or light green) can be bond together.

Table 2-1 Coordinate of PAD opening window center (um)

Pad Number	X	Y	Pad Number	X	Y	Pad Number	X	Y	Pad Number	X	Y
1	29.325	4688.13	48	559.87	29.325	95	4407	711.87	141	4407	4598.13
2	29.325	4604.13	49	637.87	29.325	96	4407	791.87	142	4407	4680.13
3	29.325	4355.87	50	715.87	29.325	97	4407	871.87	143	4200	4810.675
4	29.325	4233.87	51	868	29.325	98	4407	951.87	144	3948	4810.675
5	29.325	4111.87	52	988	29.325	99	4407	1029.87	145	3750	4810.675
6	29.325	3931.87	53	1108	29.325	100	4407	1181.87	146	3672	4810.675
7	29.325	3811.87	54	1228	29.325	101	4407	1259.87	147	3594	4810.675
8	29.325	3691.87	55	1348	29.325	102	4407	1337.87	148	3516	4810.675
9	29.325	3571.87	56	1426	29.325	103	4407	1415.87	149	3439	4810.675
10	29.325	3451.87	57	1546	29.325	104	4407	1493.87	150	3362	4810.675
11	29.325	3271.87	58	1666	29.325	105	4407	1668.87	151	3285	4810.675
12	29.325	3151.87	59	1790	29.325	106	4407	1744.87	152	3161	4810.675
13	29.325	3073.87	60	1914	29.325	107	4407	1820.87	153	3037	4810.675
14	29.325	2995.87	61	1992	29.325	108	4407	1896.87	154	2913	4810.675
15	29.325	2917.87	62	2070	29.325	109	4407	2030.7	155	2792	4810.675
16	29.325	2839.87	63	2148	29.325	110	4407	2106.7	156	2670	4810.675
17	29.325	2761.87	64	2226	29.325	111	4407	2182.7	157	2487	4810.675
18	29.325	2683.87	65	2304	29.325	112	4407	2258.7	158	2426	4810.675
19	29.325	2605.87	66	2382	29.325	113	4407	2334.7	159	2302	4810.675
20	29.325	2485.87	67	2460	29.325	114	4407	2410.7	160	2178	4810.675
21	29.325	2305.87	68	2538	29.325	115	4407	2486.7	161	2116	4810.675
22	29.325	2183.87	69	2616	29.325	116	4407	2562.7	162	2039	4810.675
23	29.325	2061.87	70	2694	29.325	117	4407	2638.7	163	1962	4810.675
24	29.325	1939.87	71	2772	29.325	118	4407	2714.7	164	1885	4810.675
25	29.325	1817.87	72	2896	29.325	119	4407	2798.13	165	1807	4810.675
26	29.325	1695.87	73	3016	29.325	120	4407	2876.13	166	1729	4810.675
27	29.325	1617.87	74	3092	29.325	121	4407	2954.13	167	1651	4810.675
28	29.325	1539.87	75	3168	29.325	122	4407	3032.13	168	1573	4810.675
29	29.325	1461.87	76	3246	29.325	123	4407	3110.13	169	1495	4810.675
30	29.325	1339.87	77	3324	29.325	124	4407	3188.13	170	1418	4810.675
31	29.325	1217.87	78	3402	29.325	125	4407	3266.13	171	1341	4810.675
32	29.325	1139.87	79	3480	29.325	126	4407	3418.13	172	1264	4810.675
33	29.325	1061.87	80	3558	29.325	127	4407	3496.13	173	1187	4810.675
34	29.325	939.87	81	3636	29.325	128	4407	3574.13	174	1109	4810.675
35	29.325	818.87	82	3714	29.325	129	4407	3652.13	175	1031	4810.675
36	29.325	740.87	83	3792	29.325	130	4407	3730.13	176	953	4810.675
37	29.325	662.87	84	3870	29.325	131	4407	3808.13	177	875	4810.675
38	29.325	479.87	85	3948	29.325	132	4407	3886.13	178	797	4810.675
39	29.325	403.87	86	4032	29.325	133	4407	3964.13	179	719	4810.675
40	29.325	319.87	87	4116	29.325	134	4407	4042.13	180	641	4810.675
41	29.325	235.87	88	4200	29.325	135	4407	4120.13	181	563	4810.675
42	29.325	151.87	89	4407	159.87	136	4407	4198.13	182	485	4810.675
43	151.87	29.325	90	4407	235.87	137	4407	4276.13	183	403.87	4810.675
44	235.87	29.325	91	4407	317.87	138	4407	4356.13	184	319.87	4810.675
45	319.87	29.325	92	4407	469.87	139	4407	4436.13	185	235.87	4810.675
46	403.87	29.325	93	4407	551.87	140	4407	4516.13	186	151.87	4810.675
47	481.87	29.325	94	4407	631.87						

2.4 Pin Description [1][2]

Table 2-2 EMC Pins (51; all GPIO shared)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
D0 PA1	IO IO	52	8mA, pullup-pe	D0: Memory data bus bit 0 PA1: GPIO group A bit 1	VDDIO
D1 PA3	IO IO	53	8mA, pullup-pe	D1: Memory data bus bit 1 PA3: GPIO group A bit 3	VDDIO
D2 PA5	IO IO	54	8mA, pullup-pe	D2: Memory data bus bit 2 PA5: GPIO group A bit 5	VDDIO
D3 PA7	IO IO	55	8mA, pullup-pe	D3: Memory data bus bit 3 PA7: GPIO group A bit 7	VDDIO
D4 PA8	IO IO	41	8mA, pullup-pe	D4: Memory data bus bit 4 PA8: GPIO group A bit 8	VDDIO
D5 PA9	IO IO	42	8mA, pullup-pe	D5: Memory data bus bit 5 PA9: GPIO group A bit 9	VDDIO
D6 PA10	IO IO	43	8mA, pullup-pe	D6: Memory data bus bit 6 PA10: GPIO group A bit 10	VDDIO
D7 PA11	IO IO	46	8mA, pullup-pe	D7: Memory data bus bit 7 PA11: GPIO group A bit 11	VDDIO
D8 PA12	IO IO	47	8mA, pullup-pe	D8: Memory data bus bit 8 PA12: GPIO group A bit 12	VDDIO
D9 PA13	IO IO	50	8mA, pullup-pe	D9: Memory data bus bit 9 PA13: GPIO group A bit 13	VDDIO
D10 PA15	IO IO	51	8mA, pullup-pe	D10: Memory data bus bit 10 PA15: GPIO group A bit 15	VDDIO
D11 PA17	IO IO	6	8mA, pullup-pe	D11: Memory data bus bit 11 PA17: GPIO group A bit 17	VDDIO
D12 PA22	IO IO	11	8mA, pullup-pe	D12: Memory data bus bit 12 PA22: GPIO group A bit 22	VDDIO
D13 PA26	IO IO	3	8mA, pullup-pe	D13: Memory data bus bit 13 PA26: GPIO group A bit 26	VDDIO
D14 PA28	IO IO	4	8mA, pullup-pe	D14: Memory data bus bit 14 PA28: GPIO group A bit 28	VDDIO
D15 PA30	IO IO	5	8mA, pullup-pe	D15: Memory data bus bit 15 PA30: GPIO group A bit 30	VDDIO
A0 PB0	O IO	15	12mA, pullup-pe	A0: Static/SDRAM memory address bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	14	12mA, pullup-pe	A1: Static/SDRAM memory address bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	13	12mA, pullup-pe	A2: Static/SDRAM memory address bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	12	12mA, pullup-pe	A3: Static/SDRAM memory address bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	38	12mA, pullup-pe	A4: Static/SDRAM memory address bit 4 PB4: GPIO group B bit 4	VDDIO
A5 PB5	O IO	37	12mA, pullup-pe	A5: Static/SDRAM memory address bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	36	12mA, pullup-pe	A6: Static/SDRAM memory address bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	35	12mA, pullup-pe	A7: Static/SDRAM memory address bit 7 PB7: GPIO group B bit 7	VDDIO
A8 PB8	O IO	32	12mA, pullup-pe	A8: Static/SDRAM memory address bit 8 PB8: GPIO group B bit 8	VDDIO

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
A9 PB9	O IO	31	12mA, pullup-pe	A9: Static/SDRAM memory address bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	16	12mA, pullup-pe	A10: Static/SDRAM memory address bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	28	12mA, pullup-pe	A11: Static/SDRAM memory address bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	27	12mA, pullup-pe	A12: Static/SDRAM memory address bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	39	12mA, pullup-pe	A13: Static/SDRAM memory address bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	40	12mA, pullup-pe	A14: Static/SDRAM memory address bit 14 PB14: GPIO group B bit 14	VDDIO
A15 CL PB15	O O IO	59	2mA, pullup-pe	A15: Static memory address bit 15 CL: NAND flash command latch PB15: GPIO group B bit 15	VDDIO
A16 AL PB16	O O IO	58	2mA, pullup-pe	A16: Static memory address bit 16 AL: NAND flash address latch PB16: GPIO group B bit 16	VDDIO
DCS_ PB19	O IO	17	8mA, pullup-pe	DCS_: SDRAM chip select PB19: GPIO group B bit 19	VDDIO
RAS_ PB20	O IO	18	8mA, pullup-pe	RAS_: SDRAM row address strobe PB20: GPIO group B bit 20	VDDIO
CAS_ PB21	O IO	19	8mA, pullup-pe	CAS_: SDRAM column address strobe PB21: GPIO group B bit 21	VDDIO
SDWE_ & BUFD_ PB22	O IO	20	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB22: GPIO group B bit 22	VDDIO
CKE PB23	O IO	26	8mA, pullup-pe	CKE: SDRAM clock enable PB23: GPIO group B bit 23	VDDIO
CKO[3] PB24	O IO	25	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CS1_ PB25	O IO	71	2mA, pullup-pe	CS1_: Static memory chip select 1 PB25: GPIO group B bit 25	VDDIO
CS2_ PB26	O IO	70	2mA, pullup-pe	CS2_: Static memory chip select 2 PB26: GPIO group B bit 26	VDDIO
CS3_ PB27	O IO	62	2mA, pullup-pe	CS3_: Static memory chip select 3 PB27: GPIO group B bit 27	VDDIO
CS4_ PB28	O IO	63	2mA, pullup-pe	CS4_: Static memory chip select 4 PB28: GPIO group B bit 28	VDDIO
RD_ PB29	O IO	61	2mA, pullup-pe	RD_: Static memory read strobe PB29: GPIO group B bit 29	VDDIO
WR_ PB30	O IO	60	2mA, pullup-pe	WR_: Static memory write strobe PB30: GPIO group B bit 30	VDDIO
WE0_ PB31	O IO	23	8mA, pullup-pe	WE0_: SDR/Static memory byte 0 write enable PB31: GPIO group B bit 31	VDDIO
WE1_ PC24	O IO	24	8mA, pullup-pe	WE1_: SDR/Static memory byte 1 write enable PC24: GPIO group C bit 24	VDDIO
WAIT_ PC27	I IO	69	2mA, Schmitt, pullup-pe	WAIT_: Slow static memory/device wait signal PC27: GPIO group C bit 27	VDDIO
FRE_ PC28	O IO	65	2mA, pullup-pe	FRE_: NAND flash read enable PC28: GPIO group C bit 28	VDDIO
FWE_ PC29	O IO	64	2mA, pullup-pe	FWE_: NAND flash write enable PC29: GPIO group C bit 29	VDDIO

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
PC30 (FRB)	IO	68	2mA, pullup-pe	PC30: GPIO group C bit 30. If NAND flash is used, it should connect to NAND FRB (NAND flash ready/busy)	VDDIO

Table 2-3 LCDC Pins (22; all GPIO shared)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
LCD_D0 PC0	O IO	1	4mA, pullup-pe	LCD_D0: LCD data bit 0 PC0: GPIO group C bit 0	VDDIO
LCD_D1 PC1	O IO	186	4mA, pullup-pe	LCD_D1: LCD data bit 1 PC1: GPIO group C bit 1	VDDIO
LCD_D2 PC2	O IO	183	4mA, pullup-pe	LCD_D2: LCD data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_D3 PC3	O IO	182	4mA, pullup-pe	LCD_D3: LCD data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_D4 PC4	O IO	179	4mA, pullup-pe	LCD_D4: LCD data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_D5 PC5	O IO	178	4mA, pullup-pe	LCD_D5: LCD data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_D6 PC6	O IO	177	4mA, pullup-pe	LCD_D6: LCD data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_D7 PC7	O IO	176	4mA, pullup-pe	LCD_D7: LCD data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_D8 PC8	O IO	175	4mA, pullup-pe	LCD_D8: LCD data bit 8 PC8: GPIO group C bit 8	VDDIO
LCD_D9 PC9	O IO	174	4mA, pullup-pe	LCD_D9: LCD data bit 9 PC9: GPIO group C bit 9	VDDIO
LCD_D10 PC10	O IO	173	4mA, pullup-pe	LCD_D10: LCD data bit 10 PC10: GPIO group C bit 10	VDDIO
LCD_D11 PC11	O IO	170	4mA, pullup-pe	LCD_D11: LCD data bit 11 PC11: GPIO group C bit 11	VDDIO
LCD_D12 PC12	O IO	169	4mA, pullup-pe	LCD_D12: LCD data bit 12 PC12: GPIO group C bit 12	VDDIO
LCD_D13 PC13	O IO	168	4mA, pullup-pe	LCD_D13: LCD data bit 13 PC13: GPIO group C bit 13	VDDIO
LCD_D14 PC14	O IO	167	4mA, pullup-pe	LCD_D14: LCD data bit 14 PC14: GPIO group C bit 14	VDDIO
LCD_D15 PC15	O IO	166	4mA, pullup-pe	LCD_D15: LCD data bit 15 PC15: GPIO group C bit 15	VDDIO
LCD_D16 PC16	O IO	165	4mA, pullup-pe	LCD_D16: LCD data bit 16 PC20: GPIO group C bit 16	VDDIO

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
LCD_D17 PC17	O IO	164	4mA, pullup-pe	LCD_D17: LCD data bit 17 PC17: GPIO group C bit 17	VDDIO
LCD_PCLK PC18	IO IO	2	4mA, pullup-pe	LCD_PCLK: LCD pixel clock PC18: GPIO group C bit 18	VDDIO
LCD_HSYNC PC19	IO IO	162	4mA, pullup-pe	LCD_HSYNC: LCD line clock/horizonal sync PC19: GPIO group C bit 19	VDDIO
LCD_VSYNC PC20	IO IO	161	4mA, pullup-pe	LCD_VSYNC: LCD frame clock/vertical sync PC20: GPIO group C bit 20	VDDIO
LCD_DE PC21	O IO	163	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC21: GPIO group C bit 21	VDDIO
LCD_CLS A21 PB17	O O IO	158	4mA, pullup-pe	LCD_CLS: LCD CLS output A21: Static memory address bit 21 PB17: GPIO group B bit 17	VDDIO
LCD_SPL A22 PB18	O O IO	157	4mA, pullup-pe	LCD_SPL: LCD SPL output A22: Static memory address bit 22 PB18: GPIO group B bit 18	VDDIO
LCD_PS A19 PC22	O O IO	160	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT A19: Static memory address bit 19 PC22: GPIO group C bit 22	VDDIO
LCD_REV A20 PC23	O O IO	159	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT A20: Static memory address bit 20 PC23: GPIO group C bit 23	VDDIO

Table 2-4 USB device 2.0 and host 1.1 Pins (14)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
DP0 [4]	AIO	115, 116		DP0: 2 USB 2.0 device data plus	VDD_{USB}
DM0 [4]	AIO	113, 114		DM0: 2 USB 2.0 device data minus	VDD_{USB}
RREF	AIO	110		RREF: External Reference for USB 2.0 device. Connect a 2.5kΩ external reference resistor, with 5% tolerance to analog ground VSSUSB	VDD_{USB}
VDDA	AIO	109		VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground VSSUSB	VDD_{USB}
VDDUSB [5]	P	105, 111, 112		VDDUSB: 3 USB analog power, 3.3V	-
VSSUSB [5]	P	108, 117, 118		VSSUSB: 3 USB analog ground	-
DP1	AIO	106		DP1: USB 1.1 host data plus	VDD_{USB}
DM1	AIO	107		DM1: USB 1.1 host data minus	VDD_{USB}

Table 2-5 SSI/AIC Pins (5; all GPIO shared)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
SSI_CLK SCLK_RSTN PD18	O O IO	84	4mA, pullup-pe	SSI_CLK: SSI clock output SCLK_RSTN: I2S system clock output or AC97 reset output PD18: GPIO group D bit 18	VDDIO
SSI_CE0_ BCLK PD19	O IO IO	85	4mA, pullup-pe	SSI_CE0_: SSI chip enable 0 BCLK: AC97/I2S bit clock PD19: GPIO group D bit 19	VDDIO
SSI_DT SDATO	O O	87	4mA, pullup-pe	SSI_DT: SSI data output SDATO: AC97/I2S serial data output	VDDIO

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
PD20	IO			PD20: GPIO group D bit 20	
SSI_DR SDATI PD21	I I IO	88	2mA, pullup-pe	SSI_DR: SSI data input SDATI: AC97/I2S serial data input PD21: GPIO group D bit 21	VDDIO
SSI_CE1__GPC SYNC PD22	O IO IO	86	2mA, pullup-pe	SSI_CE1__GPC: SSI chip enable 1 or general-purpose control signal SYNC: AC97 frame SYNC or I2S Left/Right PD22: GPIO group D bit 22	VDDIO

Table 2-6 TCU/I2C/UART Pins (6; all GPIO shared)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
PWM0 I2C_SDA PD23	O IO IO	75	4mA, pullup-pe	PWM0: PWM 0 output I2C_SDA: I2C serial data PD23: GPIO group D bit 23	VDDIO
PWM1 I2C_SCK PD24	O IO IO	74	4mA, pullup-pe	PWM1: PWM 1 output I2C_SCK: I2C serial clock PD24: GPIO group D bit 24	VDDIO
PWM2 UART0_TxD PD25	O O IO	73	2mA, pullup-pe	PWM2: PWM 2 output UART0_TxD: UART 0 transmitting data PD25: GPIO group D bit 25	VDDIO
PWM3 UART0_RxD PD26	O I IO	72	2mA, pullup-pe	PWM3: PWM 3 output UART0_RxD: UART 0 Receiving data PD26: GPIO group D bit 26	VDDIO
PWM4 A17 PD27	O O IO	57	2mA, pullup-pe	PWM4: PWM 4 output A17: Static memory address bit 17 PD27: GPIO group D bit 27	VDDIO
PWM5 A18 PD28	O O IO	56	2mA, pullup-pe	PWM5: PWM 5 output A18: Static memory address bit 18 PD28: GPIO group D bit 28	VDDIO

Table 2-7 SAR ADC Pins (7)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
XP	AI	96		XP: Touch screen X+ input	VDD_{ADC}
XN	AI	99		XN: Touch screen X- input	VDD_{ADC}
YP	AI	97		YP: Touch screen Y+ input	VDD_{ADC}
YN	AI	98		YN: Touch screen Y- input	VDD_{ADC}
PBAT/ADIN0	AI	92		ADIN0: Battery voltage input or ADC general purpose input 0	VDD_{ADC}
ADIN1	AI	93		ADIN1: ADC general purpose input 1	VDD_{ADC}
VDDADC	P	95		VDDADC: ADC analog power, 3.3 V	-
VSSADC	P	94		VDDADC: ADC analog ground	-

Table 2-8 Audio CODEC Pins (19)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
LHPO [6]	AO	134, 135		LHPO: 2 Left headphone out	VDD_{LHP}
RHPO [6]	AO	128, 129		RHPO: 2 Right headphone out	VDD_{LHP}
MICIN	AI	144		MICIN: Microphone input	VDD_{LHP}
MICBIAS	AO	143		MICBIAS: Microphone bias	VDD_{LHP}
VREF [7]	AO	140		VREF: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to VSSDAC eliminates the effects of high frequency noise	VDD_{LHP}
VDDRHP [8]	P	126, 127		VDDRHP: 2 Right headphone amplifier power, 3.3V	-
VSSRHP [8]	P	130, 131		VSSRHP: 2 Right headphone amplifier ground	-
VDDLHP [8]	P	136, 137		VDDLHP: 2 Left headphone amplifier power, 3.3V	-
VSSLHP [8]	P	132, 133		VSSLHP: 2 Left headphone amplifier ground	-
VDDCDAC [9]	P	139		VDDCDAC: CODEC DAC analog power, 3.3V	-
VSSCDAC [9]	P	138		VSSCDAC: CODEC DAC analog ground	-
VDDCADC	P	141		VDDCADC: CODEC ADC analog power, 3.3V	-
VSSCADC	P	142		VSSCADC: CODEC ADC analog ground	-

Table 2-9 MSC (MMC/SD) Pins (6; all GPIO shared)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
MSC_D0 PD10	IO IO	81	4mA, pullup-pe	MSC_D0: MSC data bit 0 PD10: GPIO group D bit 10	VDDIO
MSC_D1 PD11	IO IO	80	4mA, pullup-pe	MSC_D0: MSC data bit 1 PD11: GPIO group D bit 11	VDDIO
MSC_D2 PD12	IO IO	79	4mA, pullup-pe	MSC_D0: MSC data bit 2 PD12: GPIO group D bit 12	VDDIO
MSC_D3 PD13	IO IO	78	4mA, pullup-pe	MSC_D0: MSC data bit 3 PD13: GPIO group D bit 13	VDDIO
MSC_CMD PD08	IO IO	83	4mA, pullup-pe	MSC_CMD: MSC command PD08: GPIO group D bit 8	VDDIO
MSC_CLK PD09	O IO	82	4mA, pullup-pe	MSC_CLK: MSC clock output PD09: GPIO group D bit 9	VDDIO

Table 2-10 CPM Pins (7)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
EXCLK	AI	89	10~20 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	90		EXCLKO: OSC output	VDDIO
AVDDPLL [10]	P	100		AVDDPLL: PLL analog power, 1.8V	-
AVSSPLL [10]	P	101, 102		AVSSPLL: 2 PLL analog grounds	-
DVDDPLL [10]	P	103		DVDDPLL: PLL digital power, 1.8V	-
DVSSPLL [10]	P	104		DVSSPLL: PLL digital ground	-

Table 2-11 RTC Pins (7)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
RTCLK	AI	120	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AIO	121		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	AO	125	~2mA, open-drain	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PD29	AI AI	124	Schmitt	WKUP_: Wake signal after main power down PD29: GPIO group D bit 29, input/interrupt only	VDD_{RTC}
PPRST_	AI	123	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	122		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-
VSSRTC	P	119		VSSRTC: RTC ground	-

Table 2-12 JTAG/UART Pins (5)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
TRST_	I	151	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK	I	149	Schmitt, pull-down	TCK: JTAG clock	VDDIO
TMS	I	150	Schmitt, pull-up	TMS: JTAG mode select	VDDIO
TDI UART0_RxD	I I	148	Schmitt, pull-up	TDI: JTAG serial data input UART0_RxD: UART 0 Receiving data, PC31 is used to select between JTAG and UART	VDDIO
TDO UART0_TxD	O O	147	4mA	TDO: JTAG serial data output UART0_TxD: UART 0 transmitting data, PC31 is used to select between JTAG and UART	VDDIO

Table 2-13 System Pins (3)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
BOOT_SEL0	I	146	Schmitt	BOOT_SEL0: Boot select bit 0	VDDIO
BOOT_SEL1	I	145	Schmitt	BOOT_SEL1: Boot select bit 1	VDDIO
CHIP_MD	I	180	Schmitt	CHIP_MD: This pin should be bonding to 3.3V	VDDIO
PD00	IO	155	4mA, pullup-pe	PD00: GPIO group D bit 0	VDDIO
PD02	IO	154	4mA, pullup-pe	PD02: GPIO group D bit 2	VDDIO
PD04	IO	153	4mA, pullup-pe	PD04: GPIO group D bit 4	VDDIO
PD06	IO	152	4mA, pullup-pe	PD06: GPIO group D bit 6	VDDIO
PD15	IO	156	4mA, pullup-pe	PD15: GPIO group D bit 15	VDDIO

Table 2-14 IO/Core power supplies (26)

Pin Names	IO	PAD Number	IO Cell Char.	Pin Description	Power
VDDIO	P	7, 33, 49, 66, 91, 185		VDDIO: 6 IO digital power, 3.3V	-
VSSIO	P	8, 34, 48, 67, 184		VSSIO: 5 IO digital ground	-
VDDCORE	P	10, 21, 30, 44, 76, 172		VDDCORE: 6 CORE digital power, 1.8V	-
VSSCORE	P	9, 22, 29, 45, 77, 171, 181		VSSCORE: 7 CORE digital ground	-

Notes:

[1]. The meaning of phases in IO cell characteristics are

a) 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12mA
b) Pull-up: The IO cell contains a pull-up resistor
c) Pull-down: The IO cell contains a pull-down resistor
d) Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
e) Schmitt: The IO cell is Schmitt trig input

[2]. For any GPIO shared pin except WAIT_/PC27 and CKO/PB24, the reset state is GPIO input with internal pull-up. The WAIT_/PC27 and CKO/PB24 are initialed to WAIT_ and CKO functions with internal pull-up.

[3]. CKO can be up to 100 MHz. Please make space for other signals from it.

[4]. DM0/DP0 are 480M USB differential signals, please make them parallel. They are noise sensitive. Please make space between it and other signals, especially strong signals.

[5]. VDDUSB/VSSUSB is power supply, typical 10mA, for the embedded high speed (480Mbps) USB PHY, which is sensitive to noise. Please make it as short as possible to attached capacitance, and make space between it and other signals, especially strong signals.

[6]. RHPO and LHPO are CODEC left/right channel headphone output. They are noise sensitive. Please make space between it and other signals, especially strong signals. Please make the trace < 0.02Ω.

[7]. VREF is very sensitive to noise. Please make it as short as possible to the attached capacitance and make space between it and other signals, especially strong signals.

[8]. VDDRHP/VSSRHP and VDDLHP/VSSLHP are power supplies (typical 10mA each) for CODEC left/right channel headphone amplifiers respectively. They are noise sensitive. Please make them as short as possible to the attached capacitance and make space between it and other signals, especially strong signals. Please make the trace < 0.02Ω.

[9]. VDDCDAC/VSSCDAC is the power supply for embedded audio CODEC DAC, which is noise sensitive. Please make it as short as possible to the attached capacitance and make space between it and other signals, especially strong signals. VDDRHP, VDDLHP, VDDCDAC and VDDCADC can be directly connected. VSSRHP, VSSLHP, VSSCDAC and VSSCADC can be

directly connected.

[10]. AVDDPLL and DVDDPLL can be directly connected. AVSSPLL and DVSSPLL can be directly connected. Please make the bonding wire length of these PAD as short as possible to reduce inductance. PLL is noise sensitive. Please make it as short as possible to the attached capacitance and make space between it and other signals, especially strong signals.

[*]. When the above requirements conflict with each other, please take following priority order:

Priority	Signals or Power Supplies
Highest priority	VREF
2nd priority	VDDCDAC/VSSCDAC
3rd priority	VDDHPR/VSSHPR, VDDHPL/VSSHPL, RHPO, LHPO
4th priority	VDDUSB/VSSUSB, DP0, DM0
5th priority	AVDDPLL/AVSSPLL/DVDDPLL/DVSSPLL

[11]. Most of the PAD can be left not bond if it is not needed. But the following conditions must be fulfilled.

a) If USB1.1 host is used, the PHY power supply PAD 105 and 108 must be bonded, else, they can be left not bound.
b) USB2.0 PHY power supply PAD 111, 112, 117 and 118 must be bonded regardless of USB2.0 device is used or not.
c) SADC power supply PAD 94 and 95 must be bonded
d) CODEC power supply PAD 138, 139, 141, 142, and either of 126/127, either of 130/131, either of 136/137 and either of 132/133 must be bonded. It is recommended to bond both 126 and 127, 130 and 131, 136 and 137, 132 and 133, if CODEC is used.
e) PLL power supply PAD 100, 103, 104 and either of 101/102 must be bonded. It is recommended to bond both 101 and 102
f) RTC power supply PAD 119 and 122 must be bonded
g) VDDIO PAD 91 must be bonded. It is not recommended to bond to few VDDIO PADs.
h) Either of VSSIO PAD 8, 34, 48, 67 and 184 must be bonded. It is not recommended to bond to few VSSIO PADs.
i) Either of VDDCORE PAD 10, 21, 30, 44, 76 and 172 must be bonded. It is not recommended to bond to few VDDCORE PADs.
j) Either of VSSCORE PAD 9, 22, 29, 45, 77, 171 and 181 must be bonded. It is not recommended to bond to few VSSCORE PADs.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
VDDUSB power supplies voltage	-0.3	3.9	V
VDDCDAC power supplies voltage	-0.3	4.0	V
VDDCADC power supplies voltage	-0.3	4.0	V
VDDLHP/VDDRHP power supplies voltage	-0.3	4.0	V
VDDADC power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
AVDDPLL/DVDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to VDDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to VDDADC supplied non-supply pins except PBAT	-0.5	4.0	V
Input voltage of PBAT	-0.5	6.0	V
Input voltage to VDDCDAC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from VDDADC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDCDAC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{USB}	VDDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	VDDCDAC/VDDCADC voltage	3.0	3.3	3.6	V
V_{HP}	VDDLHP/VDDRHP voltage	3.0	3.3	3.6	V
V_{ADC}	VDDADC voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{ILH}	Input voltage range for full speed applications	0		V_{USB}	V
V_{ILH}	Input voltage range for high speed applications	120		400	mV

Table 3-5 Recommended operating conditions for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{ILH}	Input voltage range	0		V_{USB}	V

Table 3-6 Recommended operating conditions for VDDCDC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{ILH}	Input voltage range	0		V_{CDC}	V

Table 3-7 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{ILH-PBAT1}$	PBAT input voltage range when measuring low voltage battery	0		2.5	V
$V_{ILH-PBAT2}$	PBAT input voltage range when measuring high voltage battery	0		5	V

$V_{ILH-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V
$V_{ILH-TSC}$	XN/XP/YN/YP input voltage range	0		V_{ADC}	

Table 3-8 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V

Table 3-9 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-10 DC characteristics for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point	1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.88	0.94	0.99	V
I_L	Input Leakage Current			±10	μA
I_{OZ}	Tri-State output leakage current			±10	μA
R_{PU}	Pull-up Resistor	50	65	100	kΩ
R_{PD}	Pull-down Resistor	40	56	107	kΩ
C	Capacitance of the pins	4	5	10	pF
V_{OL}	Output low voltage @I_{OL}=2, 4, 8, 12mA			0.4	V
V_{OH}	Output high voltage @I_{OH}=2, 4, 8, 12mA	2.4			V
I_{OL}	Low level output current @V_{OL}=0.4V for cells of				mA
	2mA	2.2	3.7	4.6	
	4mA	4.4	7.4	9.2	
	8mA	8.9	14.7	18.4	
	12mA	13.3	22.1	27.5	
I_{OH}	High level output current @V_{OH}=2.4V for cells of				mA
	2mA	2.5	5.1	7.9	
	4mA	5.0	10.2	15.9	
	8mA	10.0	20.4	31.7	
	12mA	15.0	30.6	47.6	

Table 3-11 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OL}	Output low voltage	0		V_{USB}	V
V_{OH}	Output high voltage	0		400	mV

Table 3-12 DC characteristics for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{OLH}	Output voltage range	0		V_{USB}	V
V_{DI}	Differential input sensitivity	0.2			V

V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V
I_{OZ}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL}	Static output low voltage			0.3	V
V_{OH}	Static output high voltage	2.8			V

Table 3-13 DC characteristics for VDDCDC supplied pins

Symbol	Description	Min	Typical	Max	Unit
V_{OLH}	Output voltage range	0		V_{CDC}	V

Table 3-14 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH}	XN/XP/YN/YP output high voltage	0.9 * V_{ADC}		V_{ADC}	V
V_{OL}	XN/XP/YN/YP output low voltage	0		0.1 * V_{ADC}	V

Table 3-15 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH}	Output high voltage	2.0		3.6	V
V_{OL}	Output low voltage	-0.3		0.8	V

3.4 Characteristics of CODEC

Table 3-16 CODEC characteristics

Parameter	Conditions	Min	Typical	Max	Unit
S/N (A-weighted)-DAC	Note 1		90		dB
S/N (A-weighted)-ADC	Note 1		85		dB
Dynamic range (A-weighted) @-60dB	Fin@1kHz		90		dB
THD+N (A-weighted) @-6dB-DAC	Note 2				dB
THD+N (A-weighted) @-6dB-ADC	Note 3	70			dB
Inter-channel isolation	Fin@1kHz		60		dB
Inter-channel gain mismatch			0.1	0.2	dB
Closed loop gain			0		dB
Load resistance for HPOUTL & HPOUTR		32			Ω
Power supply rejection @ 200Hz			60		dB
Passband		0		0.42	fs
Passband ripple				±0.1	dB
Stopband		0.58			fs
Stopband attenuation		76			dB
LLINEIN/MIC resistance			40		KΩ
LLINEIN/MIC input range			1.6		Vp-p
MICBIAS voltage			2/3Avd		V
MICBIAS drive current			2		mA
HPOUT output peak value			1.8		Vp-p
Analog supply voltage		3.0	3.3	3.6	V
Digital supply voltage		1.62	1.8	1.98	V
Standby current			3		uA
Power Consumption (no tone)	DAC enable		28		mW
	ADC enable		34		mW
	ADC/DAC enable		62		mW

Note:

1. The ratio of the rms output level with 1KHz full-scale input to the rms output noise level. Measured “A-weighted” over a 20Hz to 0.44Fs bandwidth.
2. The ratio of the rms value of the signal to the rms sum of all the spectral components less than 0.44Fs bandwidth, including distortion components, tested at -6dB input. The headphone output THD+N>= 70dB under 32Ohm/16Ohm loading.

3.5 Power Consumption Specifications

Power consumption depends on the operating frequency, operating voltage, program used which determines internal and external switching activities, external loading and even environment ambient. The typical power consumption of both dynamic and static for the Jz4720 processor are provided here.

Table 3-17 Digital Dynamic Power Consumption Specifications

Symbol	Description	Conditions	Typical	Unit
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1 = VDDUSB = 3.3V, CPU clock = 360MHz, AHB/APB/SDRAM clock = 120MHz, Program = run GCC to compile a C file in Linux, Temp = room, 12MHz crystal used for EXCLK, CIM is not in use, LCD is in use		mA
I_{PLL}	VDDPLL current			mA
I_{IO}	VDDIO current			mA
I_{RTC}	VDDRTC current			uA
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1 = VDDUSB = 3.3V, CPU clock = 180MHz, AHB/APB/SDRAM clock = 60MHz, Program = run GCC to compile a C file in Linux, Temp = room, 12MHz crystal used for EXCLK, CIM is not in use, LCD is in use		mA
I_{PLL}	VDDPLL current			mA
I_{IO}	VDDIO current			mA
I_{RTC}	VDDRTC current			uA
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1 = VDDUSB = 3.3V, CPU clock = 240MHz, AHB/APB/SDRAM clock = 120MHz, Program = run GCC to compile a C file in Linux, Temp = room, 12MHz crystal used for EXCLK, CIM is not in use, LCD is in use		mA
I_{PLL}	VDDPLL current			mA
I_{IO}	VDDIO current			mA
I_{RTC}	VDDRTC current			uA

Table 3-18 Digital Static Power Consumption Specifications

Symbol	Description	Conditions	Typical	Unit
I_{CORE}	VDDcore current	VDDcore = VDDPLL = 1.8V, VDDIO1 = VDDUSB = 3.3V, Temp = room, Chip enters sleep mode with 12MHz oscillator disabled		mA
I_{PLL}	VDDPLL current			mA
I_{IO}	VDDIO current			mA
I_{RTC}	VDDRTC current			uA
I_{RTC}	VDDRTC current	Chip enters hibernating mode with all powers except VDDRTC off, Temp = room		uA

Table 3-19 CODEC Power Consumption Specifications

Table 3-20 USB Power Consumption Specifications

Table 3-21 ADC Power Consumption Specifications

3.6 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768KHz oscillator and a EXCLK oscillator. When choosing a crystal, match the crystal parameters as closely as possible.

3.6.1 32.768KHz Oscillator Specifications

3.6.2 EXCLK Oscillator Specifications

3.7 Power On, Reset and BOOT

3.7.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the Jz4720 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-22.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1. VDDRTC
2. VDDA: VDDCDAC, VDDCADC, VDDLHP, VDDRHP
3. All other 3.3V VDDs (VDD33): VDDIO, VDDADC, VDDUSB
4. All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

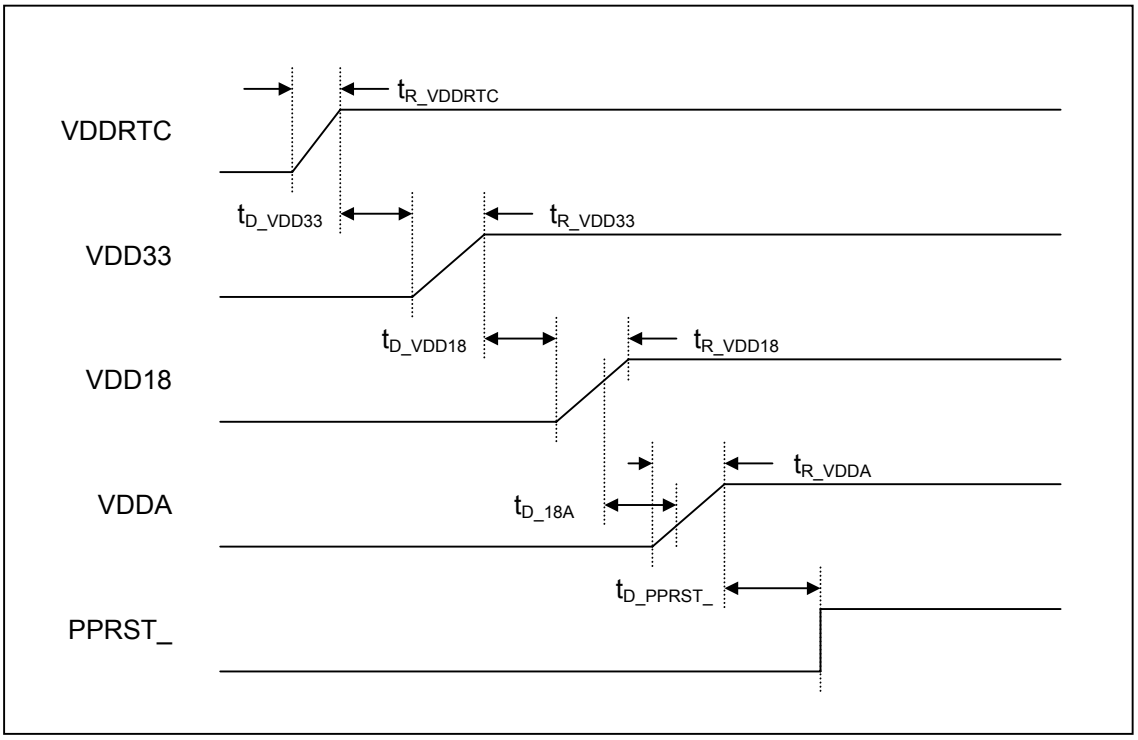

Figure 3-1 Power-On Timing Diagram

Table 3-22 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33 applies	$-t_{R\_VDDRTC}$	–	10	ms[1]
t_{R_VDD33}	VDD33 rise/stabilization time	0	–	100	ms

t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	$-t_{R\_VDD33}/2$	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0	–	100	ms
t_{D_18A}	Delay between VDD18 (actually VDDcore) arriving 1.5V and VDDA arriving 1V	0.01	–	10	ms
t_{R_VDDA}	VDDA rise/stabilization time	0	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDDA stable and PPRST_ deasserted	20	–	–	ms

Note:

1. VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.
2. VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.7.2 Reset procedure

There 3 reset sources: (1) PPRST_ pin reset; (2) WDT timeout reset; and (3) hibernating reset when exiting hibernating mode. After reset, program start from boot.

(1) PPRST_ pin reset

This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is a few RTCLK cycles after rising edge of PPRST_.

(2) WDT reset

This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

(3) Hibernating reset

This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except WAIT_ pin, are put to GPIO input function with the internal pull-up set to on. The WAIT_ pin is set to wait function with the internal pull-up set to on. The PWRON_ is output 0. The 32768Hz/12MHz oscillators are on. The JATG/UART is put to JTAG function and the TDO is output high-Z (suppose TRST_ is 0). The analog devices, the USB 2.0 PHY, USB 1.1 PHY, the CODEC DAC/ADC and the SAR-ADCs, are put in suspend mode.

3.7.3 BOOT

Jz4720 support 3 different boot sources depending on BOOT_SEL0 and BOOT_SEL1 pin values. Table 3-23 lists them.

Table 3-23 Boot from 3 boot sources

BOOT_SEL1	BOOT_SEL0	Boot Source
0	0	Boot from NOR flash at CS4
0	1	Boot from USB device
1	0	Boot from 512 page NAND flash at CS1
1	1	Boot from 2k page NAND flash at CS1

When Jz4720 BOOT from NOR at CS4_ or from NAND at CS1_, some of the memory interface pins are set to function pin from the default GPIO pin and are used in executing BOOT ROM instructions. When BOOT from USB, none of any pins are used. Table 3-24 lists the cases.

Table 3-24 Pins are used and are set to function pins during BOOT

Boot Source Condition	GPIO pin state changed from RESET
USB	None
8-bits NOR flash at CS4_	A0~A22 (PB0~PB16, PC22, PD27, PD28, PC23, PB17, PB18); CS4_ (PB28); RD_ (PB29); WR_ (PB30); SDWE_/BUFD_ (PB22); D0~D7(PA1, PA3, PA5, PA7, PA8~PA11)
16-bits NOR flash at CS4_	A0~A22 (PB0~PB16, PC22, PD27, PD28, PC23, PB17, PB18); CS4_ (PB28); RD_ (PB29); WR_ (PB30); SDWE_/BUFD_ (PB22); D0~D16(PA1, PA3, PA5, PA7, PA8~PA13, PA15, PA17, PA22, PA26, PA28, PA30)
8-bits NAND flash at CS1_	CLE(PB15); ALE(PB16); CS1_(PB25); FRE(PC28); FEW(PC29); FRB(PC30); SDWE_/BUFD_ (PB22); D0~D7(PA1, PA3, PA5, PA7, PA8~PA11)
16-bits NAND flash at CS1_	CLE(PB15); ALE(PB16); CS1_(PB25); FRE(PC28); FEW(PC29); FRB(PC30); SDWE_/BUFD_ (PB22); D0~D15(PA1, PA3, PA5, PA7, PA8~PA13, PA15, PA17, PA22, PA26, PA28, PA30)

3.8 Memory Bus AC Specifications

This section provides the timing information for these types of memory:

- SRAM / ROM / Flash
- SDRAM

3.9 Peripheral Module AC Specifications

3.9.1 LCD Module Timing

3.9.2 SPI Module Timing

3.9.3 External DMA Request and Grant