

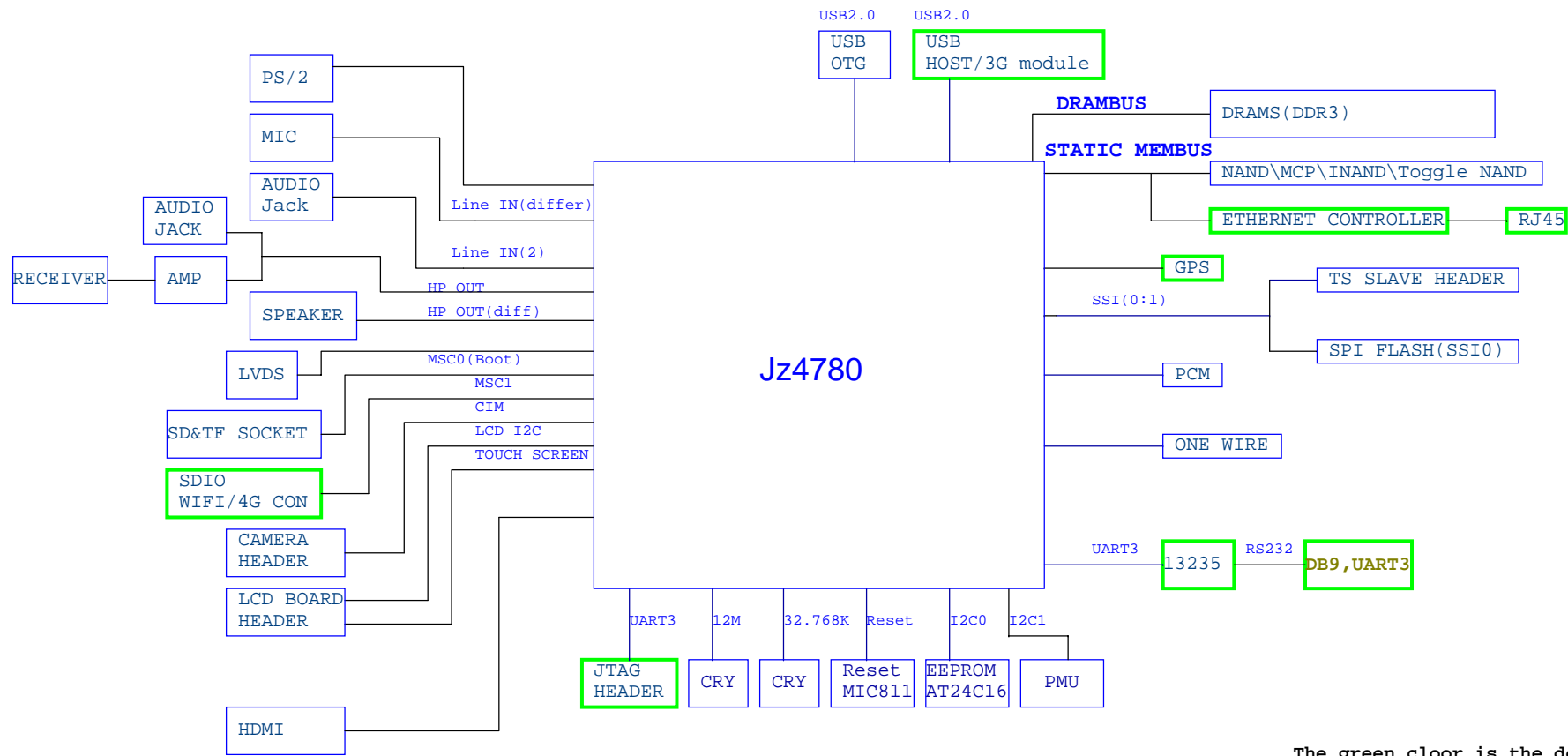


RD4780_GRUS_BOARD

Schematic Revision 1.0.2

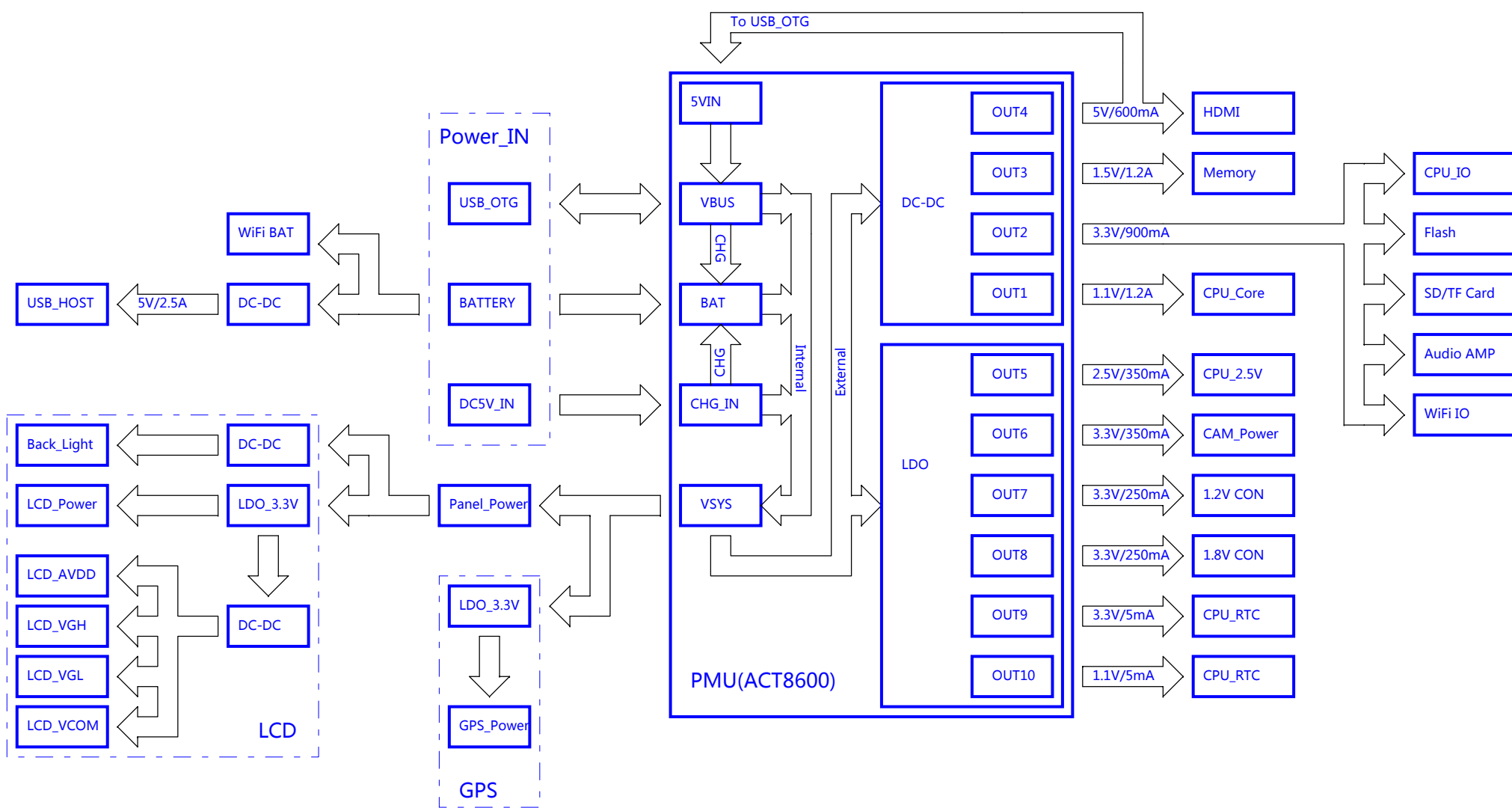
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SYSTEM ARCHITECTURE	2
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TS/ETH/UART/GPS/JTAG/USB_CON	10
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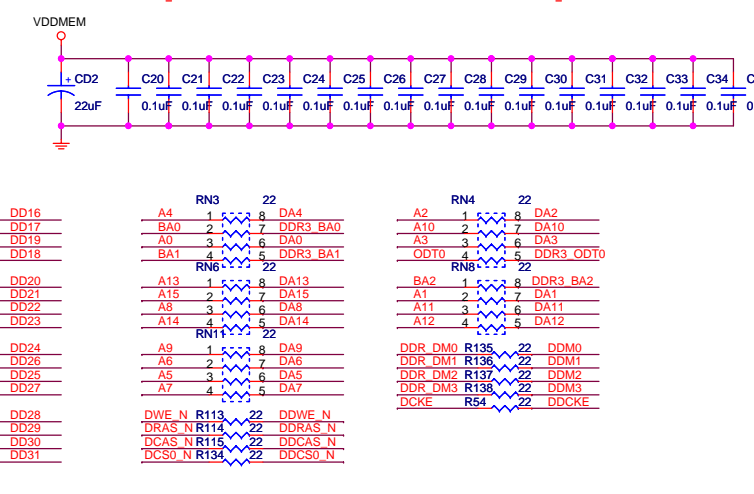
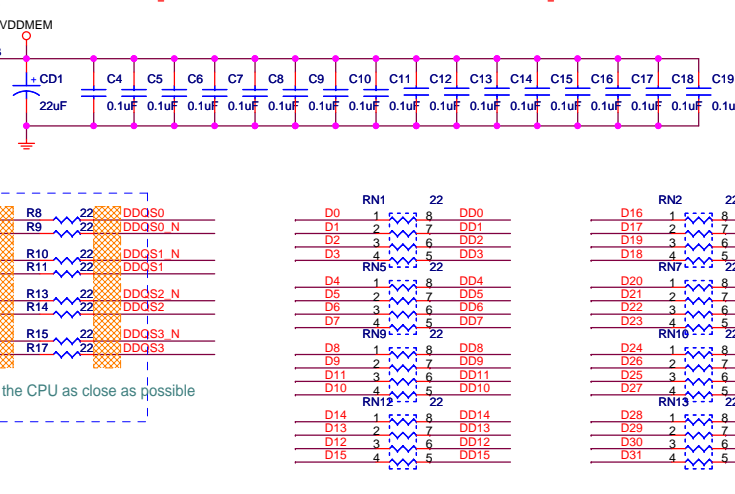
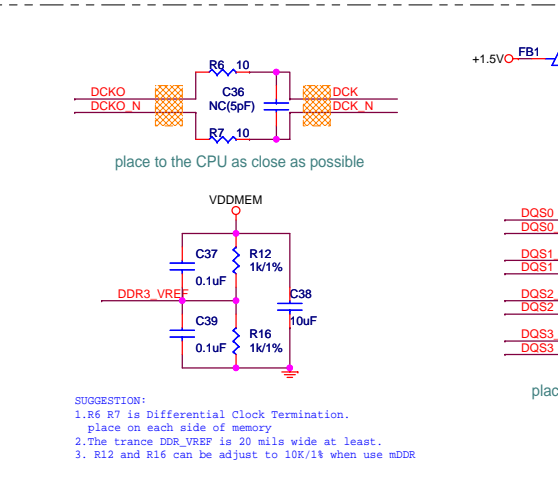
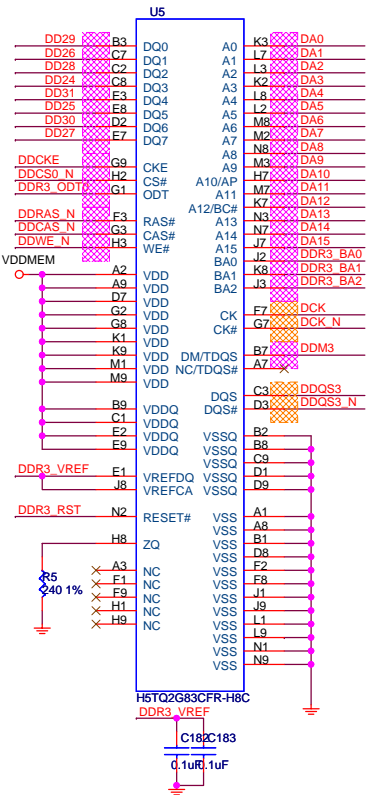
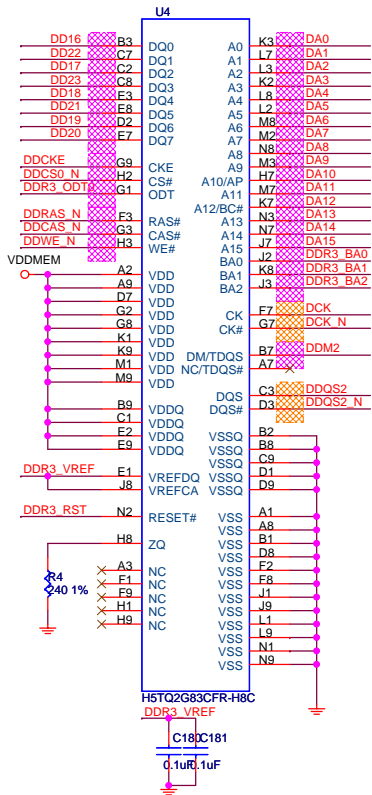
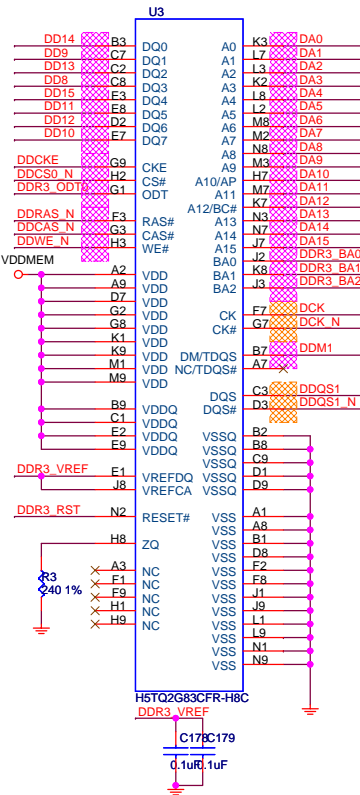
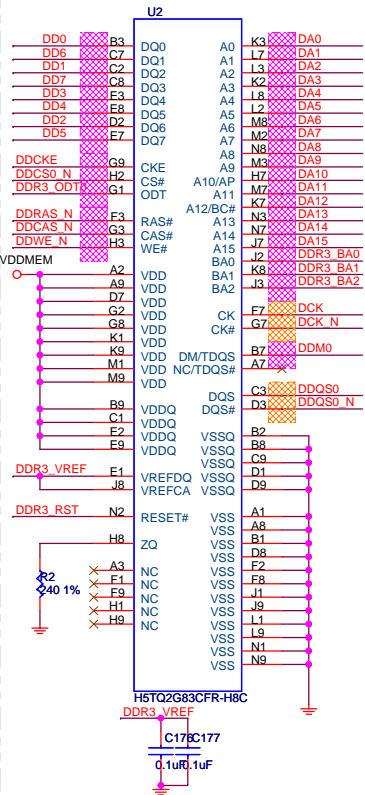
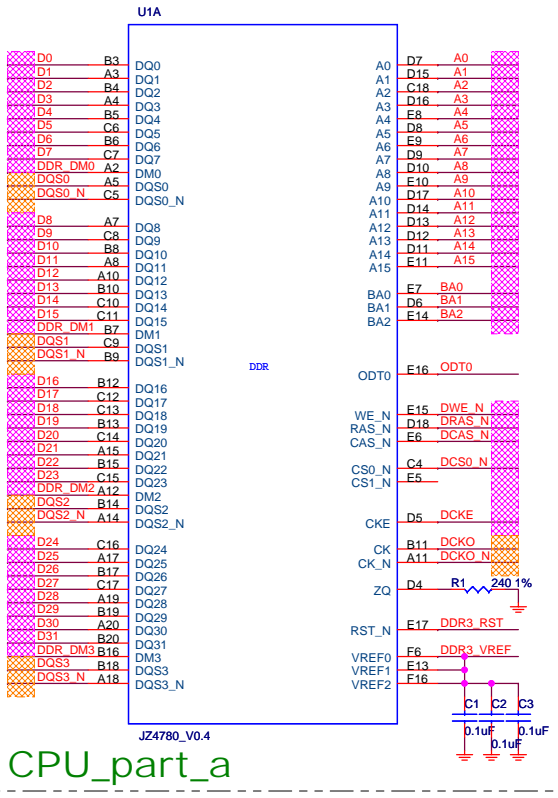
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The green color is the debug board

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A3	SYSTEM ARCHITECTURE	1.0.2	
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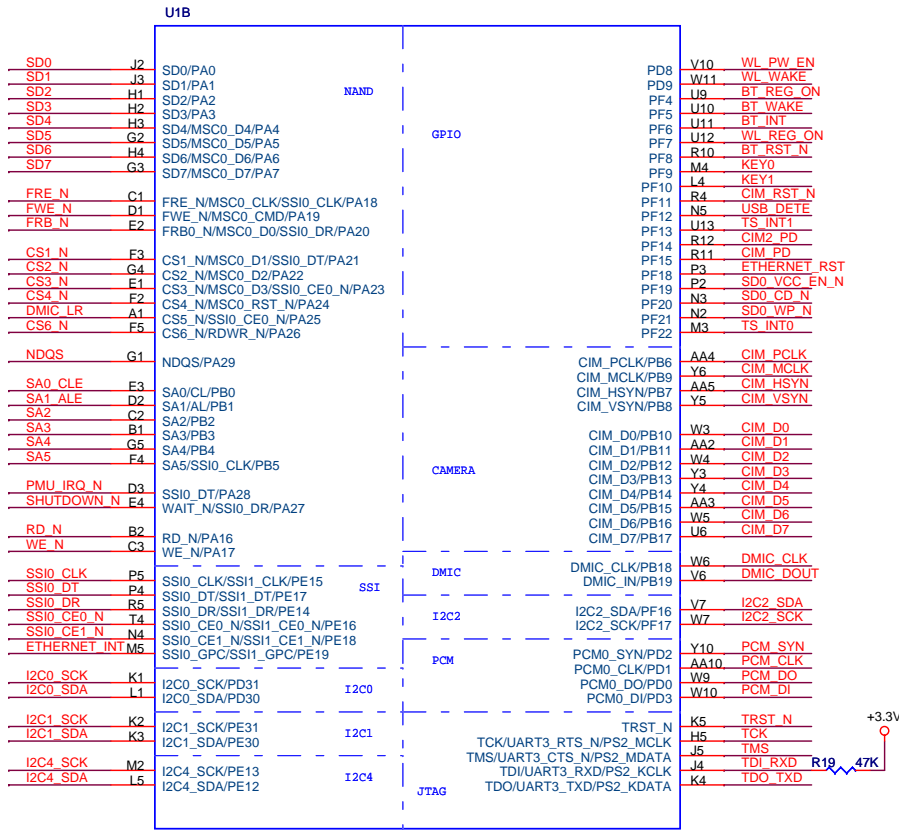




Differential pairs ZO= 100 ohm Equilong BUS ZO= 50 ohm

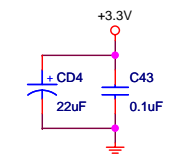
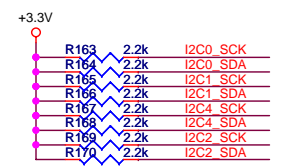
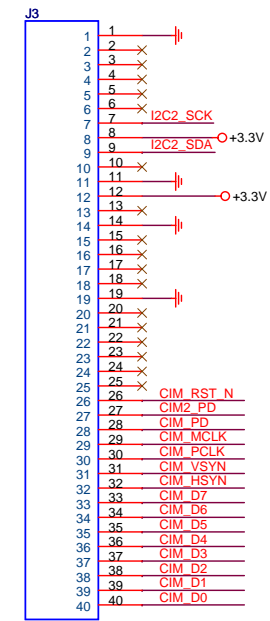
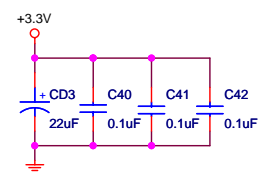
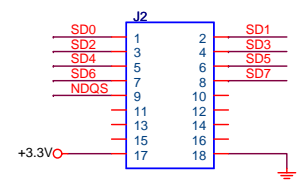
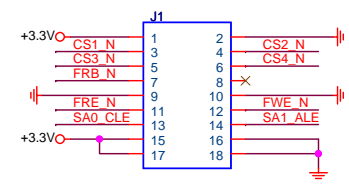
DDR3

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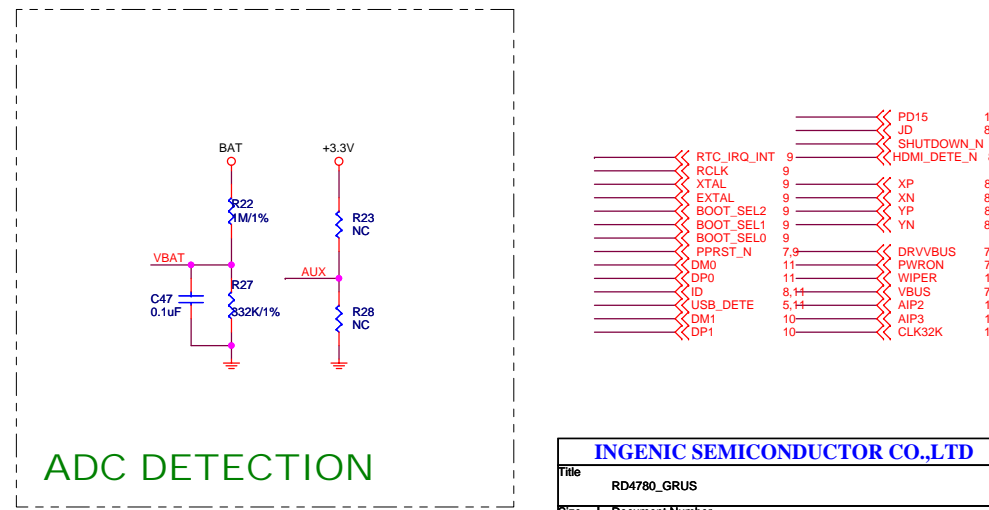
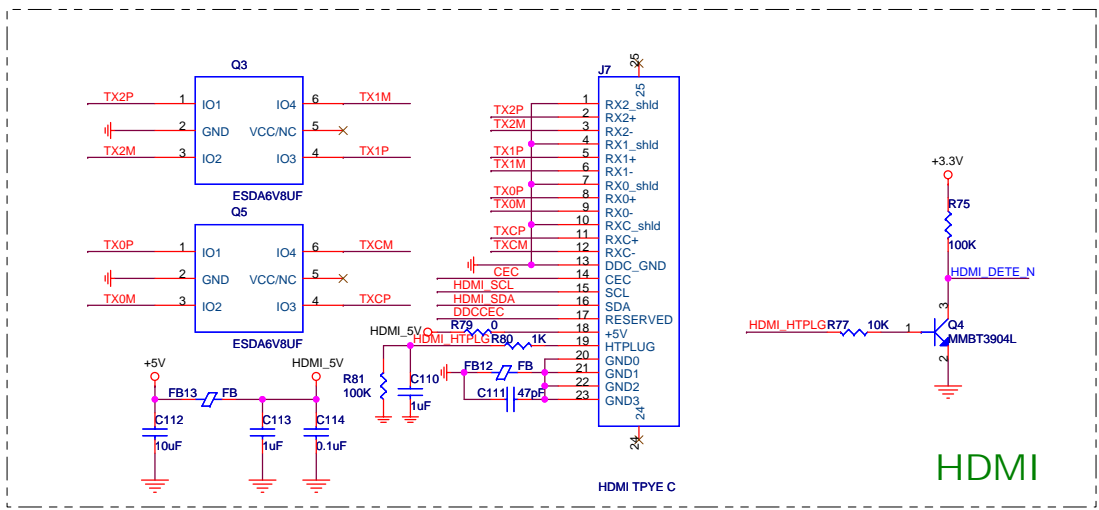
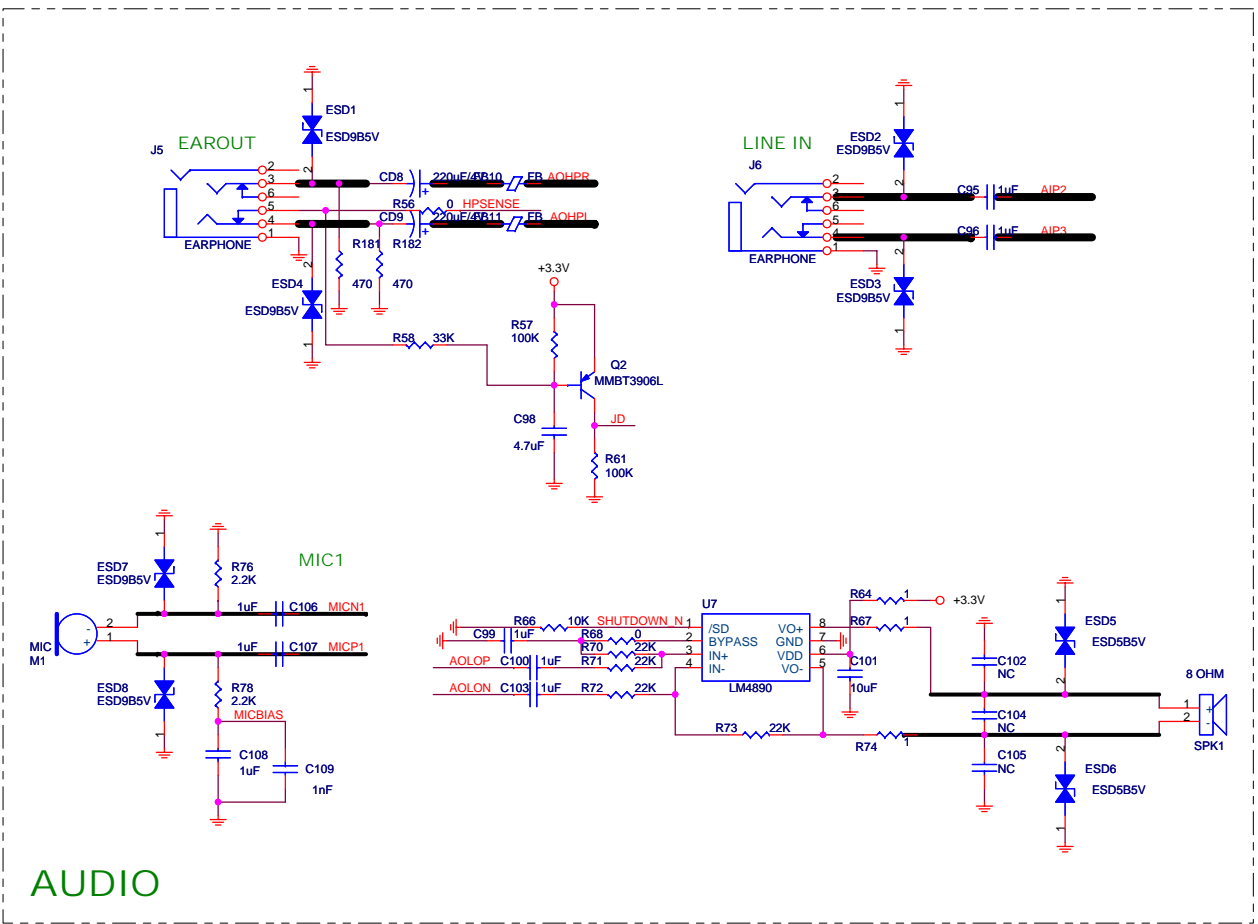
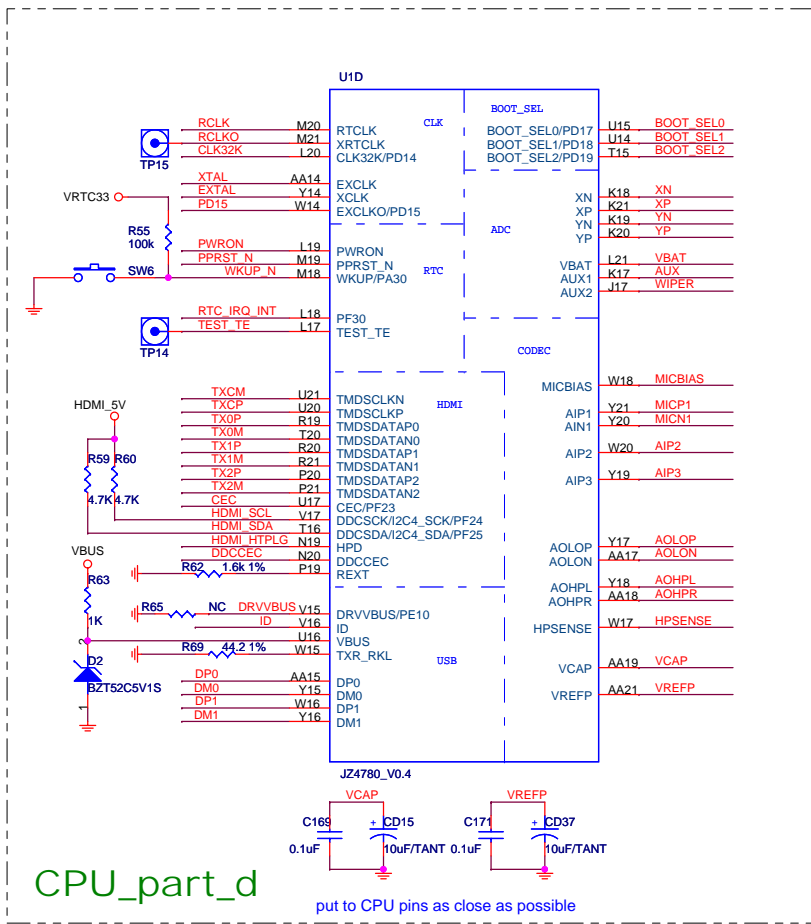
CPU_part_b

BT_RST_N	10	USB_DETE	11	SA0_CLE	10
WL_REG_ON	10	PMU_IRQ_N	7	SA1_ALE	10
BT_INT	10	KEY0	9	SA2	10
WL_PW_EN	10	KEY1	9	SA3	10
WL_WAKE	10	TS_INT0	10	SA4	10
BT_REG_ON	10	TS_INT1	10	SA5	10
BT_WAKE	10			ETHERNET_INT	10
				ETHERNET_RST	10
PCM_CLK	10	I2C0_SCK	8	RD_N	10
PCM_SYN	10	I2C0_SDA	8	WE_N	10
PCM_DI	10	I2C1_SCK	7	CS6_N	10
PCM_DO	10	I2C1_SDA	7	SD[0:7]	10
		I2C2_SCK	10	SD0_CD_N	8
TDO_TXD	10	I2C2_SDA	10	SD0_WP_N	8
TRST_N	10	I2C4_SCK	9,10	SD0_VCC_EN_N	8
TCK	10	I2C4_SDA	9,10		
TMS	10			DMIC_CLK	11
TDI_RXD	10	SSIO_CE1_N	10	DMIC_DOUT	11
		SSIO_CLK	10	DMIC_LR	11
		SSIO_DT	10		
		SSIO_DR	10	SHUTDOWN_N	6
		SSIO_CE0_N	10		

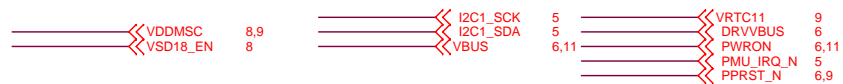
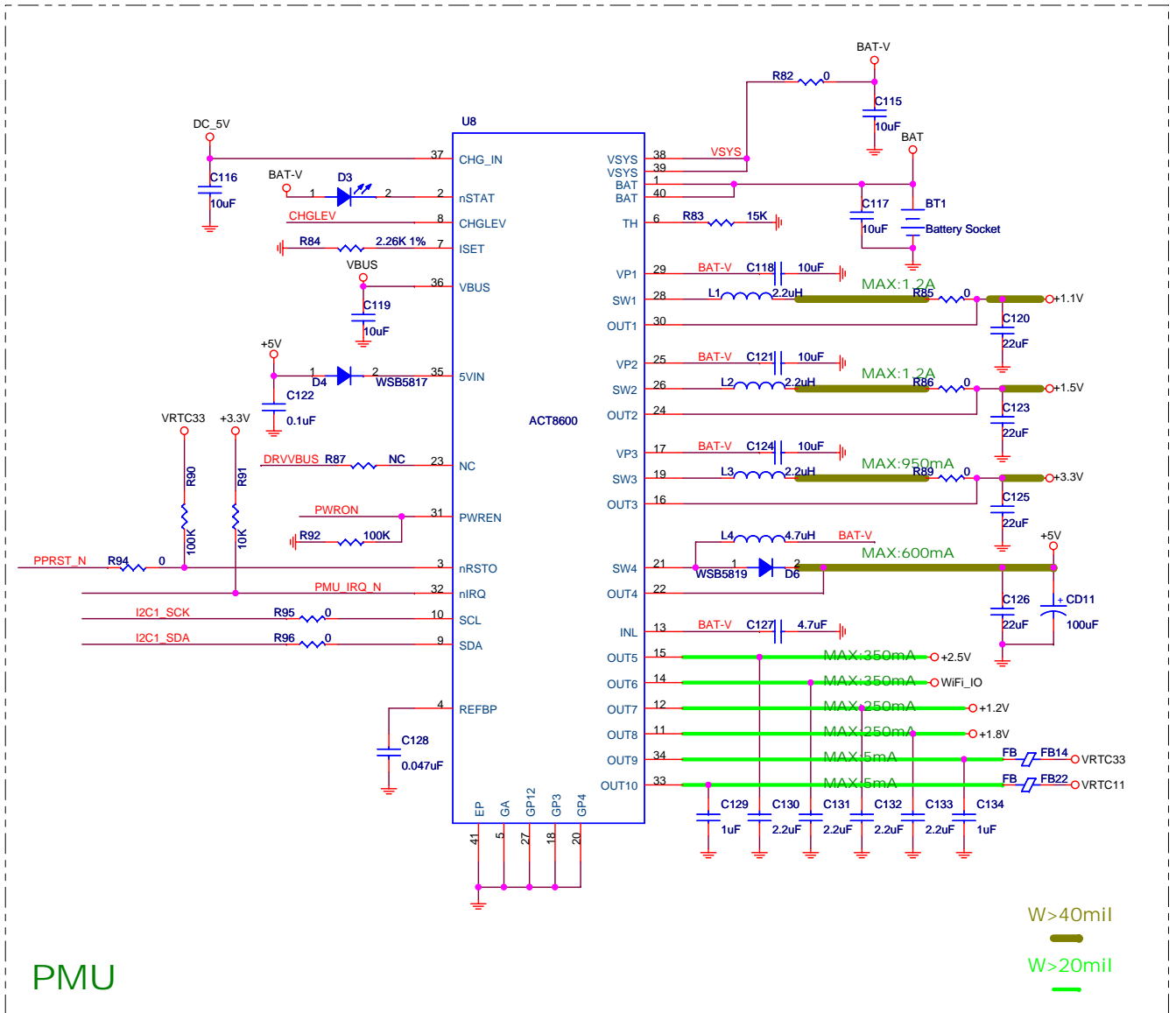
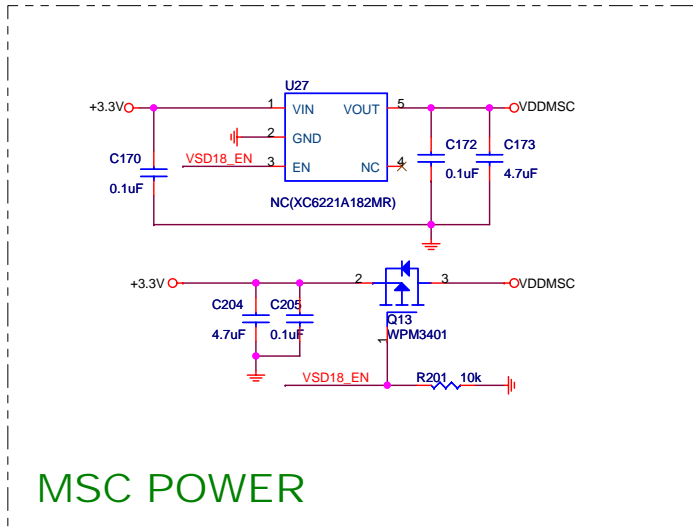
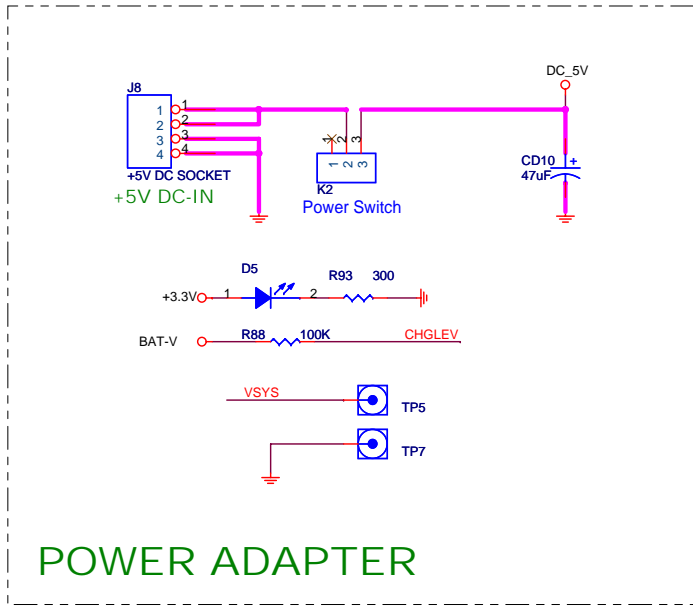


CAMERA

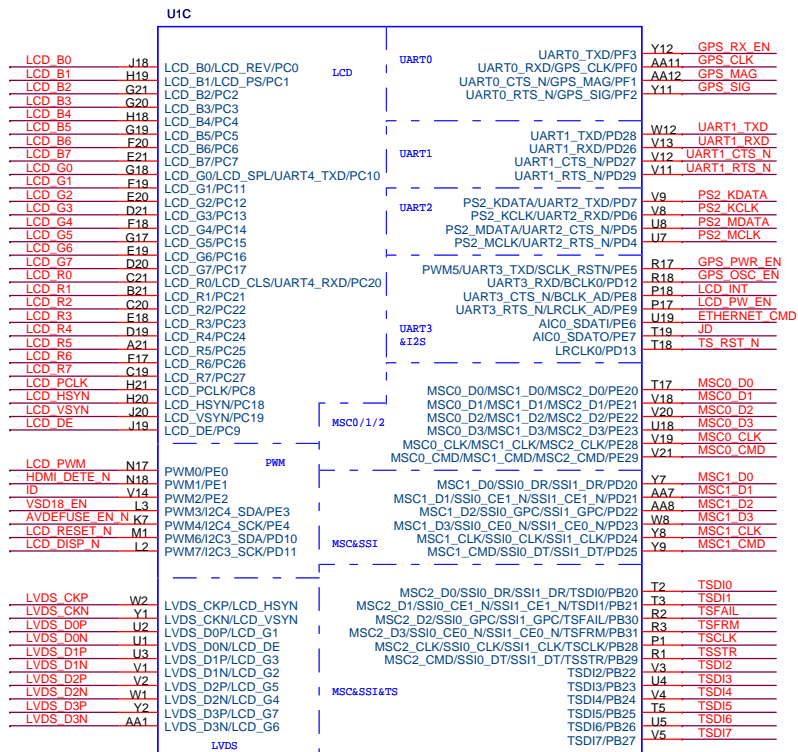
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RTC_IRQ_INT	9	PD15	10
ID	8	SHUTDOWN_N	5
XTAL	9	HDMI_DET_N	8
EXTAL	9	XP	8
BOOT_SEL2	9	XN	8
BOOT_SEL1	9	YP	8
BOOT_SEL0	9	YN	8
PPRST_N	7,9	DRVVBUS	7
DM0	11	WIPER	10
DP0	11	AIP2	7,11
ID	8,11	WIPER	10
USB_DET	5,11	AIP3	10
DM1	10	CLK32K	10
DP1	10		

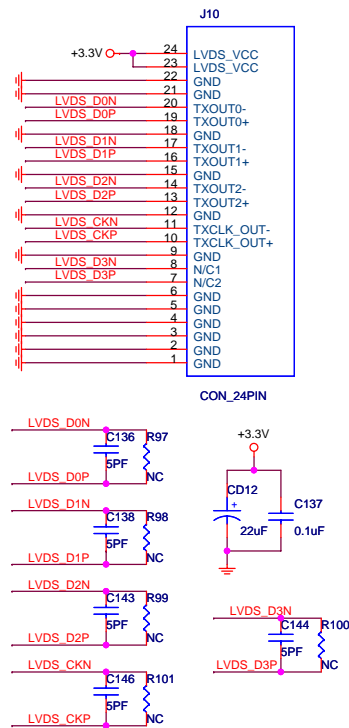


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Title RD4780_GRUS		
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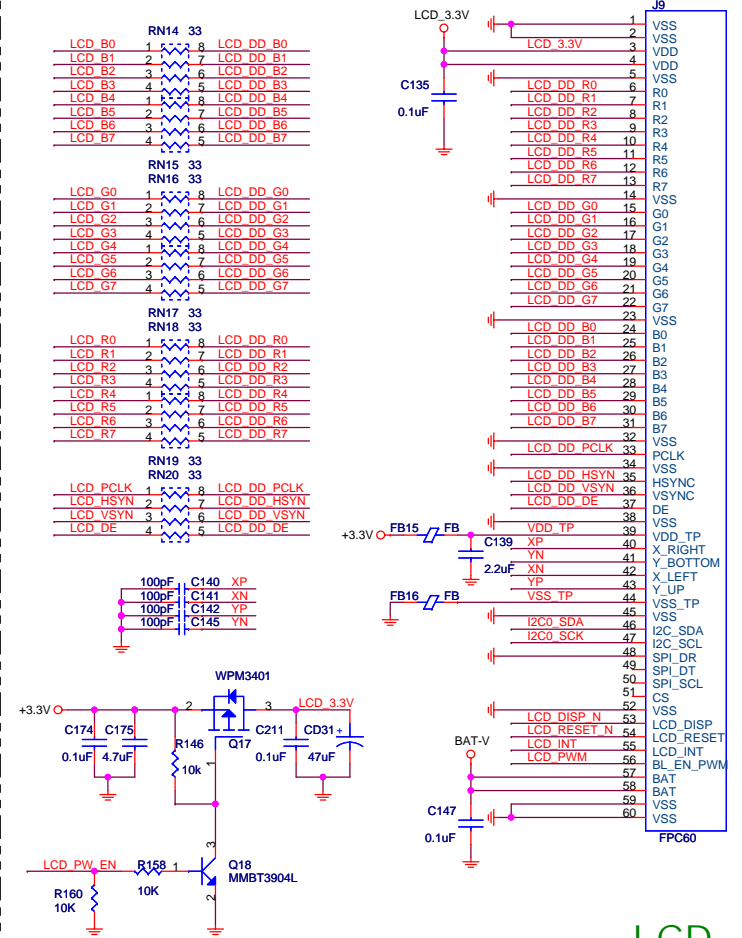


JZ4780_V0.4

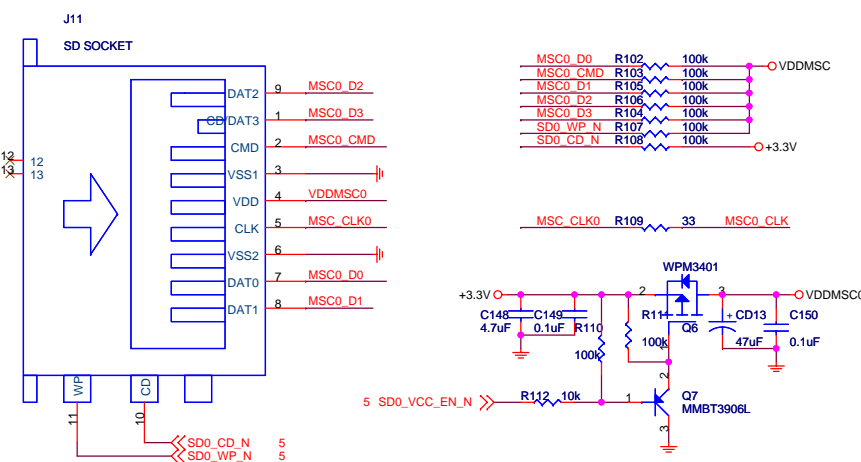
CPU_part_c



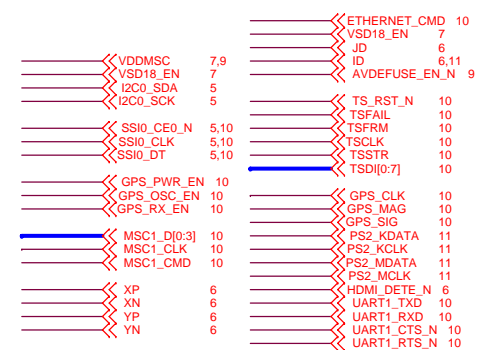
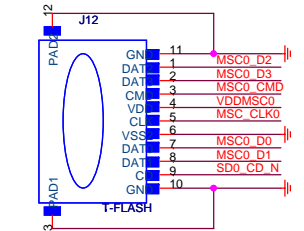
LVDS



LCD



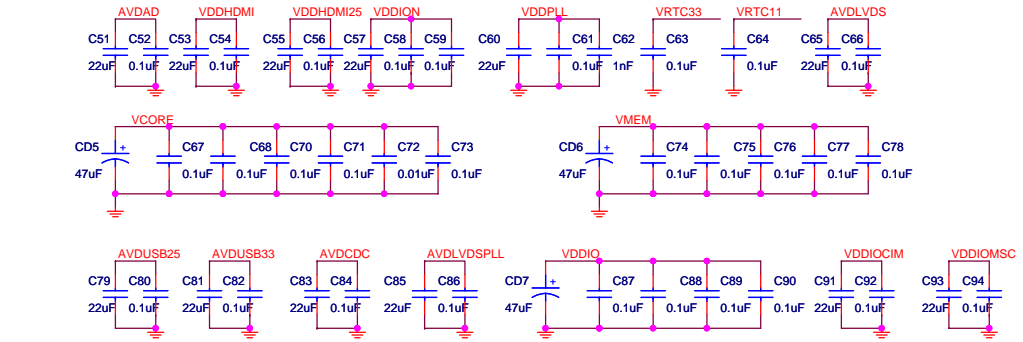
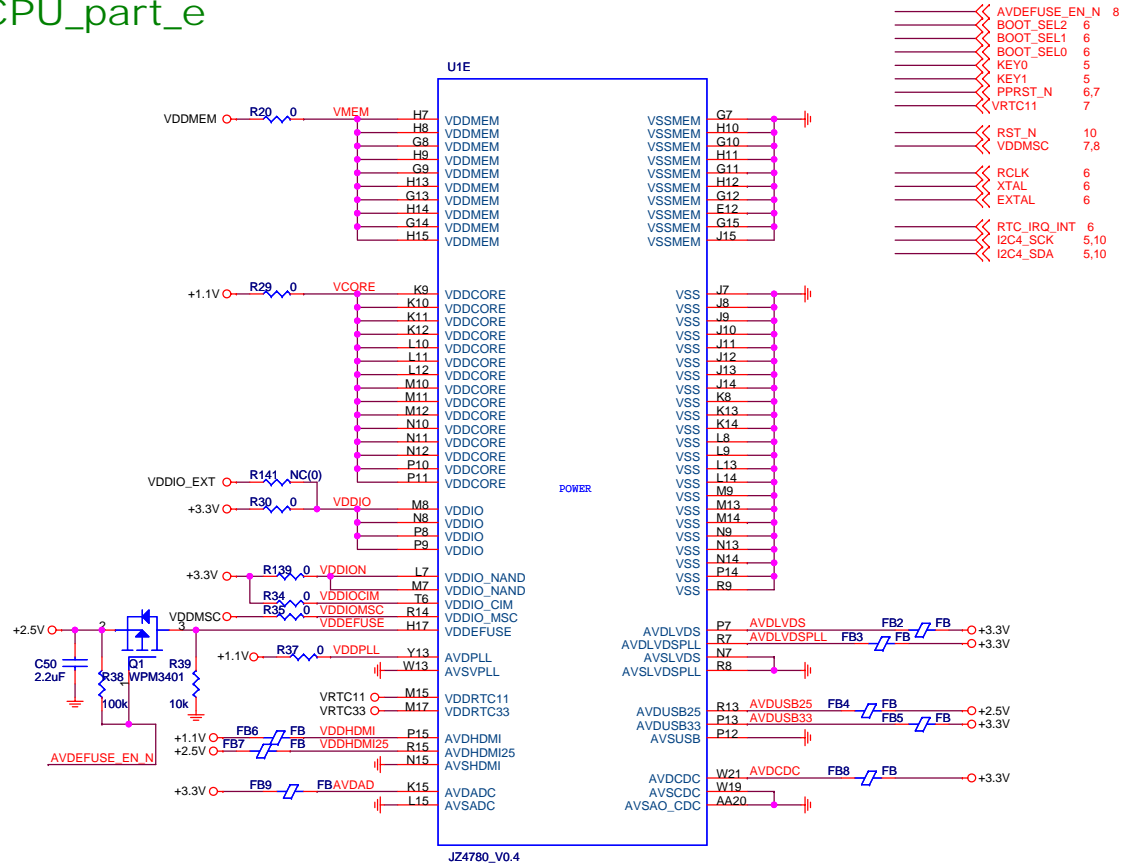
MMC0



INGENIC SEMICONDUCTOR CO.,LTD

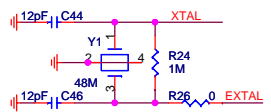
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CPU_part_e



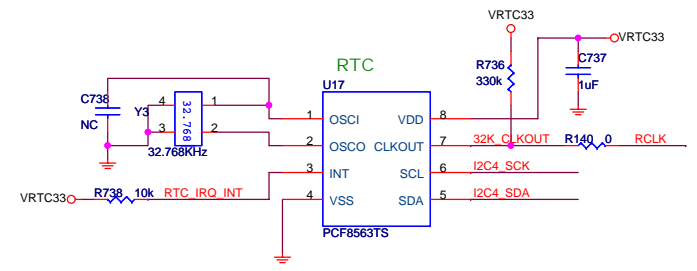
AVDEFUSE_EN_N	8
BOOT_SEL2	6
BOOT_SEL1	6
BOOT_SEL0	6
KEY0	5
KEY1	5
PPRST_N	6,7
VRTC11	7
RST_N	10
VDDMSC	7,8
RCLK	6
XTAL	6
EXTAL	6
RTC_IRQ_INT	6
I2C4_SCK	5,10
I2C4_SDA	5,10

MAIN CLOCK

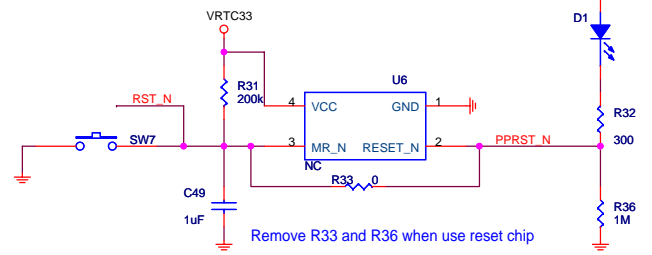


Boot Mode Select

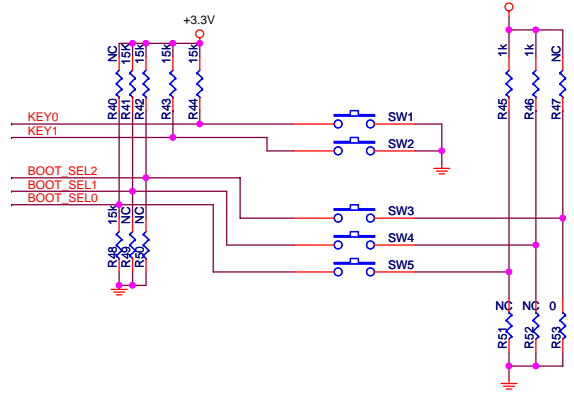
BOOT_SEL[2:1:0]	
111	USB Boot
110	NAND Boot
101	MSC0 Boot
000	SPI Boot
100	MSC1 Boot
011	eMMC Boot
010	NOR Boot(CS2)



RESET CIRCUITS

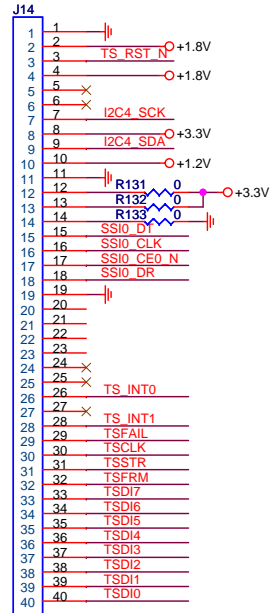


FUNCTION KEY

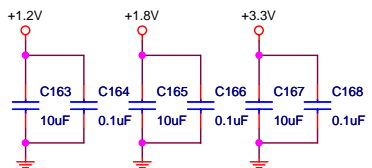


WL_REG_ON	5
BT_INT	5
WL_PW_EN	5
WL_WAKE	5
BT_REG_ON	5
BT_WAKE	5
TDO_TXD	5
TRST_N	5
TCK	5
TMS	5
TDI_RXD	5
RD_N	5
WE_N	5
CS6_N	5
SD[0:7]	5
ETHERNET_INT	5
ETHERNET_RST	5
ETHERNET_CMD	8
CS6_N	5
DM1	6
DP1	6
PCM_CLK	5
PCM_SYN	5
PCM_DI	5
PCM_DO	5
AIP2	6
AIP3	6
BT_RST_N	5
RST_N	9
GPS_PWR_EN	8
GPS_OSC_EN	8
GPS_RX_EN	8
GPS_CLK	8
GPS_MAG	8
GPS_SIG	8
MSC1_D[0:3]	8
MSC1_CLK	8
MSC1_CMD	8
PMU_IRQ_N	5,7
CS6_N	5
UART1_TXD	8
UART1_RXD	8
UART1_CTS_N	8
UART1_RTS_N	8
SSIO_CE0_N	5
SSIO_CE1_N	5
SSIO_CLK	5
SSIO_DT	5
SSIO_DR	5
TS_RST_N	8
PD15	6
TS_INT0	5
TS_INT1	5
TSFAIL	8
TSFRM	8
TSCLK	8
TSSTR	8
TSSTR	8
TSDI[0:7]	8
WIPER	6
I2C4_SCK	5,9
I2C4_SDA	5,9
I2C2_SCK	5
I2C2_SDA	5
I2C1_SCK	5,7
I2C1_SDA	5,7
SA0_CLE	5
SA1_ALE	5
SA2	5
SA3	5
SA4	5
SA5	5
CLK32K	6

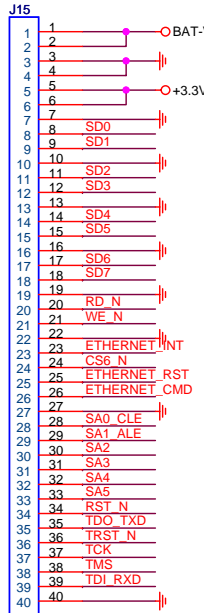
TS Interface Connector



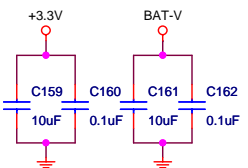
TS INTERFACE



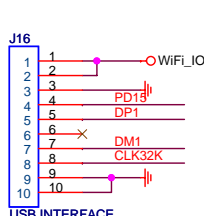
Ethernet & JTAG Interface



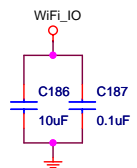
Ethernet & JTAG



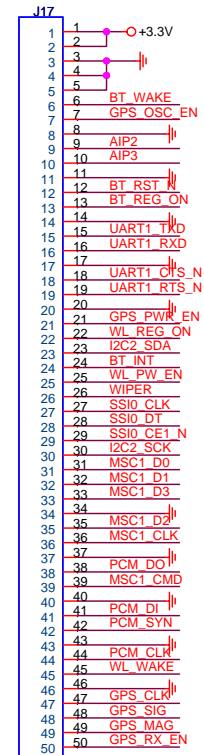
USB Interface



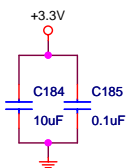
USB INTERFACE



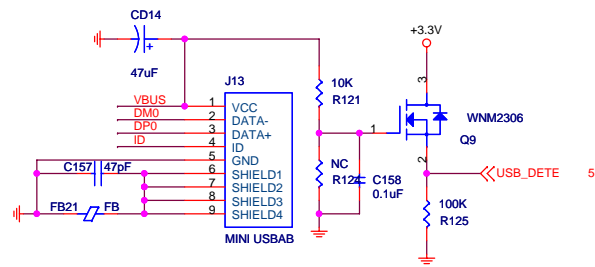
WiFi & GPS Interface



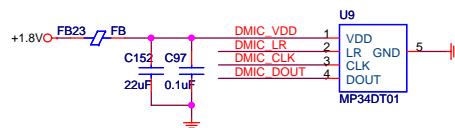
WiFi&GPS



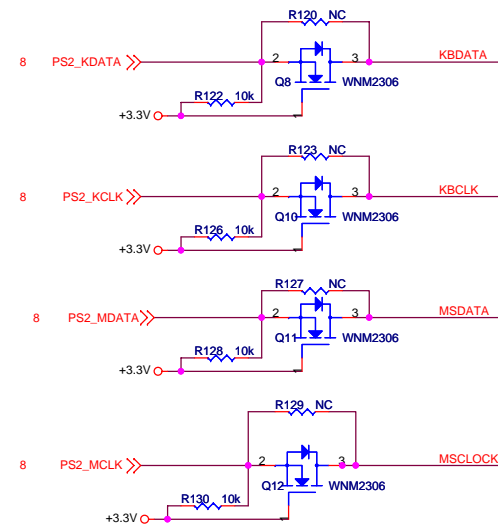
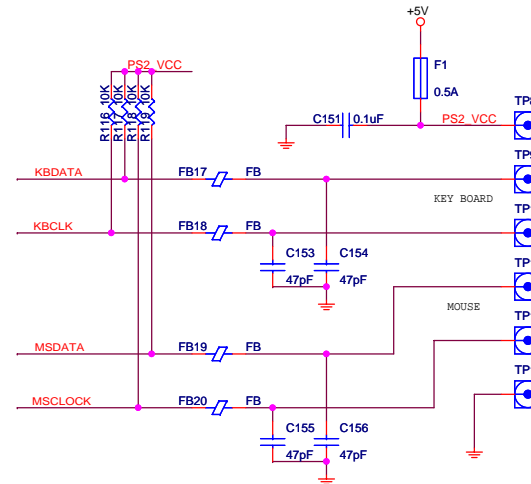
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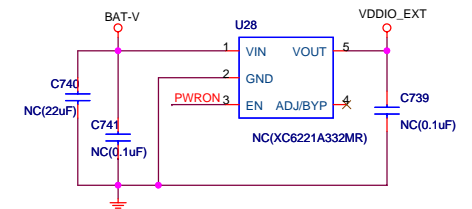
USB2.0_OTG



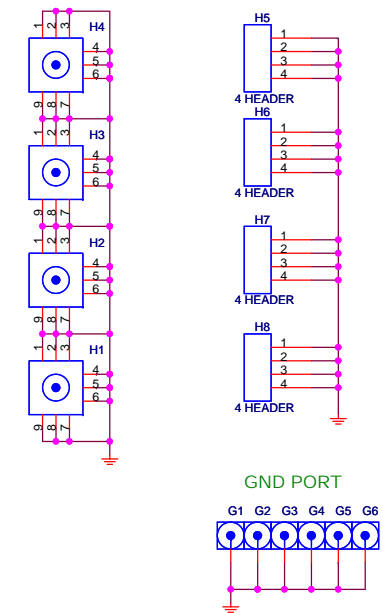
Digital microphone



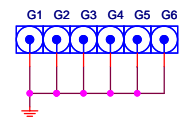
PS2 PORT



VDDIO_EXT



GND PORT



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Data Revision Change

Data	Revision	Change
Aug 28 2012	Rev1.0	1. First Revision
Dec 29 2012	Rev1.0.2	1. PAGE05: Delete R18 and connect SHUTDOWN_N to CPU PIN E4. 2. PAGE06: Change the footprint of Audio connector J5 & J6 3. PAGE06: Change the footprint of D2. 4. PAGE07: Change OUT2 to 1.5V and OUT3 to 3.3V. Change the OUT1,OUT2,OUT3 net to the back of resistors. 5. PAGE07: Change MSC power chip U27 to XC6221A182MR and NC 6. PAGE08: Change the schematic and PCB package of J11. 7. PAGE09: Change R736 from 10K to 330K to reduce hibernate current. 8. PAGE09: Change R31 from 10K to 200K, R36 from 100K to 1M, C49 from 0805 4.7uF to 0603 1uF, in order to reduce hibernate current.

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