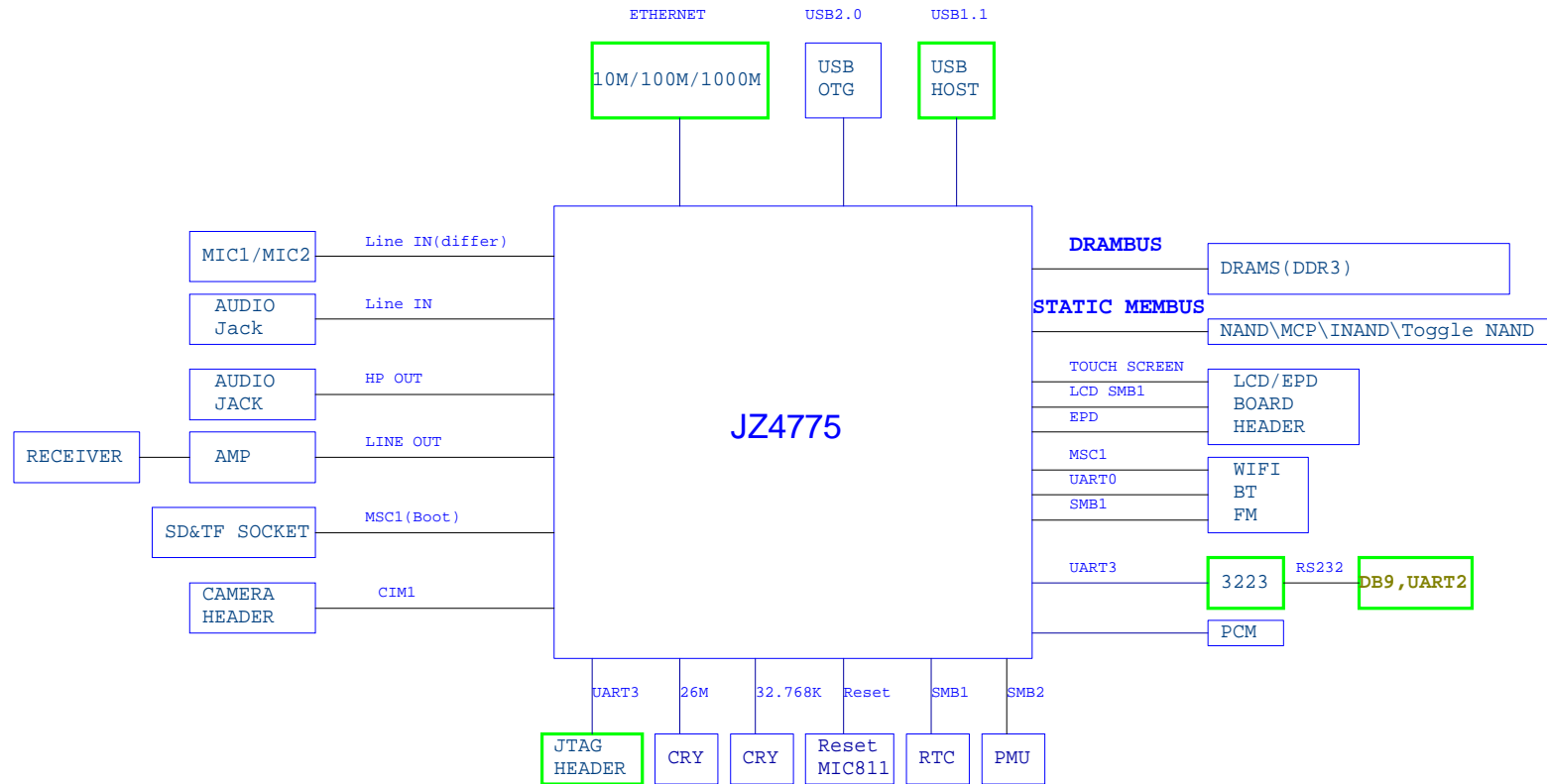




RD_JZ4775_MENSA_BOARD

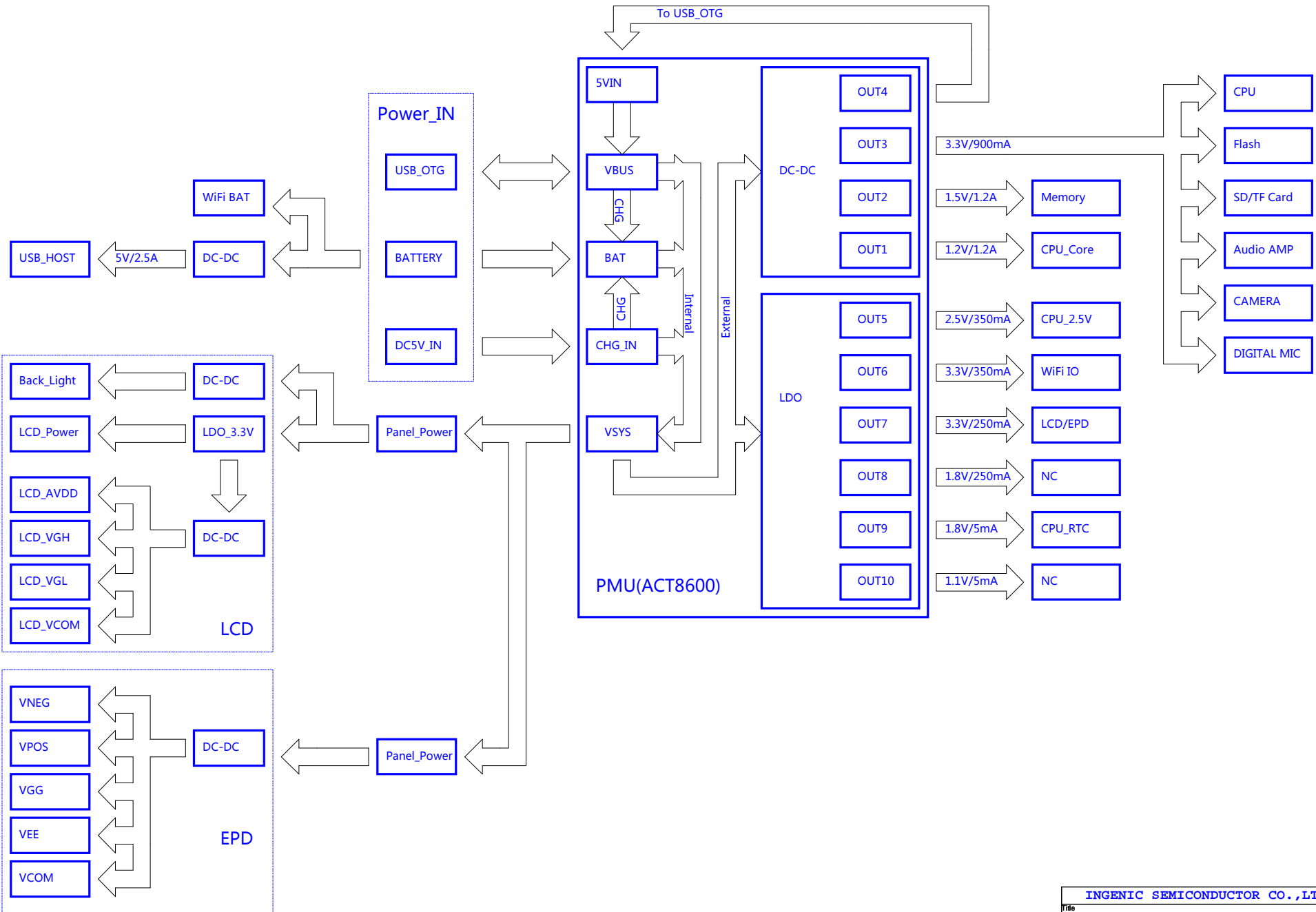
Schematic Revision 1.0.1

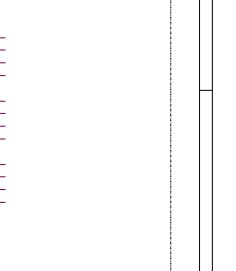
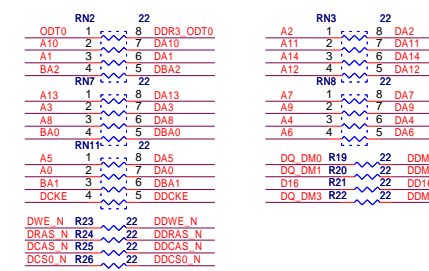
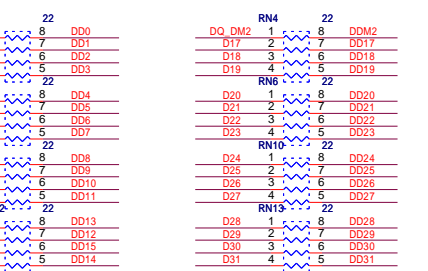
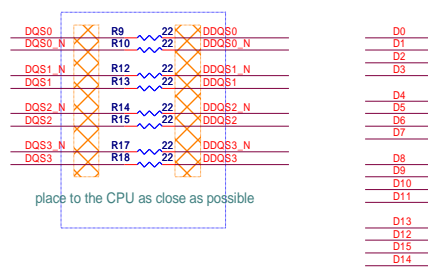
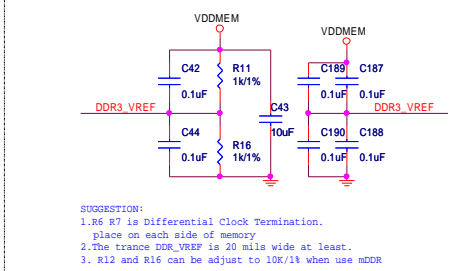
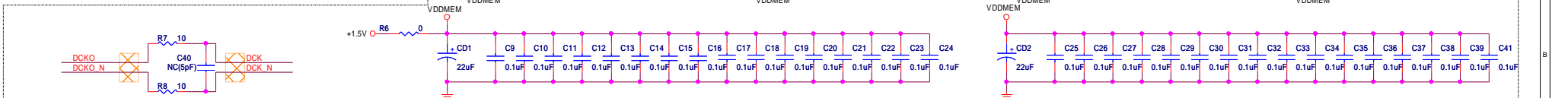
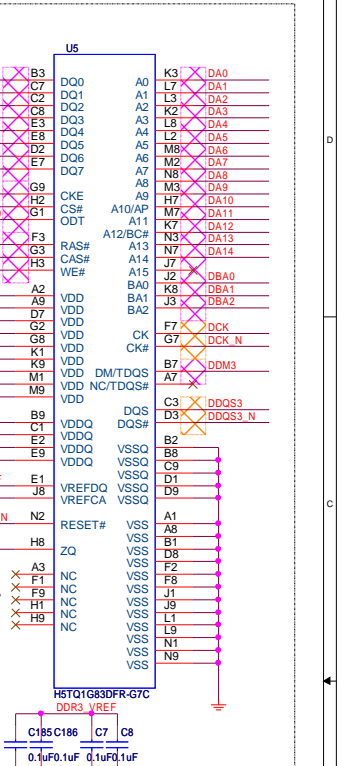
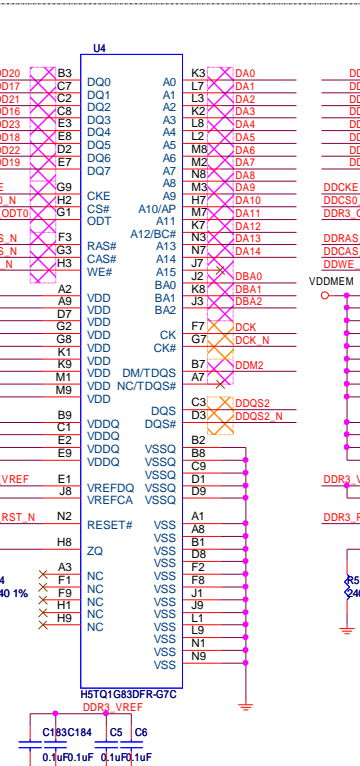
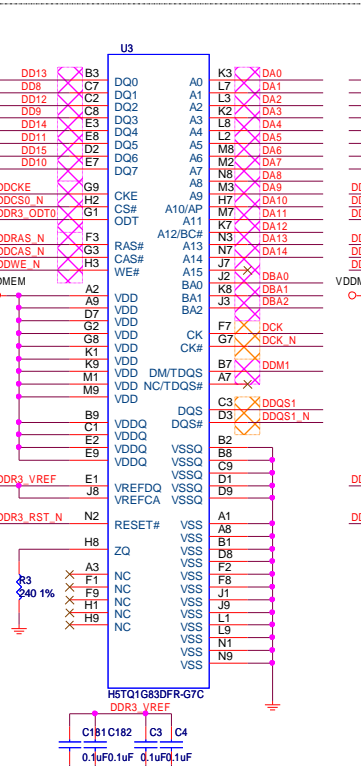
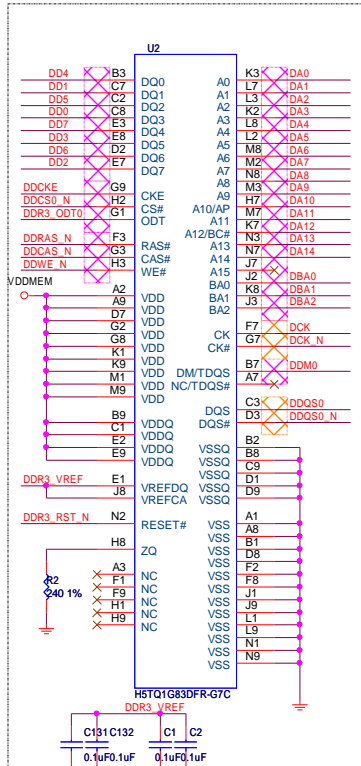
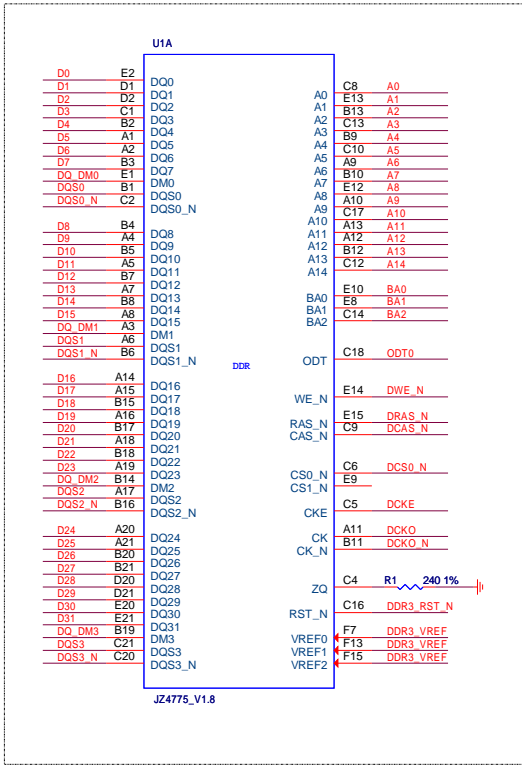
Title	Page
COVER SHEET	1
SYSTEM ARCHITECTURE	2
POWER ARCHITECTURE	3
DDR3	4
Nand/Camera	5
AUDIO/KEY	6
RTC	7
LCD/EPD	8
PMU	9
IW8101/IW8103	10
IW8103B/MT5913	11
USB OTG/SD CARD/PCM	12
DEBUG	13
HISTORY	14



The green cloor is the debug board

INGENIC SEMICONDUCTOR CO.,LTD			
Title RD_JZ4775_MENSA_BOARD			
Size A3	Document Number SYSTEM ARCHITECTURE	Rev V1.0.1	
Date: Monday, March 11, 2013	Sheet 2	of 14	





- SUGGESTION:
1. R6 R7 is Differential Clock Termination, place on each side of memory.
 2. The trance DDR_VREF is 20 mils wide at least.
 3. R12 and R16 can be adjust to 10K/1% when use mDDR

Differential pairs Z0= 100 ohm
Equi long BUS Z0= 50 ohm

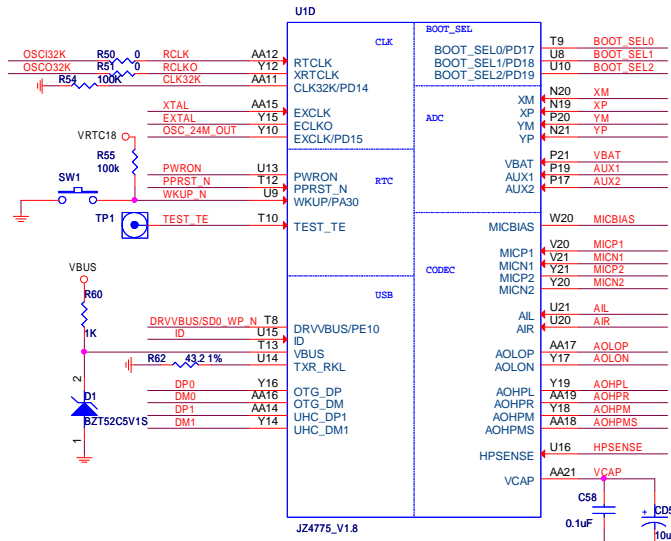
DDR3

INGENIC SEMICONDUCTOR CO.,LTD

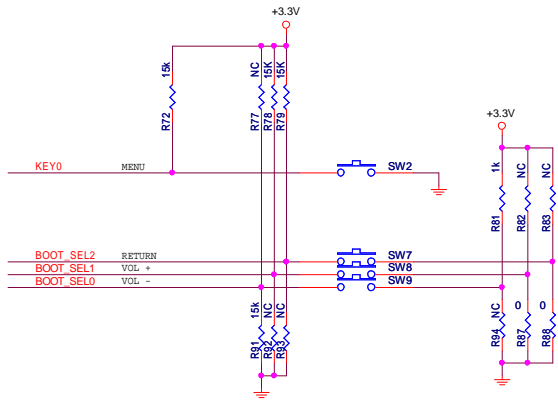
Title: RD_JZ4775_MENSA_BOARD

Size: A3 Document Number: DDR3 Rev: V1.0.1

Date: Monday, March 11, 2013 Sheet: 4 of 14

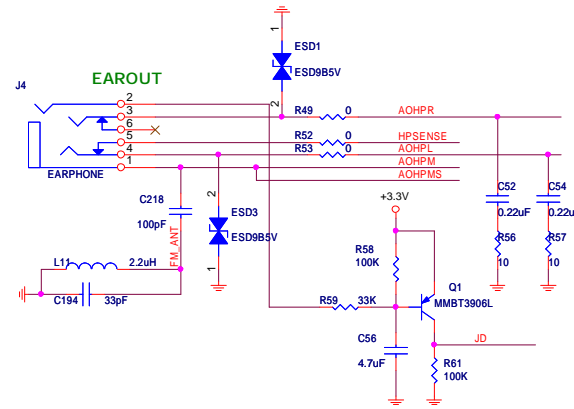
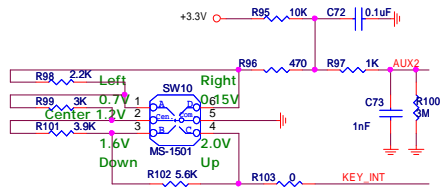


FUNCTION KEY

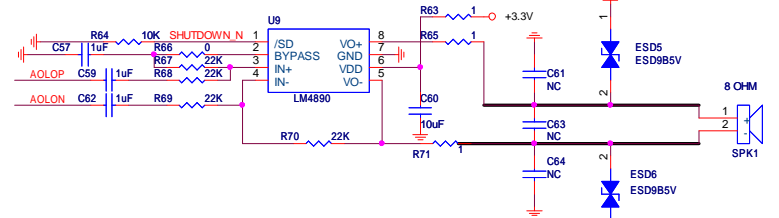
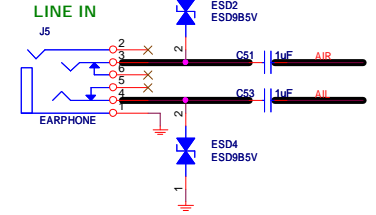


Boot Mode Select

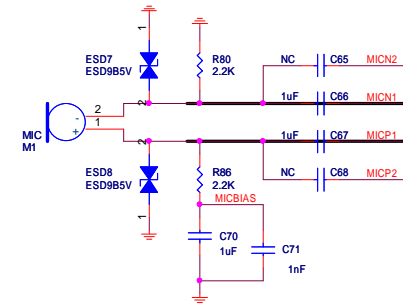
BOOT_SEL[2:1:0]	BOOT FROM
111	USB Boot
110	NAND Boot
101	MSC0 Boot
000	SPI Boot
100	MSC1 Boot
011	eMMC Boot
010	NOR Boot (CS2)



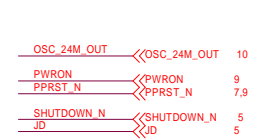
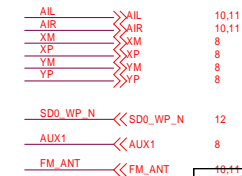
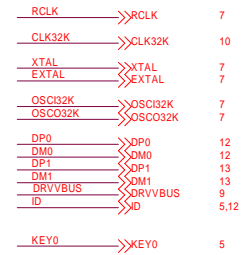
The AOHMS and AOHPM must be connected at terminate, near the headphone Jack



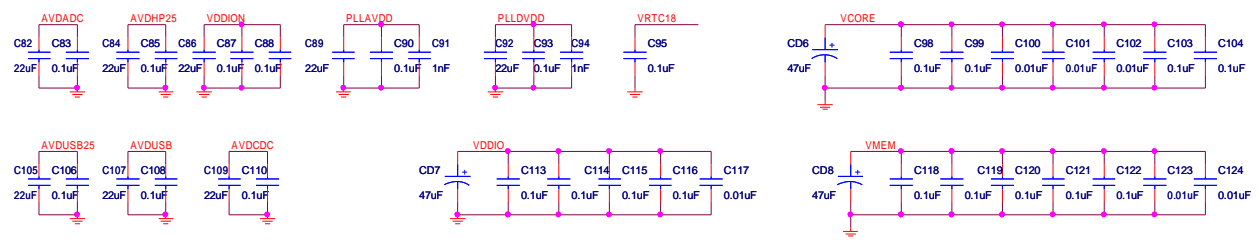
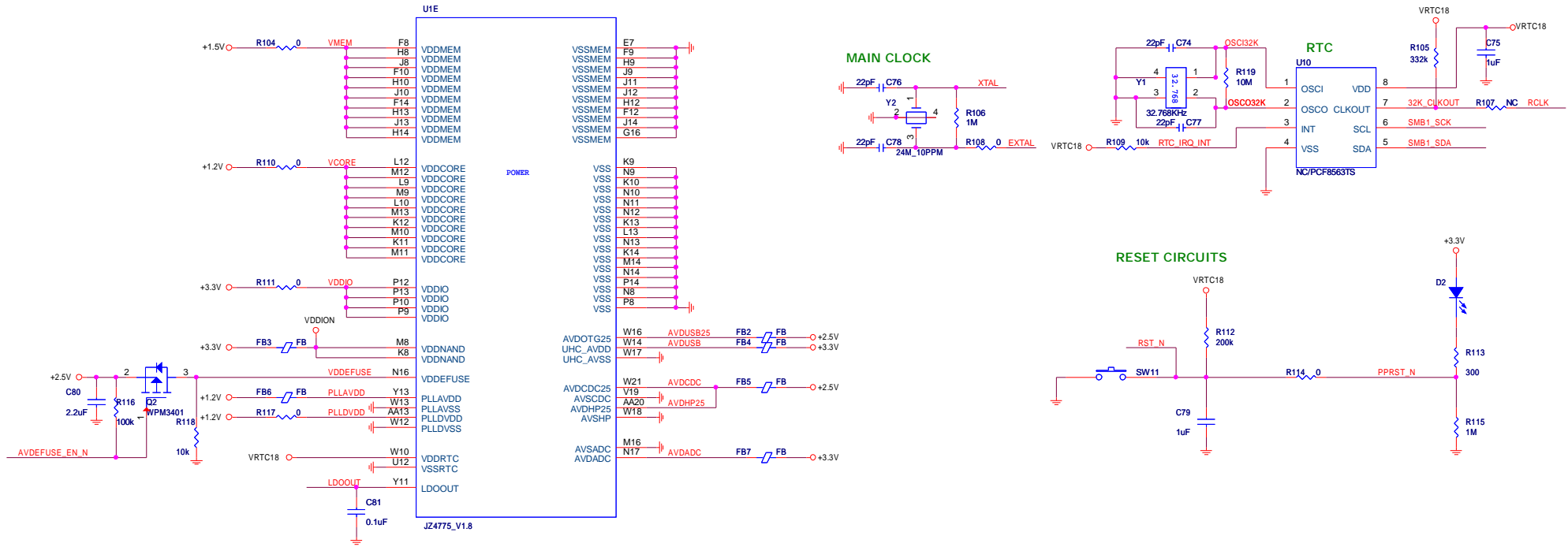
MIC1 MIC2



AUDIO

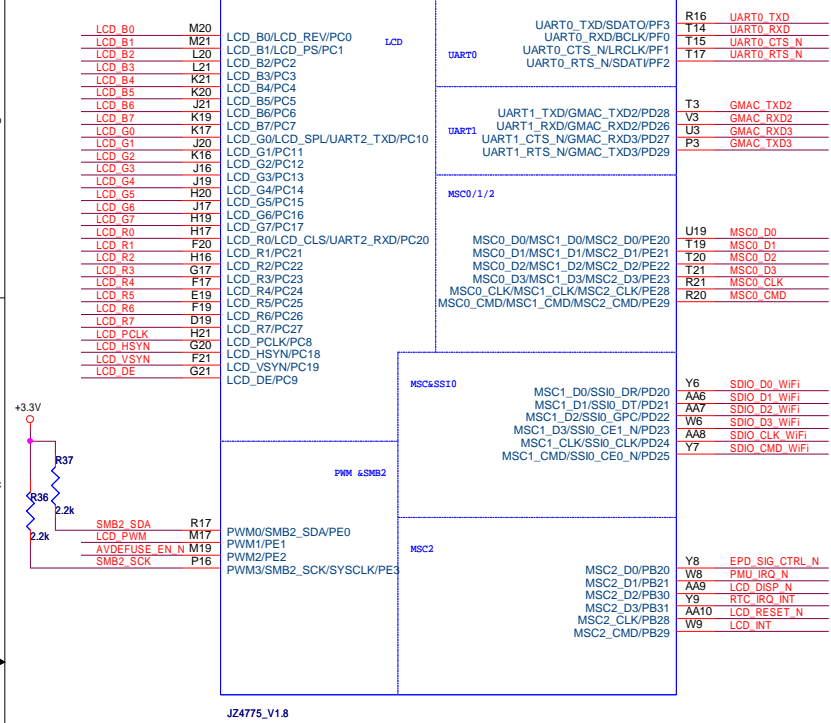


INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD_JZ4775_MENSA_BOARD	
Size	Document Number	Rev
A3	AUDIOKEY	V1.0.1
Date:	Monday, March 11, 2013	Sheet 6 of 14



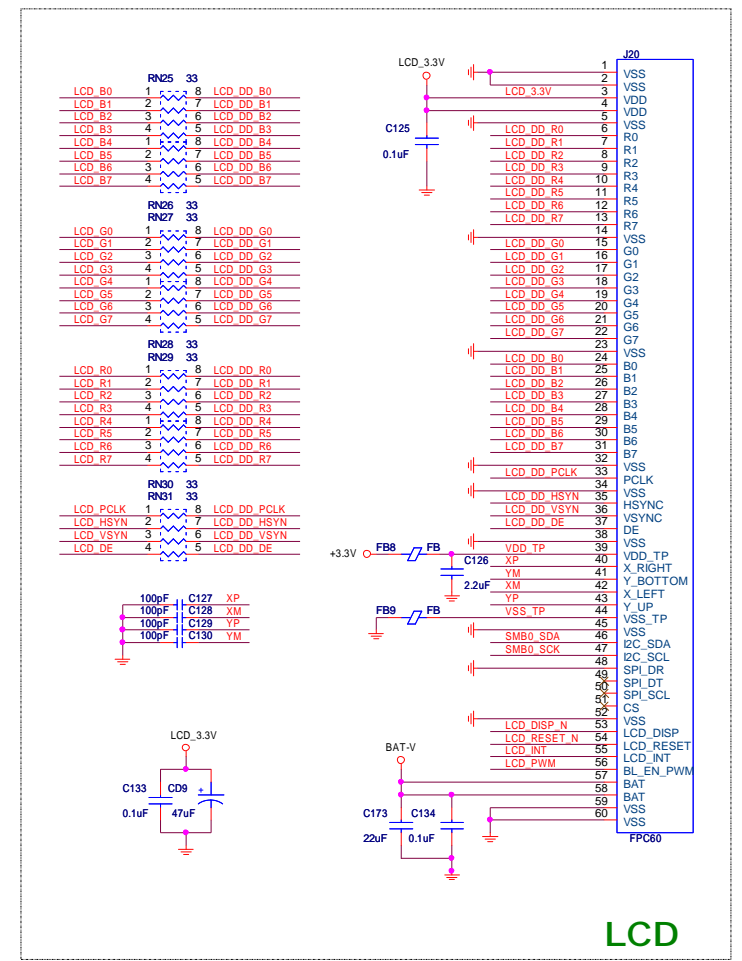
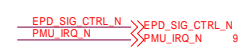
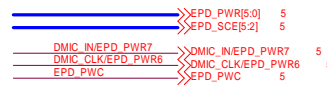
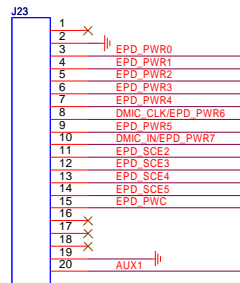
AVDEFUSE_EN_N	8
XTAL	6
EXTAL	6
OSC032K	6
OSC032K	6
SMB1_SCK	5,10
SMB1_SDA	5,10
RTC_IRQ_INT	9
RCLK	6
RST_N	13
PPRST_N	6,9

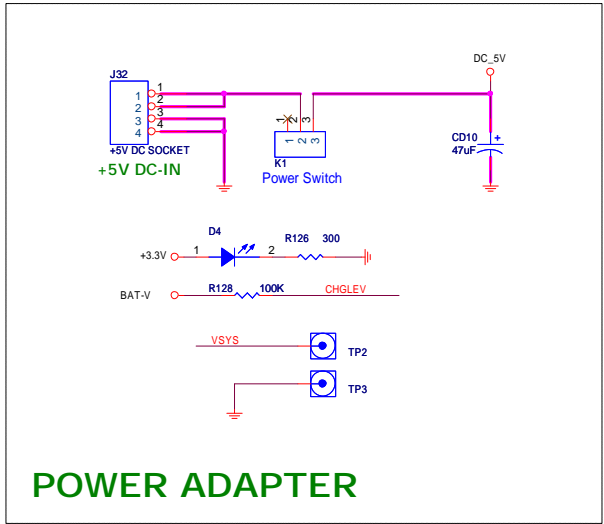
UIC



JZ4775_V1.8

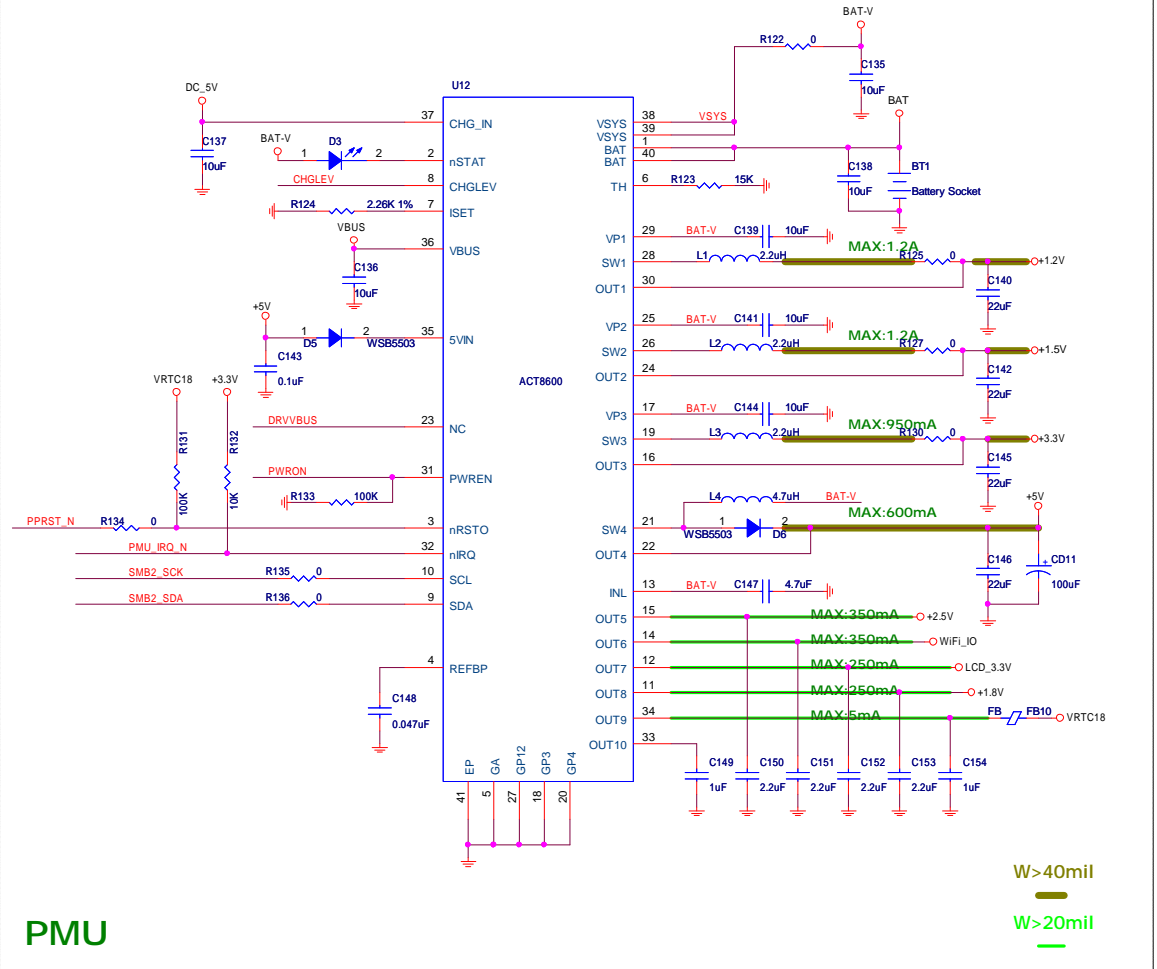
EPD Connector





POWER ADAPTER

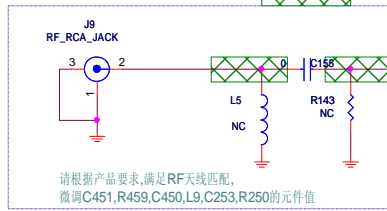
- PPRST_N << PPRST_N 6,7
- PMU_IRQ_N << PMU_IRQ_N 8
- SMB2_SCK << SMB2_SCK 8
- SMB2_SDA << SMB2_SDA 8
- PWRON << PWRON 6
- DRVVBUS << DRVVBUS 6



PMU

INGENIC SEMICONDUCTOR CO.,LTD		
Title	RD_JZ4775_MENSA_BOARD	
Size	Document Number	Rev
A3	PMU	V1.0.1
Date:	Monday, March 11, 2013	Sheet 9 of 14

RF Microstrip
Z0= 50 ohm



请根据产品要求,满足RF天线匹配,
微调C451,R459,C450,L9,C253,R250的元件值

请根据晶体要求,满足实际测试
+/-10PPM误差范围,
微调C252,C256的元件值,
Layout时晶振下方不能走线

Please note the input/output
direction of UART interface,
IW8103's input should connect to
the output of host, and
IW8103's output should connect
to input of host.

Please note the input/output
direction of PCM
interface, IW8103's input should connect to the
output of host, and IW8103's output should
connect to input of host.

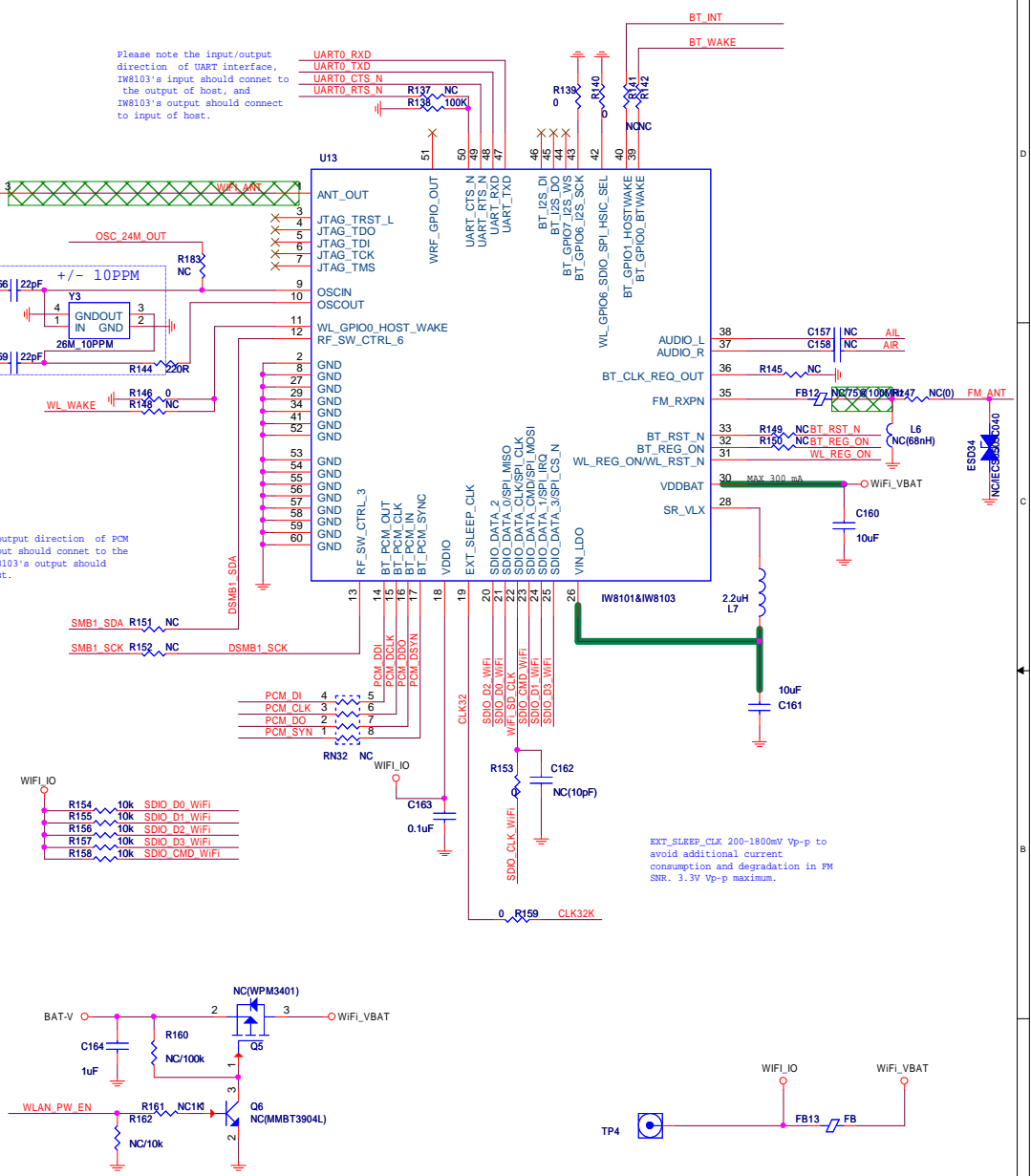
Component select in IW8101 & IW8103

Part Number	IW8103	IW8101
	value	
C157,C158	1uF	NC
C164	1uF	NC
ESD34	TESB0R15V05B1X	NC
FB12	75@100MHz	NC
FB13	NC	75@100MHz
L7	2.2uH	1.5uH
Q5	WPM3401	NC
Q6	MMBT3904L	NC
RN32	0 OHM	NC
R138	NC	100K OHM
R139,R146	NC	0 OHM
R137,R141,R142,R147 R148,R149,R150	0 OHM	NC
R160	100K OHM	NC
R162	10K OHM	NC
R161	1K OHM	NC
U14	0 OHM	MURATA BPF LFB182G45CL3D264
Y3	37.4MHz, +/-10ppm	26MHz, +/-10ppm

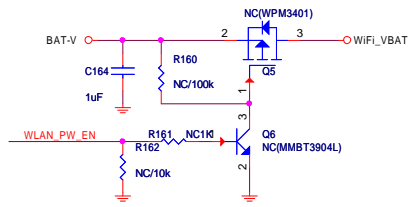
备注
使用IW8103, WIFI_IO电压调整为2.8V,同时系统的3.3V也调整为2.8V
清单内无标识的物料为共用料, 请按原理图标识值进行选择

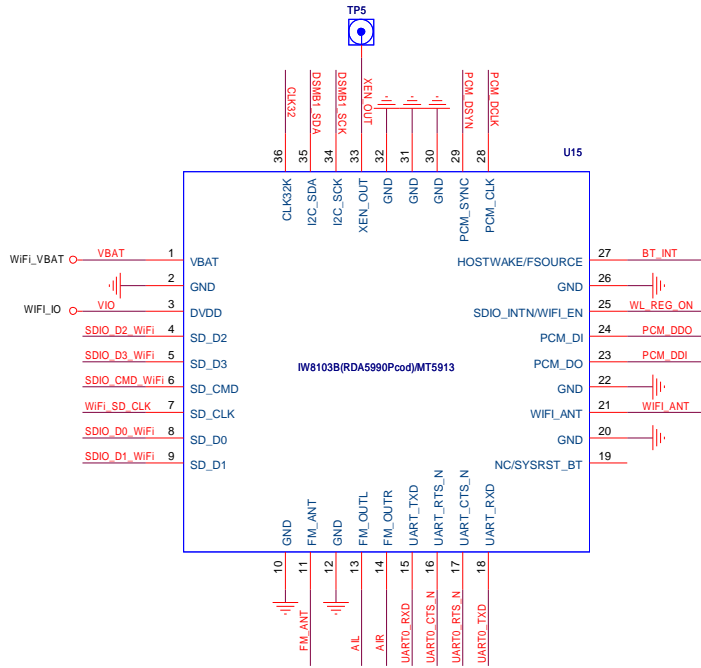
器件编号	IW8103	IW8103B
Y3	37.4MHz +/- 10ppm	26MHz +/- 10ppm
C157,C158	1uF	0.1uF
R151,R152	NC	0R
L7	2.2uH	4.7uH
FB12	75@100MHz Bead	100pF CAP
R140,R142	0R	NC

- 6 OSC_24M_OUT >>
- 8.11 SDIO_D0_WIFI >>
- 8.11 SDIO_D1_WIFI >>
- 8.11 SDIO_D2_WIFI >>
- 8.11 SDIO_D3_WIFI >>
- 8.11 SDIO_CMD_WIFI >>
- 8 SDIO_CLK_WIFI >>
- 6 CLK32K >>
- 5.12 PCM_DI >>
- 5.12 PCM_DO >>
- 5.12 PCM_SYN >>
- 5.12 PCM_CLK >>
- 5 WL_WAKE >>
- 5.11 WL_REG_ON >>
- 5 BT_REG_ON >>
- 5 BT_WAKE >>
- 5.11 BT_INT >>
- 5 BT_RST_N >>
- 8.11 UART0_RXD >>
- 8.11 UART0_TXD >>
- 8.11 UART0_CTS_N >>
- 8.11 UART0_RTS_N >>
- 5 WLAN_PW_EN >>
- 6.11 AIL >>
- 6.11 AIR >>
- 5.7 SMB1_SDA >>
- 5.7 SMB1_SCK >>
- 11 WIFI_ANT >>
- 6.11 FM_ANT >>
- 11 CLK32 >>
- 11 WIFI_SD_CLK >>
- 11 PCM_DDI >>
- 11 PCM_DDO >>
- 11 PCM_DSYN >>
- 11 PCM_DCLK >>
- 11 DSMB1_SDA >>
- 11 DSMB1_SCK >>

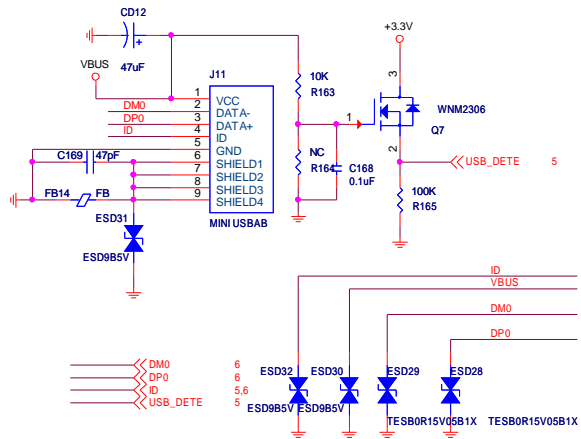


WIFI Power

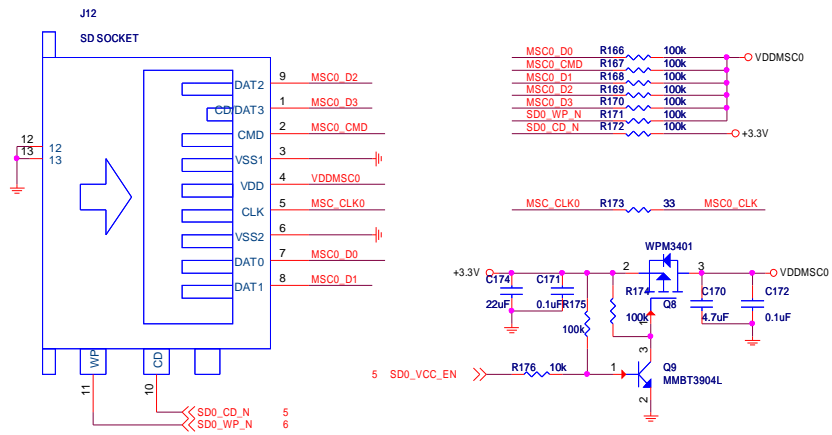
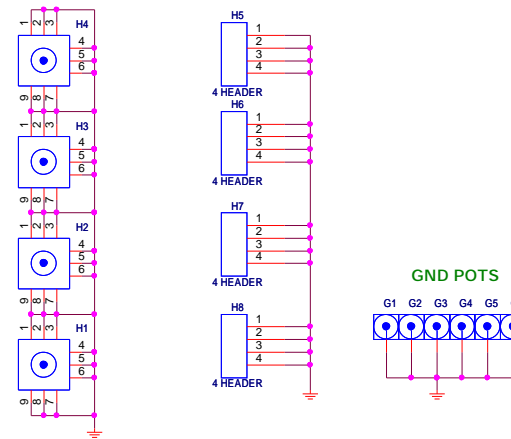




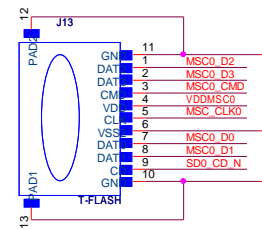
- 8,10 SDIO_D0_WIFI
- 8,10 SDIO_D1_WIFI
- 8,10 SDIO_D2_WIFI
- 8,10 SDIO_D3_WIFI
- 8,10 SDIO_CMD_WIFI
- 10 WiFi_SD_CLK
- 10 CLK32
- 5,10 WL_REG_ON
- 5,10 BT_INT
- 8,10 UART0_RXD
- 8,10 UART0_TXD
- 8,10 UART0_CTS_N
- 8,10 UART0_RTS_N
- 6,10 AIL
- 6,10 AIR
- 10 WiFi_ANT
- 6,10 FM_ANT
- 10 PCM_DDI
- 10 PCM_DDI
- 10 PCM_DSYN
- 10 PCM_DCLK
- 10 DSMB1_SDA
- 10 DSMB1_SCK



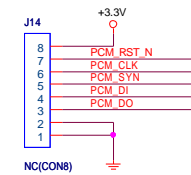
USB2.0_OTG



MMC0

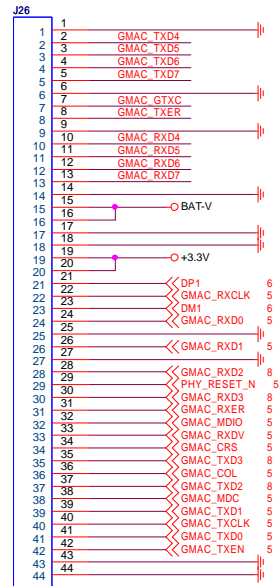


PCM CODEC CONNECT

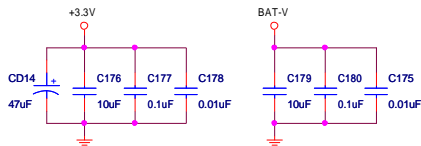


PCM_DI	>>	PCM_DI	5.10
PCM_DO	>>	PCM_DO	5.10
PCM_SYN	>>	PCM_SYN	5.10
PCM_CLK	>>	PCM_CLK	5.10
PCM_RST_N	>>	PCM_RST_N	5
MSC0_D0	>>	MSC0_D0	8
MSC0_D1	>>	MSC0_D1	8
MSC0_D2	>>	MSC0_D2	8
MSC0_D3	>>	MSC0_D3	8
MSC0_CLK	>>	MSC0_CLK	8
MSC0_CMD	>>	MSC0_CMD	8
SD0_CD_N	>>	SD0_CD_N	5
SD0_WP_N	>>	SD0_WP_N	6
SD0_VCC_EN	>>	SD0_VCC_EN	5

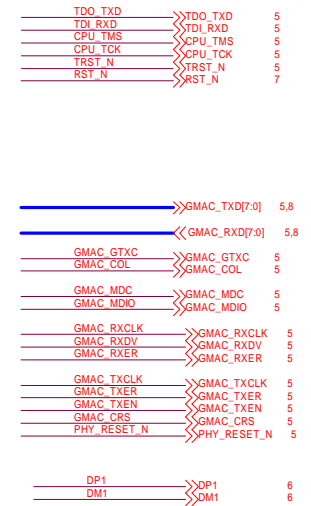
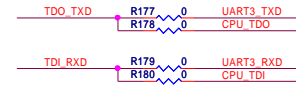
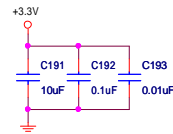
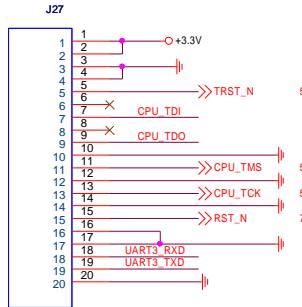
Ethernet & USB Con



Ethernet & USB Con



JDI & Uart Con



Data	Revision	Change
------	----------	--------

Jan 8 2013	Rev1.0	1. First Revision
Feb 28 2013	Rev1.0.1	<ol style="list-style-type: none"> 1. PAGE06: Change the Package of D1 2. PAGE06: R82 change to NC&R87 change to 0R 3. PAGE07: The power of AVDADC connect to +3.3V 4. PAGE07: Add R119 for 32.768k crystal 5. PAGE07: Delete the reset IC U11 6. PAGE10: Q6 change to NC 7. Change the power of VRTC from VRTC33 TO VRTC18 for save power 8. Change out1 of PMU to +1.2V 9. Connect the J12.12&J12.13 to GND 10. Change the package of U1 11. Change R62 from 44.2R 1% to 43.2R 1%. 12. Change all the I2C net name to SMB, such as SMB0_SCK etc.