Ingenic® JZ4775

Board Design Guide

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Release history

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Content

1 Overview

JZ4775 is a mobile application processor targeting for multimedia rich and mobile devices like tablet computer, EBook, mobile digital TV. This SOC introduces a kind of innovative architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices. JZ4775 provides high-speed CPU computing power and fluent 720p video replay.

The CPU (Central Processing Unit) core, equipped with 16kB instruction and 16kB data level 1 cache, and 256kB level 2 cache, operating at 1GHz, and full feature MMU function performs OS related tasks.

At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. The SIMD instruction set implemented by XBurst® engine, in together with the on chip video accelerating engine and post processing unit, delivers high video performance. The maximum resolution of 720p in the formats of H.264, VC-1, MPEG-1/2, MPEG-4, RealVideo and VP8 are supported in decoding.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or up to 64-bit ECC MLC/TLC NAND flash memory and toggle NAND flash for cost sensitive applications. It provides the interface to DDR2, DDR3 and LPDDR memory chips with lower power consumption.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. The LCD controller support regular RGB, 1024x768 output, WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG and USB 1.1 host, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Introduction

This design guide provides recommendations for system designs based on the JZ4775 processor. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor.

The design guidelines in this document are used to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** It is based on INGENIC's simulations and lab experience to date are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by

INGENIC. They should be used as an example, but may not be applicable to particular designs.

Note: In this manual, processor means the JZ4775 processor if not specified.

The guidelines recommended in this manual are based on experience and simulation work completed by INGENIC while developing systems with JZ4775. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

1.2 Reference Platform

Figure 1-1 shows the JZ4775 Development Board Architecture.

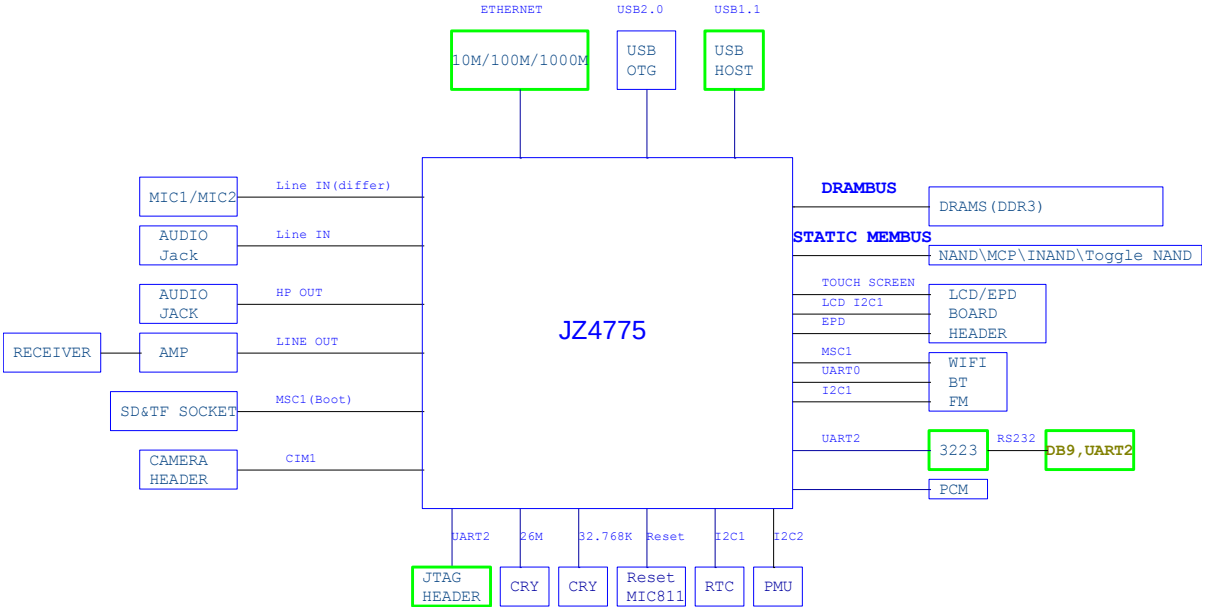


Figure 1-1 JZ4775 Development Board Architecture

2 Platform Stack-Up and Placement

In this section, an example of a JZ4775 platform component placement and stack-up is presented for a PMP product.

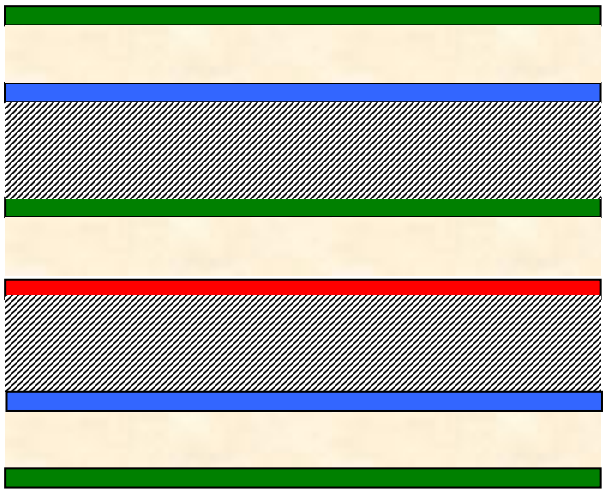
2.1 General Design Considerations

This section describes motherboard layout and routing guidelines for JZ4775 platforms. This section does not describe the function of any bus, or the layout guidelines for an add-in device. If the guidelines listed in this manual are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., 50Ω ± 10%) is the nominal trace impedance for a 4-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time. Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 2-1.

2.2 Nominal 6-Layer Board Stack-Up

The JZ4775 platform requires a board stack-up yielding a target board impedance of 50 Ω ± 10%. Recommendations in this design guide are based on the following a 6-layer board stack-up:



Signal	Layer 1
Prepreg	Layer 2
Ground	Layer 3
Core	Layer 4
Signal	Layer 5
Prepreg	Layer 6
Power	Layer 7
Core	Layer 8
Ground	Layer 9
Prepreg	Layer 10
Signal	Layer 11
Total Thickness	62 mils.

Figure 2-1 6-layer PCB Stack-Up

Table 2-1 PCB Parameter

Description	Nominal Value	Tolerance	Comments
Board Impedance Z0	50Ω	± 10%	With nominal 4 mil trace width
Dielectric Thickness	4.3 mils	± 0.5 mils	1 x 2116 Pre-Preg
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	4.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Solder mask Er	4.0	± 0.5	@ 100 MHz
Solder mask Thickness	1.0 mils	± 0.5 mils	From top of trace

2.3 PCB Technology Considerations

The following recommendation aids in the design of a JZ4775 based platform. Simulations and reference platform are based on the following technology, and we recommend that designers adhere to these guidelines.

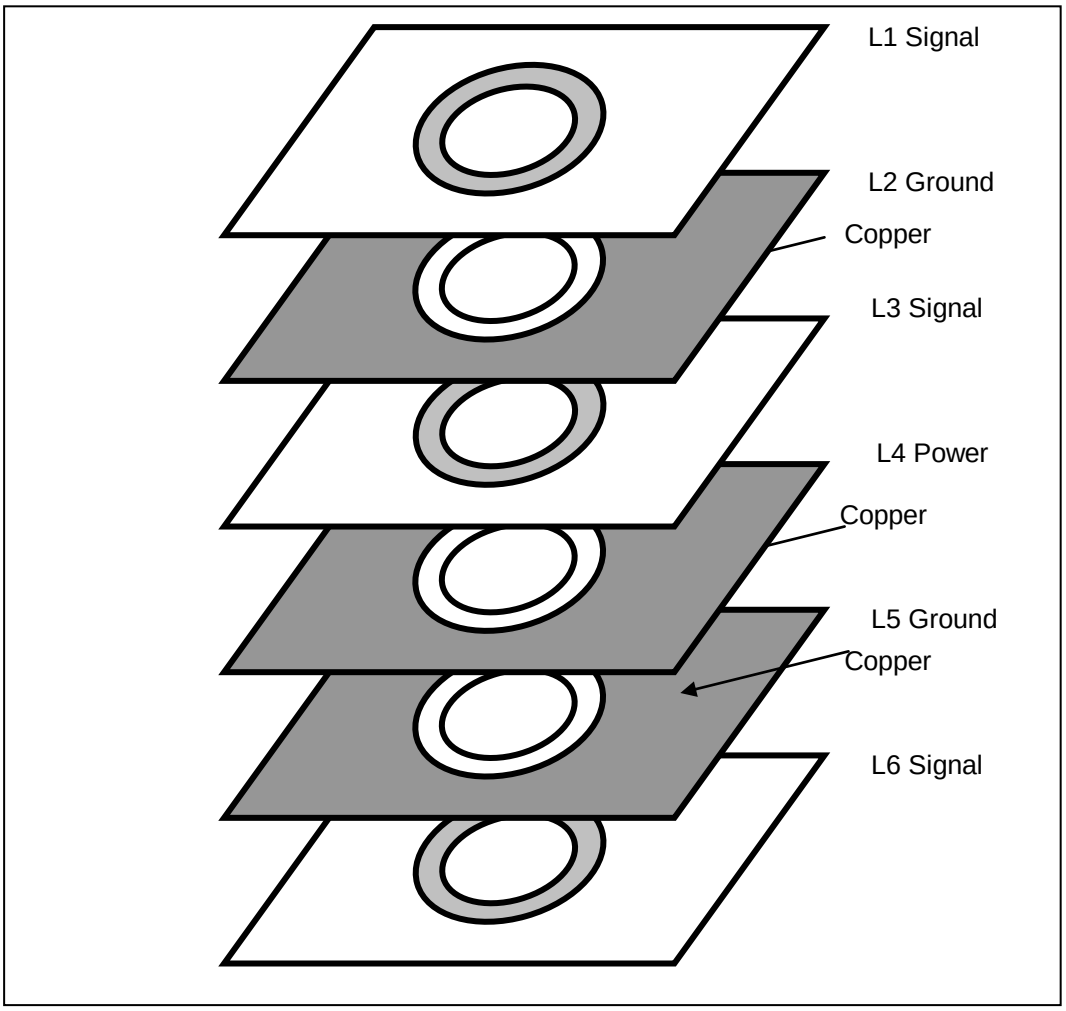


Figure 2-2 PCB Technologies – Stack-Up

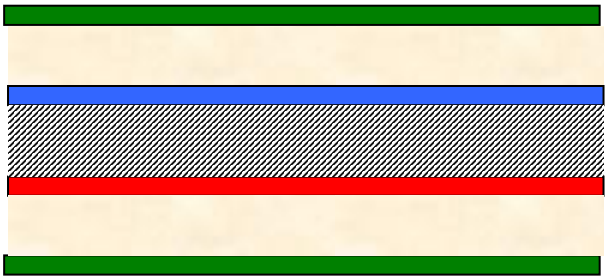
Table 2-2 PCB Parameter for Vias

Number of Layers	
Stack Up	6 Layer
Cu Thickness[1]	0.5 oz Outer (before plating); 1 oz inner
Final Board Thickness	62 mils (- 5mils / +8mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	16 mils
Via Anti-Pad	20 mils
Via Finished Hole	8 mils

1. The Cu Thickness is just a reference value. It is calculated by the PCB board producers for impedance matching.

2.4 4-Layer Board Stack-Up

The JZ4775 platform requires a board stack-up yielding a target board impedance of 50 Ω ± 10%. If a 4-layer board is used, the stack-up should be:



Signal	Layer 1
Prepreg	Layer 2
Ground	Layer 3
Core	Layer 4
Power	Layer 5
Prepreg	Layer 6
Signal	Layer 7
Total Thickness	40 mils.

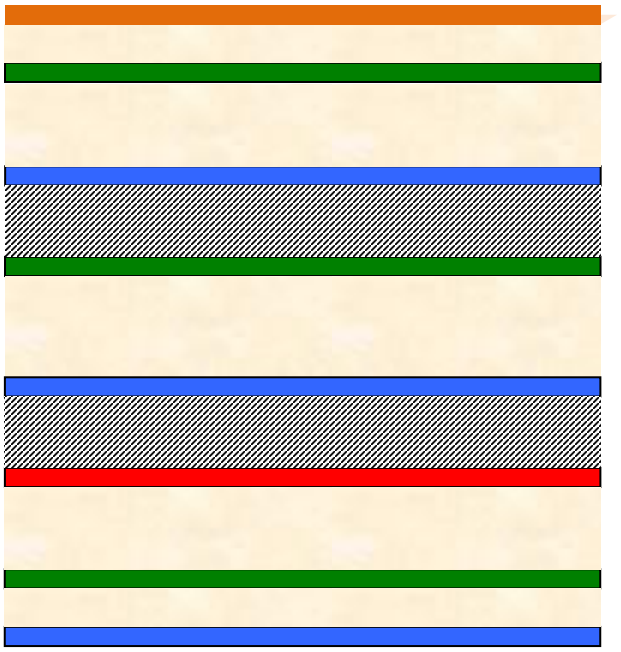
Figure 2-3 4-layer PCB Stack-Up

Table 2-3 PCB Parameters

Description	Nominal Value	Tolerance	Comments
Board Impedance Z0	50Ω	± 10%	With nominal 4 mil trace width
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	4.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Solder mask Er	4.0	± 0.5	@ 100 MHz
Solder mask Thickness	1.0 mils	± 0.5 mils	From top of trace

2.5 8-Layer HDI Board Stack-Up

The JZ4775 platform requires a board stack-up yielding a target board impedance of 50 Ω ± 10%. If a 8-layer HDI board is used, the stack-up should be:



Placement	Layer 1
Prepreg	Layer 2
Signal	Layer 3
Prepreg	Layer 4
Ground	Layer 5
Core	Layer 6
Signal	Layer 7
Prepreg	Layer 8
Ground	Layer 9
Core	Layer 10
Power	Layer 11
Prepreg	Layer 12
Signal	Layer 13
Prepreg	Layer 14
Ground	Layer 15
Total Thickness	40 mils.

Figure 2-4 8-layer PCB Stack-Up

Table 2-4 PCB Parameters

Description	Nominal Value	Tolerance	Comments
Board Impedance Z0	50Ω	± 10%	With nominal 4 mil trace width
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	4.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Solder mask Er	4.0	± 0.5	@ 100 MHz
Solder mask Thickness	1.0 mils	± 0.5 mils	From top of trace

3 Static Memory Interface Design Guidelines

3.1 Overview

The External NAND Memory Controller (NEMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of static memory and bus interfaces. It enables the connection of static memory such as conventional NAND flash memory (8bit and 16bit bus width), Toggle NAND flash memory (ONLY 8bit bus width), etc. to this processor or the external memory interface.

Static memory interface

- Support 3 external chip selection CS3~1#. Each bank can be configured separately
- The size and base address of static memory banks are programmable
- Direct interface to 8/16-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
- Wait insertion by WAIT pin
- Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

NAND flash interface

- Support on CS3~CS1, sharing with static memory bank3~bank1
- Support both of conventional NAND flash memory and Toggle NAND flash memory
- Support most types of NAND flashes, 8/ 16-bit data access, 512B/2KB/4KB/8KB/16KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2KB/4KB/8KB/16KB page size, 4 and 5 address cycles are supported
- Support read/erase/program NAND flash memory
- Support boot from NAND flash

3.2 Boot Memory

BOOT_SEL [2:0] pins define the boot time configurations as listed in the following table.

Table 3-1 Boot Configuration

BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	Boot From
1	1	1	USB boot (USB 2.0 device, EXTCLK=24MHz)
1	0	0	SD boot @ MSC1 (MMC/SD use GPIO Port E)
1	0	1	SD boot@ MSC0 (MMC/SD use GPIO Port A)
0	1	1	eMMC boot @ MSC0 (use GPIO Port A)
1	1	0	NAND boot @ CS1
0	0	0	SPI boot @ SPI0/CE0
0	0	1	USB boot (USB 2.0 device, EXTCLK=26MHz)
0	1	0	NOR boot @ CS4 (just for FPGA testing)

The boot procedure is showed in the following flow chart:

- In case of NAND/SDcard/iNAND/SPI boot, if it fails, enter MSC1 and USB boot.
- In case of USB boot, if it cannot connect to USB host within 10 seconds, restart the boot procedure.
- In case of NOR boot, if it fails, restart the boot procedure.
- If the boot procedure has been repeated more than 3 times, enter hibernating mode.

3.3 NAND Flash Connection

It supports on CS [3:1], sharing with static memory bank3~bank1.

The following Figure 3-1 is an example of 16-bit NAND Flash Interconnection; Figure3-2 is an example of 8-bit Toggle NAND Flash Interconnection.

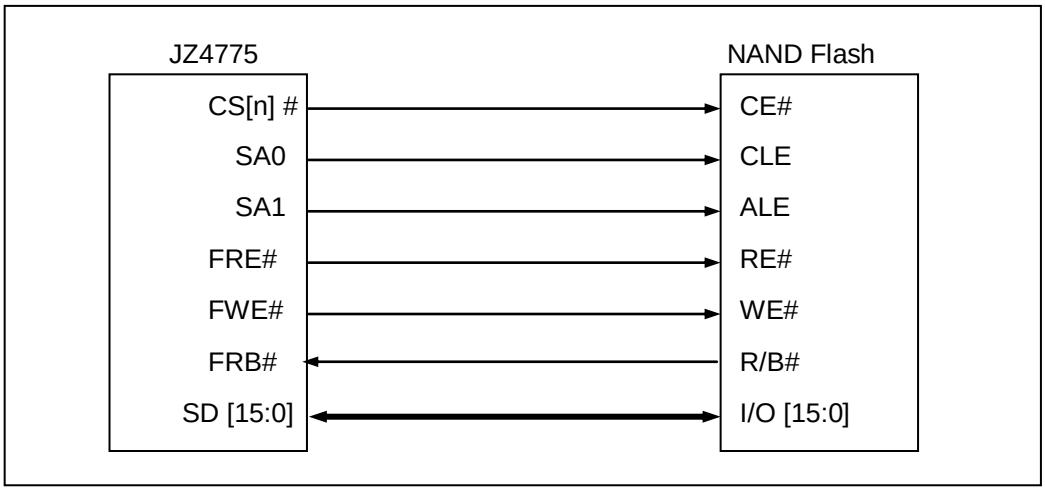


Figure 3-1 16-bit NAND Flash Interconnection Example

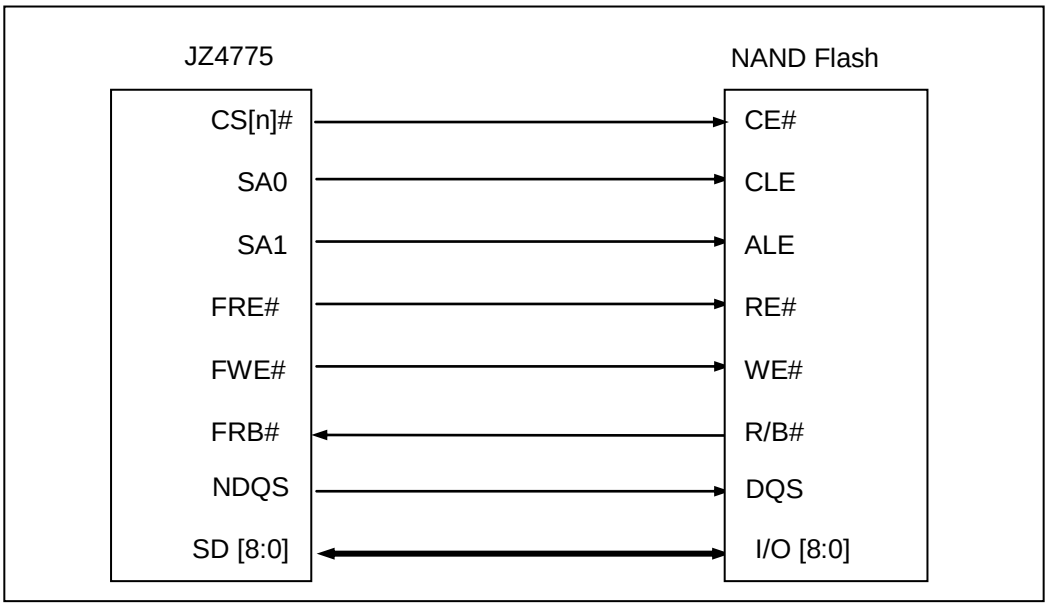


Figure 3-2 8-bit Toggle NAND Flash Interconnection Example

4 DDR3 SDRAM

4.1 Overview

DDRC (DDR Controller) is a general IP which provides an interface to DDR2, DDR3, mobile DDR (LPDDR) memory. The DDRC IP is designed for SOC usage and is configurable, scalable to meet the requirement of various SOC.

4.2 Connection to two 2 Gb x 16 DDR3 SDRAM device

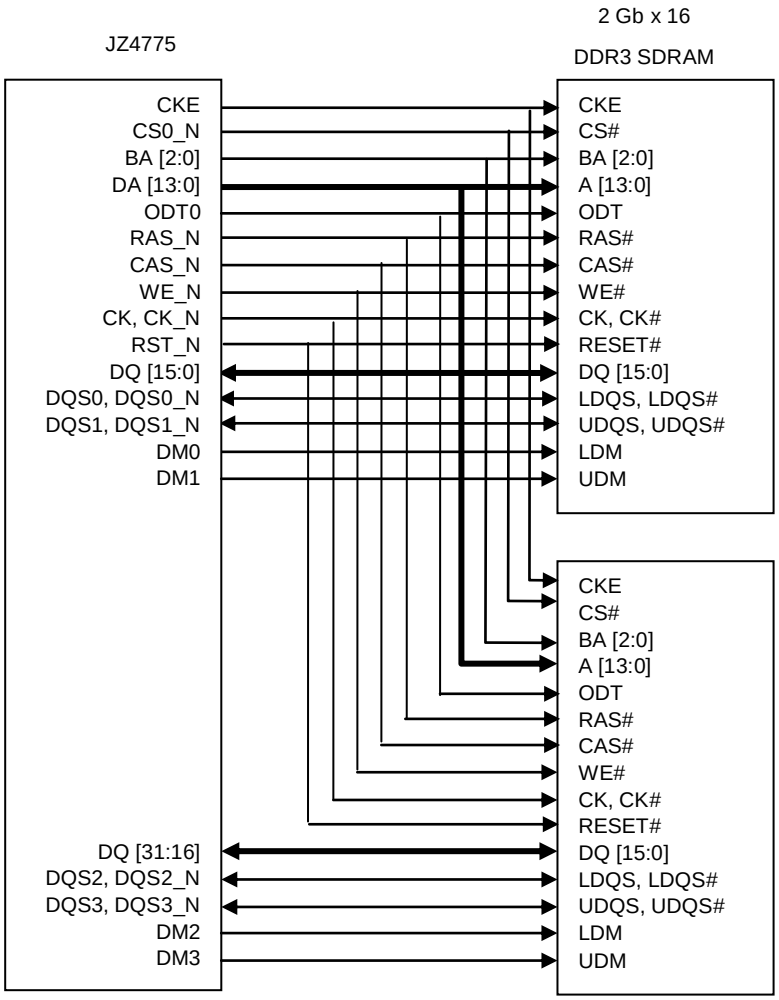


Figure 4-1 Two 16-bit DDR3 Interconnection Example

4.3 Connection to four 1 Gb x 8 DDR3 SDRAM device

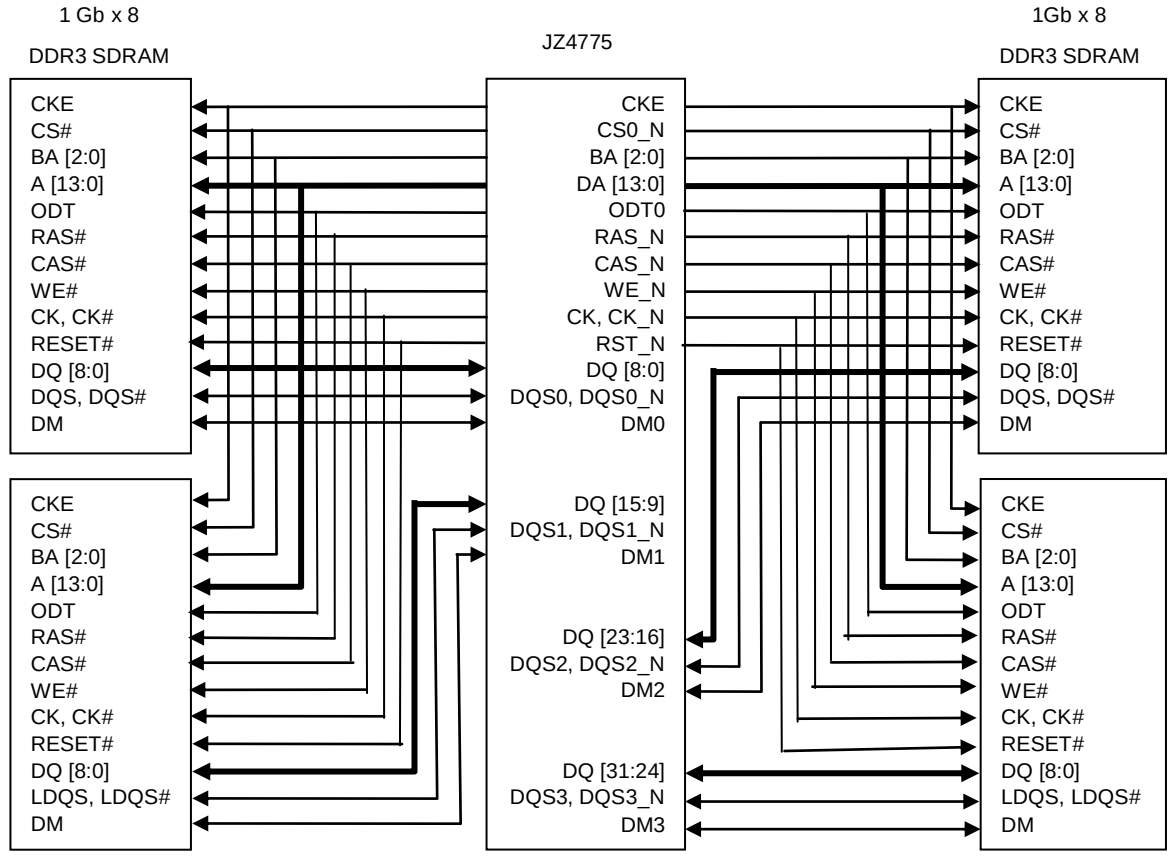


Figure 4-2 Four 8-bit DDR3 Interconnection Example

4.4 Layout Guideline

In the classical high-speed flow, to ensure the maximum performance of the DDR3, we should observe the following guidelines. The questions we should be noticed are: Flight time delay and skew, Signal integrity and impedance matching, Crosstalk, Power supply bypassing.

The basic recommendations are as follows:

- The minimum Stack-up required four layer stack. There must have a ground layer to separated two signal layers. Just as describes in Figure 2-3.
- Signals should be routed based on the relative tightness of the skew budgets. In order of priority:
  1) The double data rate signals, DQ, DM, and DQS/DQS# should be routed first since these have the strictest budgets, ¼ of a clock period available for set up or hold relative to the differential strobe.
  2) Differential clock, CK/CK# and single data rate signals, Address/Command/Control. These have looser budgets with ½ of a clock period for set up and hold.
  3) If read and write leveling techniques are not used, make sure that the rising edges of all differential DQS/DQS# signals are within ¼ of a clock period of the rising edge of the differential clock, CK/CK#.
  4) Route all Vref and support signals (JTAG etc. if implemented)

- The fundamental high-speed PCB issues are flight time delay and skew. Controlling the maximum placement of components. All of the shorter nets in a clock domain must be match the longest one. Therefore, flight time delay and skew are controlled by the matching of the trace.

  Assumptions are 151 ps. /inch for top layer microstrip (air in cross section) and 179 ps./inch for stripline or embedded microstrip (no air in cross section). The below table is the recommended budgets.

Table 4-1 The Recommended Budgets

Skew Control Recommendations for DDR Interfaces.				
	Bit Rate	@ 400 Mbps	@ 800 Mbps	@ 1600 Mbps
DQ to DQS Domain	Skew in ps.	50	25	10
	Skew in Inches of Microstrip	0.33	0.17	0.07
	Skew in Inches of Stripline	0.28	0.14	0.06
Addr/Cmd to CK/CK# Domain	Skew in ps.	100	50	25
	Skew in Inches of Microstrip	0.67	0.33	0.17
	Skew in Inches of Stripline	0.56	0.28	0.14
DQS to CK	Skew in ps.	375	188	94
	Skew in Inches of Microstrip	2.50	1.25	0.63
	Skew in Inches of Stripline	2.08	1.04	0.52

- Signal integrity refers to controlling overshoot, ring back, and transition edges. These issues are caused by the mismatch of impedance. Trace impedance is governed by the trace width as well as the thickness and dielectric constant of the PCB insulating materials (usually FR-4). So you should keep the impedance average in a trace, be sure the bending and via as little as possible.

  When the signal has a via in its trace, there must be a GND via beside the signal via.
- Crosstalk is fundamentally controlled by the PCB stack-up and minimum trace spacing. The best approach to avoiding a crosstalk problem is to ensure all the signals have high-quality signal return paths and to spread the signal out.
  - Each signal layer should have a nearby full ground plane to provide the shortest return current path. In order to maintain consistent characteristic impedance, it is important that the traces be routed over solid ground planes (Figure 4-3) not separate (Figure 4-4). A high speed signal trace should never be routed across a plane split. This will interrupt the return currents that flow beneath the conductor and can lead to crosstalk with neighboring traces. This will also increase emissions from the board.

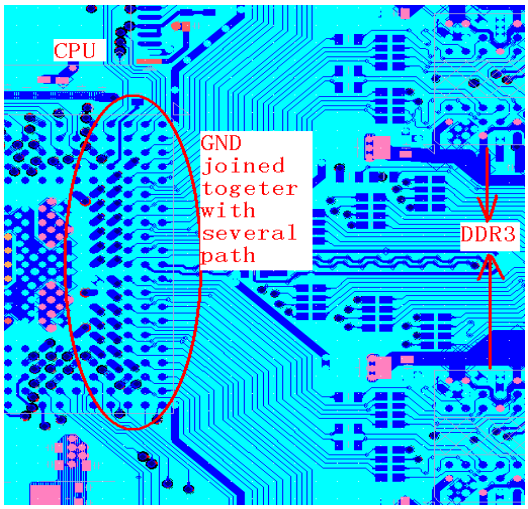


Figure 4-3 GND Joined Together

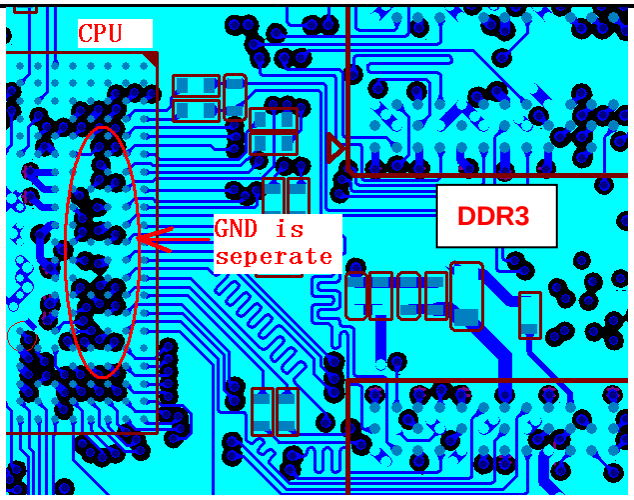


Figure 4-4 GND is separate

- Each bus (D0~D8, DQS0/DQS0_N and DQM0 compose one bus, and etc.) should not cross other buses. If routing is carried out on two layers, byte lanes should be alternated between layers in order to reduce congestion, and crosstalk at the DRAMs; e.g. Byte lanes 0 and 2 should be routed on one layer, and 1 and 3 on the other.
- The crosstalk and characteristic impedance of an array of traces are interrelated. In order to minimize crosstalk, the characteristic impedance of a trace should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces. To achieve this, the space between traces should be twice the height of the trace above the ground plane. Figure4-5 shows the recommended spacing ("H" means the height from reference plane.).

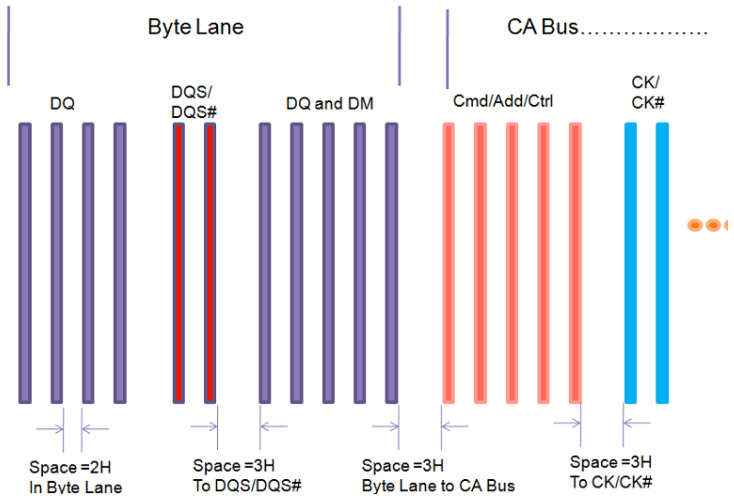


Figure 4-5 Spacing between Different Signal Groups

- Precise power supply bypassing is important for high-speed PCB. Control the power supply high-frequency impedance means controlling power supply inductance. Power supply high-frequency impedance is beaten down by many small capacitors connected between the power and ground plane. Using many capacitors, rather than a large one, will reduce the inductance. The inductance of a capacitor is dependent on its size. The capacitor

need to be placed very close to the device they are bypassing.

- VREF is used as a reference by the input buffers of the DDR3 memories. It is recommended to be 1/2 of the DDR3 power supply voltage and should be created using a resistive divider as shown in the schematic. Other methods are not recommended. Figure 4-5 shows the layout guidelines for VREF.

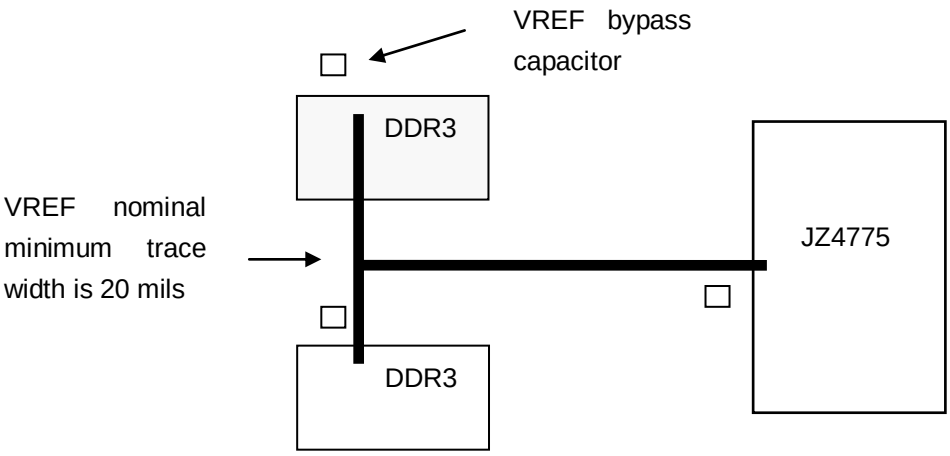


Figure 4-6 VREF Routing and Topology

- The region of the PCB used for DDR3 circuitry must be isolated from other signals. Region should be encompassing all DDR3 circuitry and varies signals depending on placement. Non-DDR3 signals should not be routed on the DDR3 signal layer within the DDR3 keep out region. No breaks should be allowed in the reference ground layers in the region. In addition, the +1.5V power plane should cover the entire keep out region.
- Bypassing capacitors should be close to the devices, or positioned for the shortest connections to pins, with wide traces to reduce impedance.

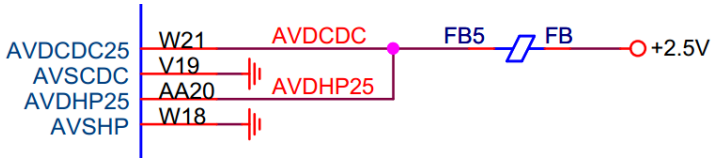
5 Audio Codec Design Guidelines

5.1 Overview

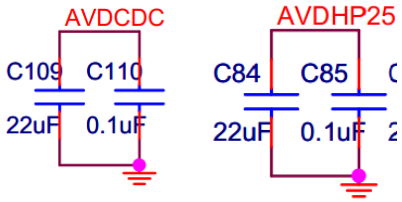
This chapter describes the embedded audio CODEC in the processor. This embedded CODEC is an I2S audio CODEC. AIC (AC'97 and I2S Controller) module is an interface to this CODEC for audio data replaying and recording.

5.2 Audio Power

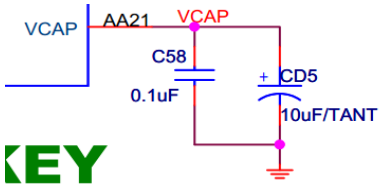
AVDCDC25 and AVDHP25should are connected to a cleaned +2.5V power.



For correct working, it is required to connect decoupling capacitors (22μF and 100nF ceramic) between the pins AVDCDC25, AVDHP25 and AVSCDC, AVSHP.



A 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor should be attached from VCAP to AVSCDC to eliminate the effects of high frequency noise.



5.3 Headphone Out

The capacitor-less circuit for headphone out is recommended，because this circuit is no POP noise which is caused by the coupled capacitor.

The AOHPL and AOHPR pins are applied directly to the loads. The ground of the headphone is connected to AOHPM. The DC value of the signal AOHPL\ AOHPR\ AOHPM equals to VREF/2.

The measurement ground reference corresponds to the physical interconnection of AOHPM and AOHPMS. AOHPM and AOHPMS have to be connected together as close as possible of the headphone connector. The measurement is done between AOHPL/R and the measurement ground reference.

The C52, C54, R56, R57 combine into two RC circuits to improve the headphone out performance.

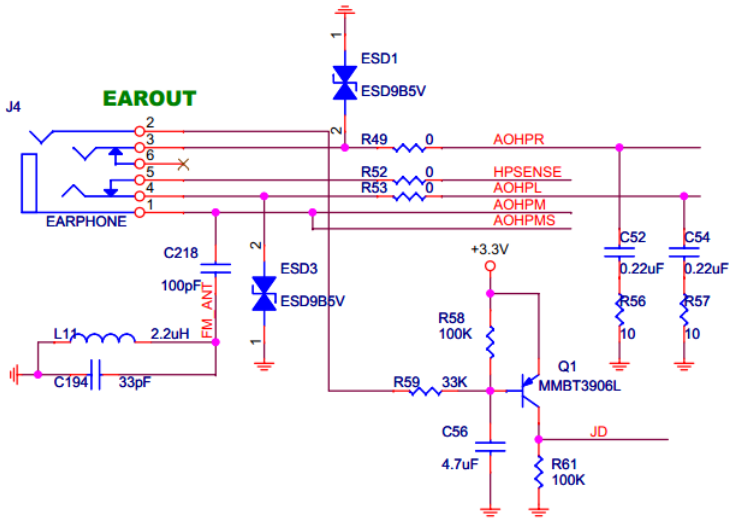
The ESD1 and ESD3 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic

discharge. The device provides protection for contact discharges to greater than +/-15KV.

JD is used to implement the insert test. When the jack is inserted, the value of JD will be high: Otherwise, JD will be low.

Through the detection circuit on HPSENSE implement the insert test of the jack. HPSENSE is default, and JD is reserved.

The FM_ANT pin is used as an antenna of FM module.



The AOHPMS and AOHPM must be connected at terminate, near the headphone Jack

5.4 Mic In

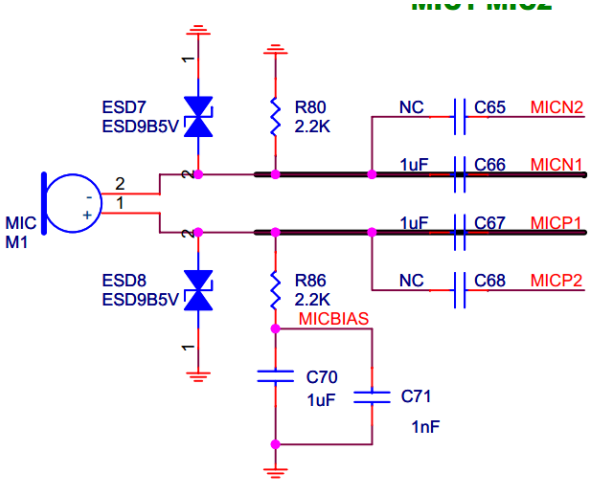
Specific value of resistor (R80, R86, commonly from 2.2k Ohm to 4.7k Ohm) and Vmicbias (if generated on board, usually from 1 to 2V or more) depends on the selected EC (Electret Condenser) microphone.

The 1nf decoupling capacitance used in MICBIAS pin removes high frequency noise of the chip.

Setting SB_MIC1/SB_MIC2 to 1 will close microphone input path for saving power, also setting SB_MICBIAS to 1 will close MICBIAS stage and the MICBIAS output voltage will be zero.

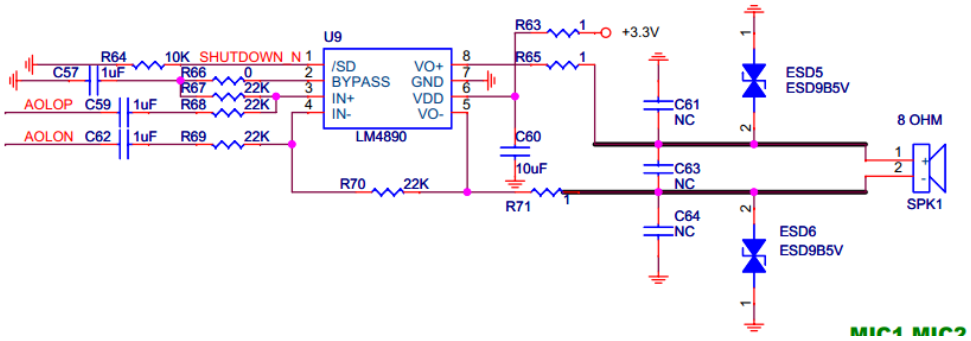
MICBIAS output voltage scales with AVDCDC, equals to 5/6*AVDCDC (typical 2.08V).

MICBIAS output current is 4mA max.



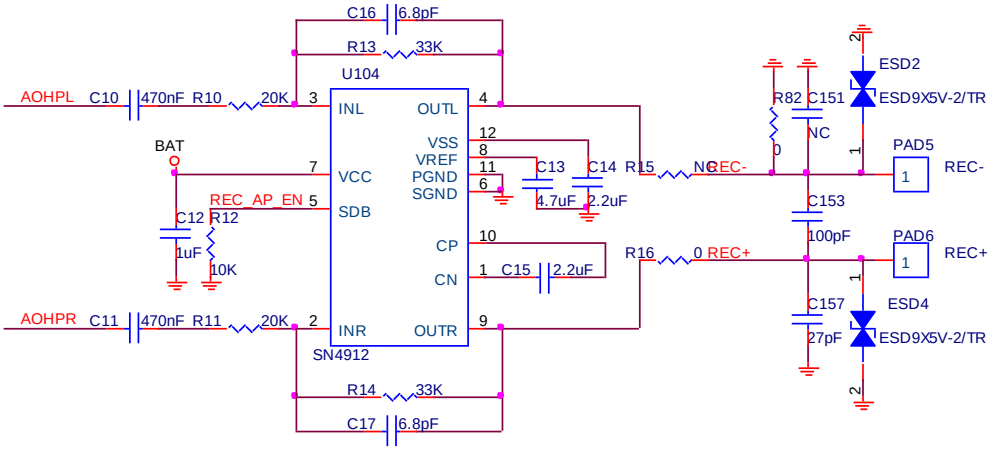
5.5 Speaker

The ESD5 and ESD6 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. The device provides protection for contact discharges to greater than +/-15KV.



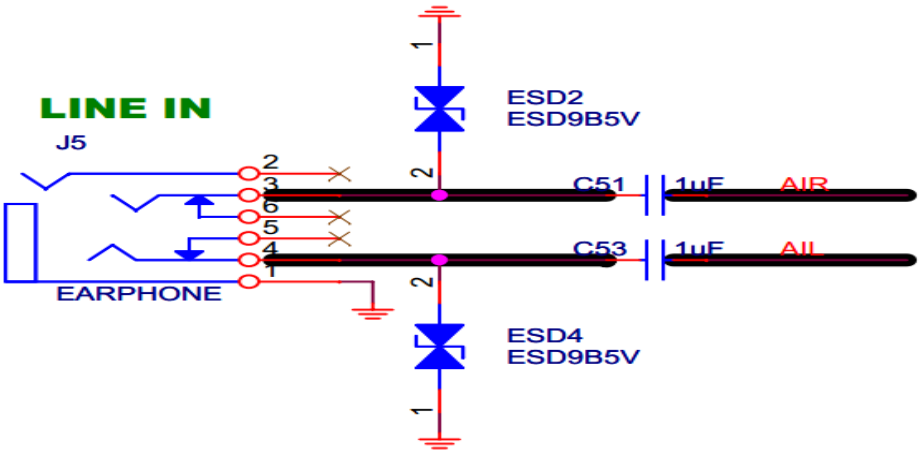
5.6 Receiver

The ESD2 and ESD4 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. The device provides protection for contact discharges to greater than +/-15KV.



5.7 Line In

The ESD2 and ESD4 is an ESD transient voltage suppression component which provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge. The device provides protection for contact discharges to greater than +/-15KV.



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5.8 Layout Guideline

To ensure the maximum performance of the Audio, proper component placement and routing techniques are required. These techniques include properly isolating associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must not cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.

- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance. It is especially for VCAP.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

6 USB and OTG Design Guidelines

6.1 USB Overview

JZ4775 integrates USB Host Controller (UHC) which is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.

Familiarity with the Universal Serial Bus Specification, Revision 1.1 and the OHCI specification are necessary to fully understand the material.

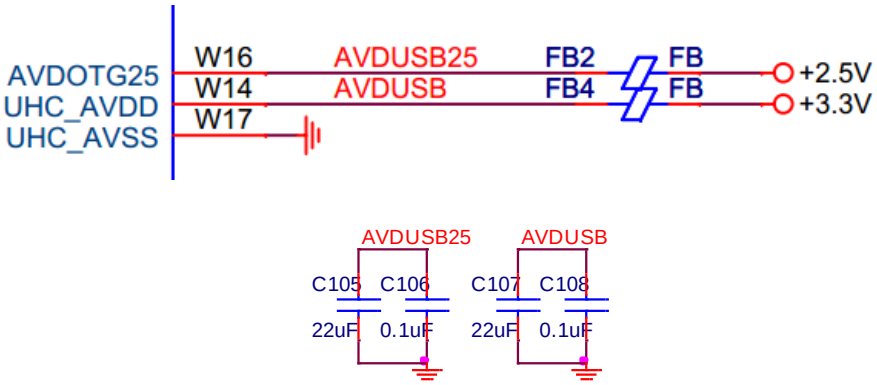
It supports both low-speed and high-speed USB devices.

6.1.1 USB Power

For a correct working, it is required to connect decoupling capacitor (22µF and 100nF ceramic) between the pins AVDOTG25, UHC_AVDD and UHC_AVSS.

AVDOTG25 should be connected to a cleaned +2.5V power.

UHC_AVDD should be connected to a cleaned +3.3V power.



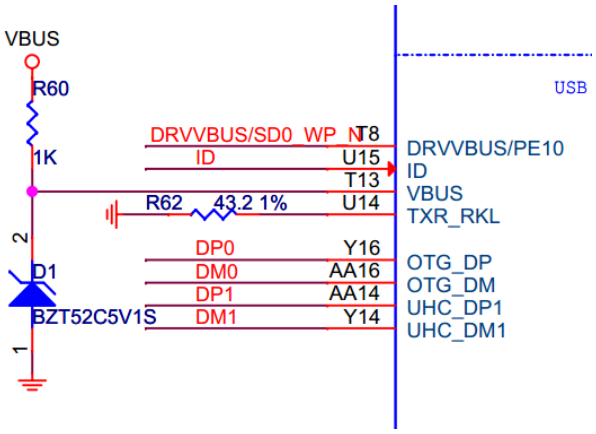
6.2 OTG Overview

The Universal Serial Bus (USB) supports serial data exchanges between a host computer and a variety of simultaneously accessible portable peripherals. Many of these portable devices would benefit a lot from being able to communicate to each other over the USB interface. And OTG make this possible. An OTG device can plays the role of both host and device.

JZ4775 also integrates USB 2.0 OTG interface, which compliant with USB protocol Revision 2.0 OTG. It supports low-speed (1.5 Mbps), full-speed (12 Mbps) and high speed (480 Mbps). Operates either as the function controller of a high-/full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions.

6.2.1 OTG Power

We should have a pin of VBUS supply power OTG, it have to connect to an external charge. The DRVVBUS is used to control whether to supply power for OTG.



To enable the OTG, the circuit should monitor the VBUS pin and can supply voltage for this pin and ID pin need connect CPU's ID pin and one GPIO pin for insert detection. The range of VBUS is 4.75V ~ 5.25V, so it need be protected by a zener diode D1.Figure 6-1 shows the classic design for OTG function.

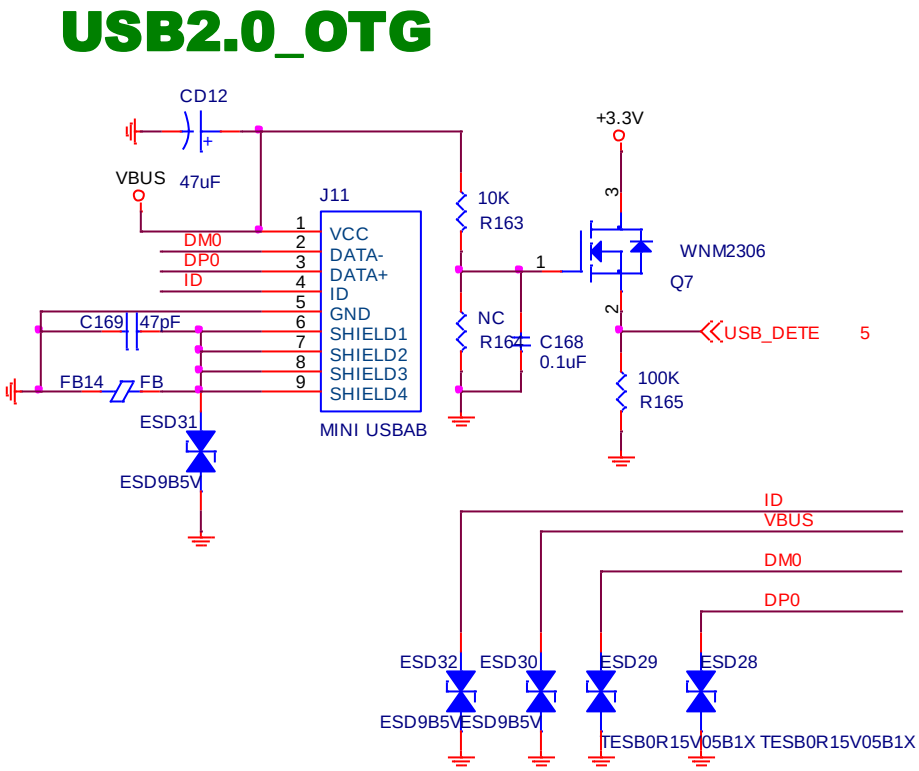


Figure 6-1 Classic Design for USB 2.0 OTG

To achieve this function, DRVBUS control 5V boost circuit whether supply voltage for VBUS or not. DRVVBUS controlled by the processor. Via the state of USB_DETE and ID pins, the processor can complete this task.

6.3 Guidelines for the USB and OTG interface

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both DP1/DM1 data lines.

- 15 Ω series resistors should be placed as close as possible to the JZ4775. These series resistors provide source termination of the reflected signal.
- 47-pF caps must be placed as close as possible to the JZ4775 as well as on the processor side of the series resistors on the USB data lines (DP1, DM1). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (DP1, DM1). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the DP and DM signals should be 45 Ω (to ground) for each USB signal DP or DM. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 6-2 6-3. The impedance is 90 Ω between the differential signal pairs DP and DM, to match the 90 Ω USB twisted-pair cable impedance . Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals'. (i.e., hand-routing preferred). The DP/DM signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the DP/DM signal pair to adjacent signal traces will help to prevent cross-talk. The DP/DM signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

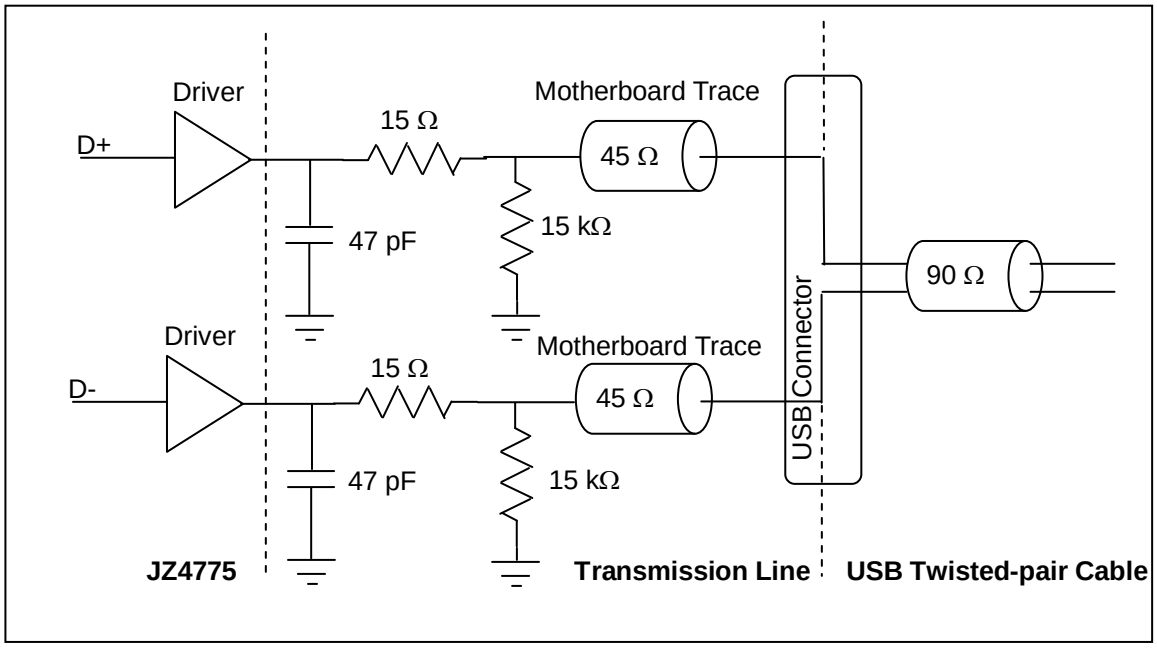


Figure 6-2 Recommend USB Host Schematic

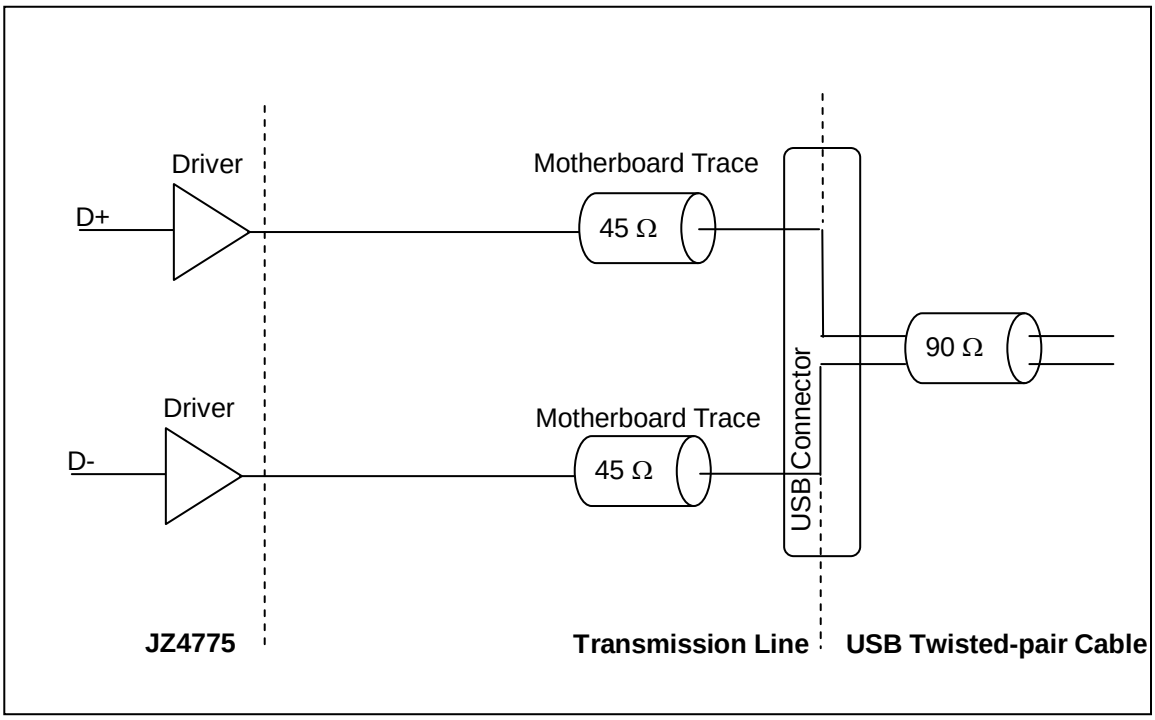


Figure 6-3 Recommend USB OTG Schematic

7 LCD

The JZ4775 integrated LCD controller has the capabilities to driving the latest TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller. And OSD is also supported for LCD controller

Table 7-1 TFT and CCIR Pin Mapping

Pin	Generic 8-bit Serial TFT	Generic 18/16-bit Parallel TFT		Special TFT 1 18/16-bit Parallel		Special TFT 2 18/16-bit Parallel		Special TFT 3 18/16-bit Parallel		CCIR656 8-bit	CCIR601 16-bit
Lcd_pclk/ Slcd_clk	CLK	CLK		DCLK		CLK		HCLK		CLK	CLK
Lcd_vsync/ Slcd_cs	VSYNC	VSYNC		SPS		GSRT		STV		VSYNC	VSYNC
Lcd_hsync/ Slcd_rs	HSYNC	HSYNC		LP		GPCK		STH		HSYNC	HSYNC
Lcd_de	DE	DE		-		-		-		-	-
Lcd_ps	-	-		Pulse		Toggle		Toggle		-	-
Lcd_cls	-	-		Pulse		Pulse		Pulse		-	-
Lcd_rev	-	-		Toggle		Toggle		Toggle		-	-
Lcd_spl	-	-		Pulse		Pulse		Toggle		-	-
Lcd_dat17	-	R5	-	R5	-	R5	-	R5	-	-	-
Lcd_dat16	-	R4	-	R4	-	R4	-	R4	-	-	-
Lcd_dat15	-	R3	R5	R3	R5	R3	R5	R3	R5	-	D15
Lcd_dat14	-	R2	R4	R2	R4	R2	R4	R2	R4	-	D14
Lcd_dat13	-	R1	R3	R1	R3	R1	R3	R1	R3	-	D13
Lcd_dat12	-	R0	R2	R0	R2	R0	R2	R0	R2	-	D12
Lcd_dat11	-	G5	R1	G5	R1	G5	R1	G5	R1	-	D11
Lcd_dat10	-	G4	G5	G4	G5	G4	G5	G4	G5	-	D10
Lcd_dat9	-	G3	G4	G3	G4	G3	G4	G3	G4	-	D9
Lcd_dat8	-	G2	G3	G2	G3	G2	G3	G2	G3	-	D8
Lcd_dat7	R7/G7/B7	G1	G2	G1	G2	G1	G2	G1	G2	D7	D7
Lcd_dat6	R6/G6/B6	G0	G1	G0	G1	G0	G1	G0	G1	D6	D6
Lcd_dat5	R5/G5/B5	B5	G0	B5	G0	B5	G0	B5	G0	D5	D5
Lcd_dat4	R4/G4/B4	B4	B5	B4	B5	B4	B5	B4	B5	D4	D4
Lcd_dat3	R3/G3/B3	B3	B4	B3	B4	B3	B4	B3	B4	D3	D3
Lcd_dat2	R2/G2/B2	B2	B3	B2	B3	B2	B3	B2	B3	D2	D2
Lcd_dat1	R1/G1/B1	B1	B2	B1	B2	B1	B2	B1	B2	D1	D1
Lcd_dat0	R0/G0/B0	B0	B1	B0	B1	B0	B1	B0	B1	D0	D0

Table 7-2 TFT 24 bit parallel mode/16 bit parallel mode2

Pin	16 bit Parallel mode2	24 bit Parallel
Lcd_pclk/ Slcd_clk	CLK	CLK
Lcd_vsync/Slcd_cs	VSYNC	VSYNC
Lcd_hsync/Slcd_rs	HSYNC	HSYNC
Lcd_de	DE	DE
Lcd_ps	-	-
Lcd_cls	-	-
Lcd_rev	-	-
Lcd_spl	-	-
Lcd_dat17	R7	R7
Lcd_dat16	R6	R6
Lcd_dat15	R5	R5
Lcd_dat14	R4	R4
Lcd_dat13	R3	R3
Lcd_dat12	G7	R2
Lcd_dat11	G6	G7
Lcd_dat10	G5	G6
Lcd_dat9	0 (NC for panel)	G5
Lcd_dat8	G4	G4
Lcd_dat7	G3	G3
Lcd_dat6	G2	G2
Lcd_dat5	B7	B7
Lcd_dat4	B6	B6
Lcd_dat3	B5	B5
Lcd_dat2	B4	B4
Lcd_dat1	B3	B3
Lcd_dat0	0 (NC for panel)	B2
Lcd_lo6_o[5]	0	R1
Lcd_lo6_o[4]	0	R0
Lcd_lo6_o[3]	0	G1
Lcd_lo6_o[2]	0	G0
Lcd_lo6_o[1]	0	B1
Lcd_lo6_o[0]	0	B0

Table 7-3 Data mapping to GPIO function

pin name in LCD	mapping to GPIO function
Lcd_dat17/Slcd_dat17	lcd_r7
Lcd_dat16/Slcd_dat16	lcd_r6
Lcd_dat15/Slcd_dat15	lcd_r5
Lcd_dat14/Slcd_dat14	lcd_r4
Lcd_dat13/Slcd_dat13	lcd_r3
Lcd_dat12/Slcd_dat12	lcd_r2
Lcd_dat11/Slcd_dat11	lcd_g7
Lcd_dat10/Slcd_dat10	lcd_g6
Lcd_dat9/Slcd_dat9	lcd_g5
Lcd_dat8/Slcd_dat8	lcd_g4
Lcd_dat7/Slcd_dat7	lcd_g3
Lcd_dat6/Slcd_dat6	lcd_g2
Lcd_dat5/Slcd_dat5	lcd_b7
Lcd_dat4/Slcd_dat4	lcd_b6
Lcd_dat3/Slcd_dat3	lcd_b5
Lcd_dat2/Slcd_dat2	lcd_b4
Lcd_dat1/Slcd_dat1	lcd_b3
Lcd_dat0/Slcd_dat0	lcd_b2
Lcd_lo6_o[5]	lcd_r1
Lcd_lo6_o[4]	lcd_r0
Lcd_lo6_o[3]	lcd_g1
Lcd_lo6_o[2]	lcd_g0
Lcd_lo6_o[1]	lcd_b1
Lcd_lo6_o[0]	lcd_b0

8 EPD

8.1 Overview

The JZ4775 integrated EPD controller. The controller provides a low cost SOC solution for EPD applications.

Features:

- Supports PVI and AUO compatible EPD panels
- Supports different size up to 4096x4096@20Hz
- Supports 2/3/4 bits grayscale and color display
- Pixel base updating
- Supports hand-writing mode
- Supports SW LUT algorithm
- Supports AUTO-DU, AUTO-GC4 mode

The following figures show the connection example:

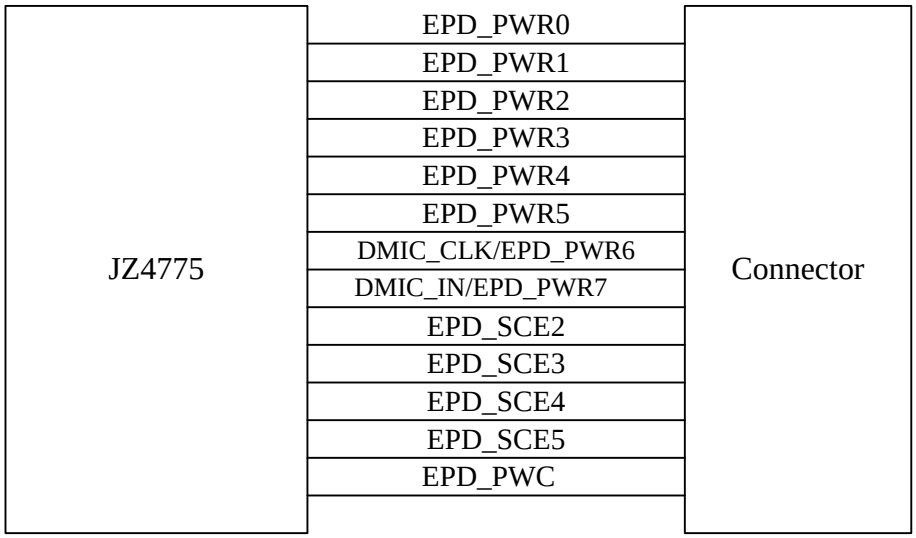


Table 8-1 Example of EPD Interconnection

9 Camera

9.1 Overview

The CIM (Camera Interface Module) of JZ4775 connects to a CMOS or CCD type image sensor. The CIM source the digital image stream through a common 8-bit parallel common digital protocol. The CIM can directly connect to external CMOS image sensors and ITU656 standard video decoders.

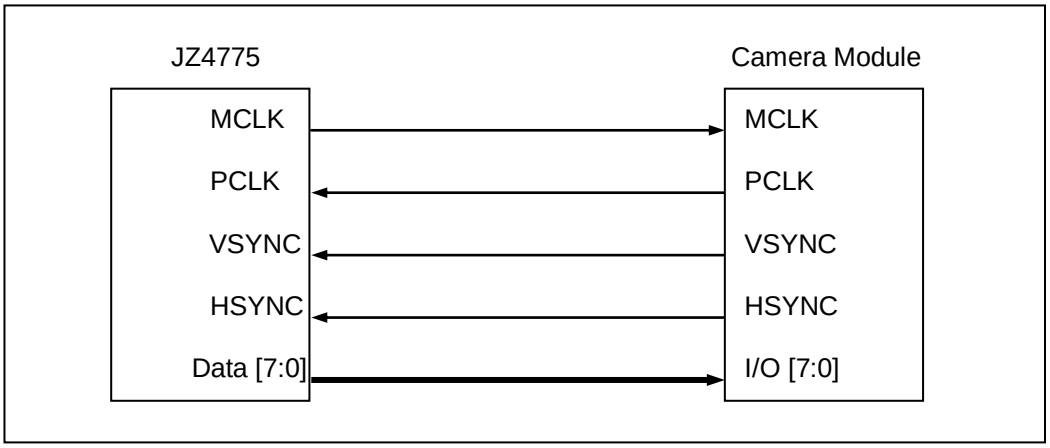


Figure9-1 Example of Camera Module Interconnection

10 SAR A/D Controller

10.1 Overview

The A/D is CMOS low-power dissipation 12bit touch screen SAR analog to digital converter. It operates with 3.3/1.2V power supply. It is developed as an embedded high resolution ADC targeting to the 65nm CMOS process and has wide application in portable electronic devices, high-end home entertainment center, communication systems and so on.

The SAR A/D controller is dedicated to control A/D to work at three different modes: Touch Screen (measure pen position and pen down pressure), Battery (check the battery power), and two auxiliary input. Touch Screen can transfer the data to memory through the DMA or CPU. Battery and two auxiliary inputs can transfer the data to memory through CPU.

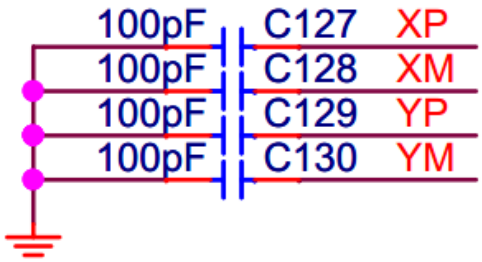
Table 10-1 SAR ADC Pins Description

NAME	I/O	Description
XM	AI	Touch screen analog differential X- position input
YM	AI	Touch screen analog differential Y- position input
XP	AI	Touch screen analog differential X+ position input
YP	AI	Touch screen analog differential Y+ position input
VBAT	AI	VBAT direct input
AUX1	AI	Auxiliary Input
AUX2	AI	Auxiliary Input

10.2 Touch Screen

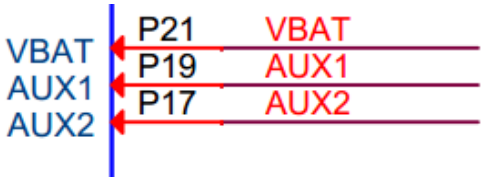
The JZ4775 can support 5-wire resistive touch screen.

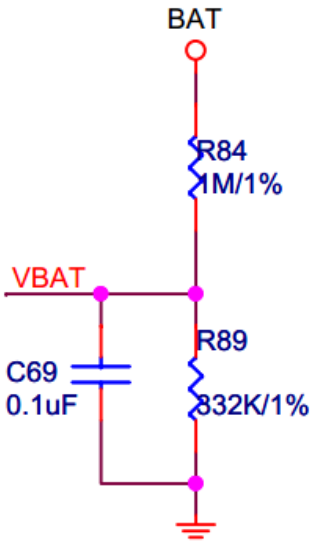
There is needed a decouple capacitor for every channel to avoid the crosstalk from LCD. The value is decided by the touch screen and can be from 100pF to 1000pF.



10.3 Battery Voltage Measurement

Users who already deployed divider resistors on board level can use VBAT to direct measure the battery value. The following figure is the approach we recommend. Use the recommended resistance; you can control the power consumption easier.



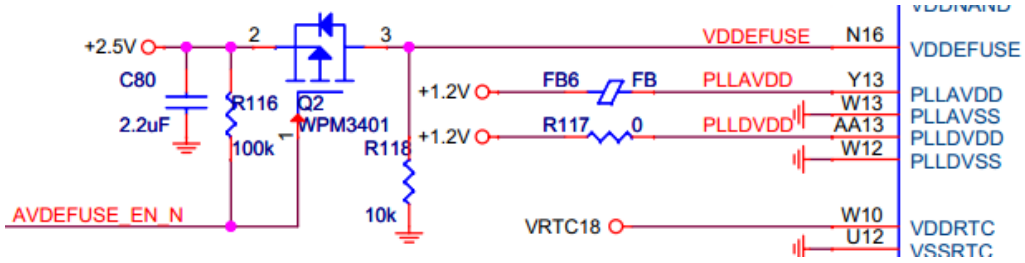


11 OTP EFUSE

11.1 Overview

Total 256 bits of EFUSE are provided, separated into lower 128bits segment and higher 28bits segment. Each segment can be programmed separately or together. Each segment has a protect bit, which has higher priority than program segment selection. Programming frequency should be within 133 MHz and 166Mhz. Programming time is around 3ms for either program in 128bits or 256bits.

Important: In program mode, supply AVDEFUSE with 2.5V. AVDEFUSE pin should be kept 0V except during programming. Maximum accumulative time for AVDEFUSE pin exposed under 2.5V+/-10% should be less than 1 sec. In read mode, leave AVDEFUSE to 0V.



12 Ethernet Design Guidelines

12.1 Overview

As the JZ4775 processor supports 10, 100 or 1000Mbps configuration 、MII、RMII、GMII and RGMII PHY interfaces.

12.2 JZ4775 Ethernet Controller Connection

JZ4775 connection example is shown as figure 11-1.

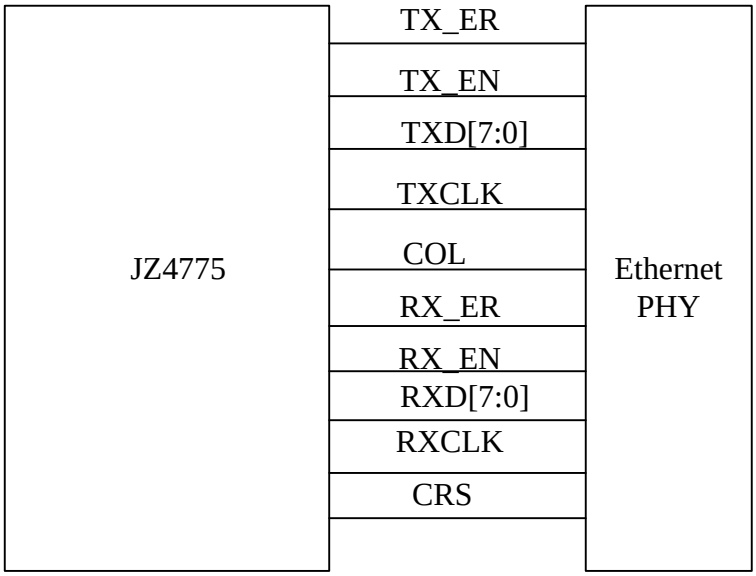


Figure 12-1 Connection

13 RTC

13.1 Overview

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, a power-on-reset generator, the real time and alarm logic, and the power down and wakeup control logic.

The external WAKEUP_N pin is with up to 2s glitch filter / alarm wakeup.

13.2 RTC Clock

The following figure is a typical design.

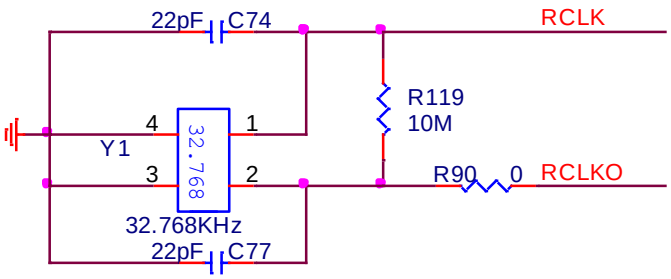


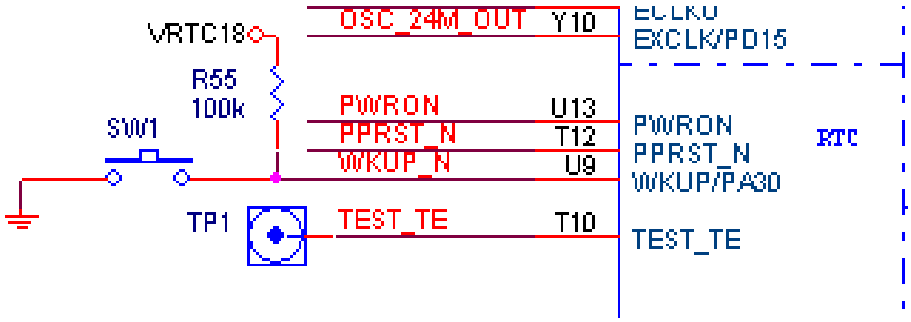
Table 13-1 RTC Clock Routing Summary

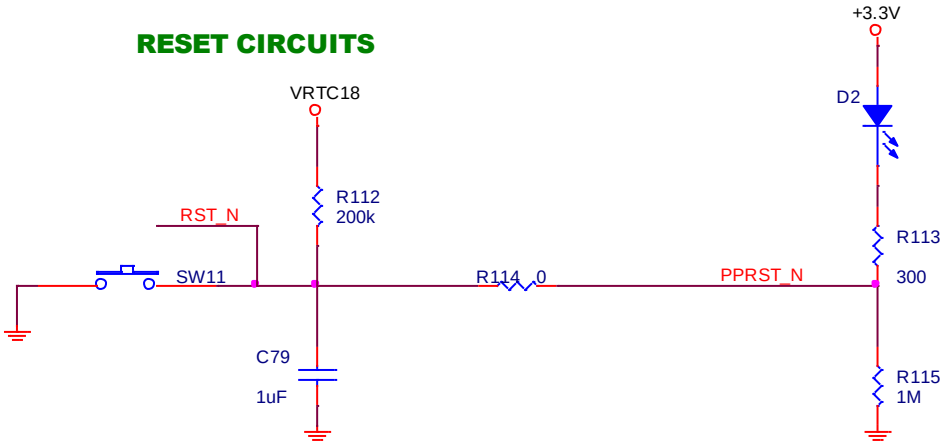
Trace Impedance	Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R90, C77, and C74 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R119 = 10M ± 5% C74=C77=22pF±10 % The value of C74, C77 and R90 should be referred to the crystal's specification	Ground

13.3 Power Control

The following is the recommended circuit for the system power control.

PWRON is an active high signal from CPU. If the power circuit enable signal is active high signal, you can use the PWRON directly. The resistance of R115 in the next figure is recommended to be 1M ohm; in this case, you can consume less current when power down mode.





14 Miscellaneous Peripheral Design Guidelines

14.1 SSI Design Guideline

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codec, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.
The following figures show the connection example:

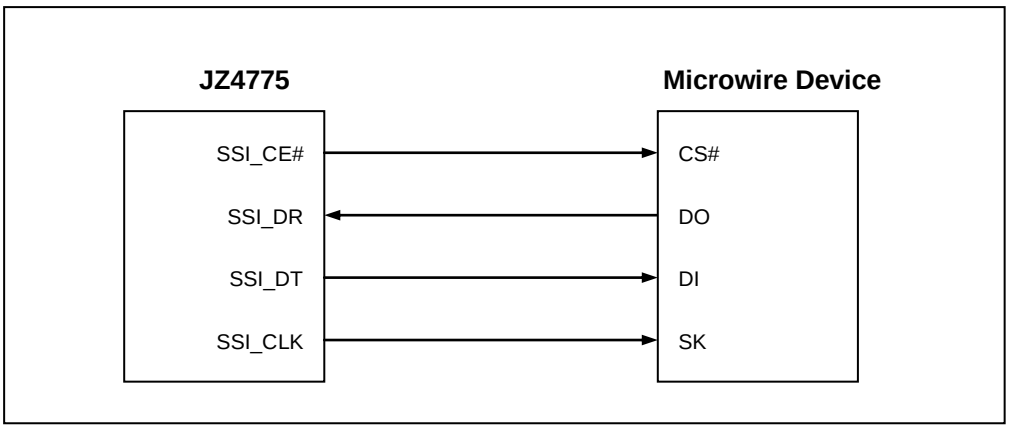


Figure 14-1 Microwire Interconnection

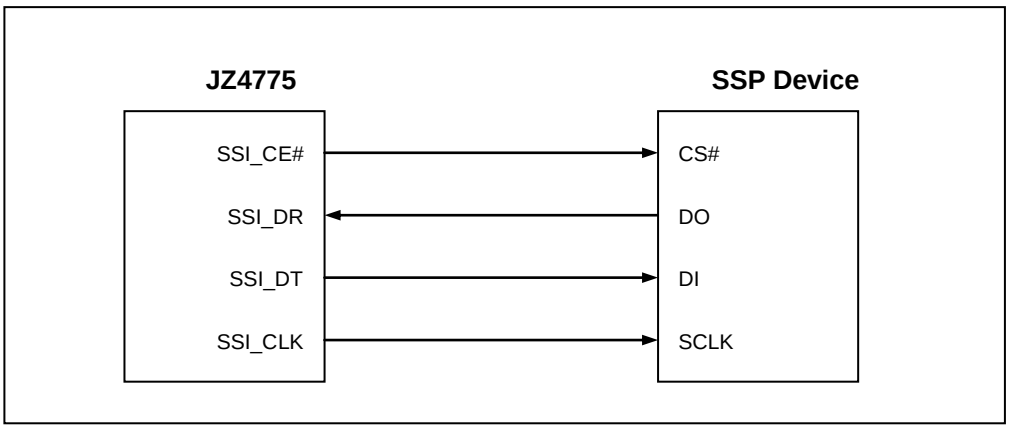


Figure 14-2 SSP Interconnection

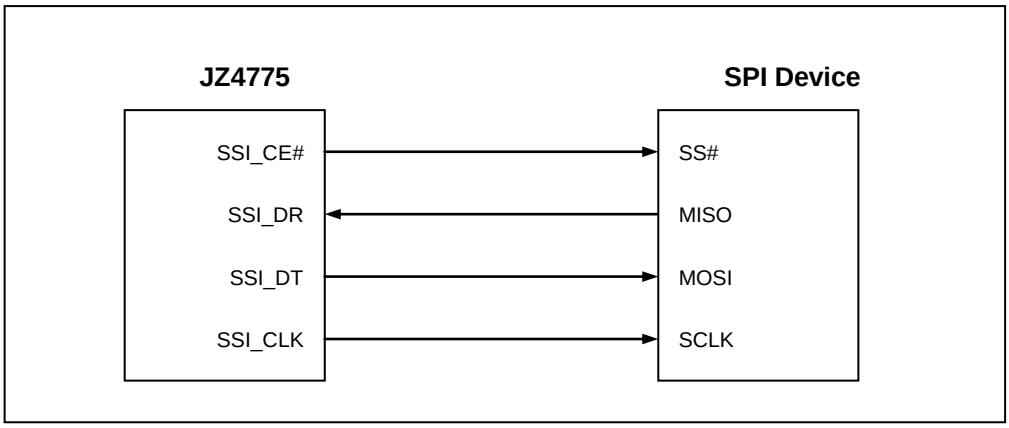


Figure 14-3 SPI Interconnection

14.2 UART

The JZ4775 processor has four UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550 industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.0

14.2.1 UART Implementation

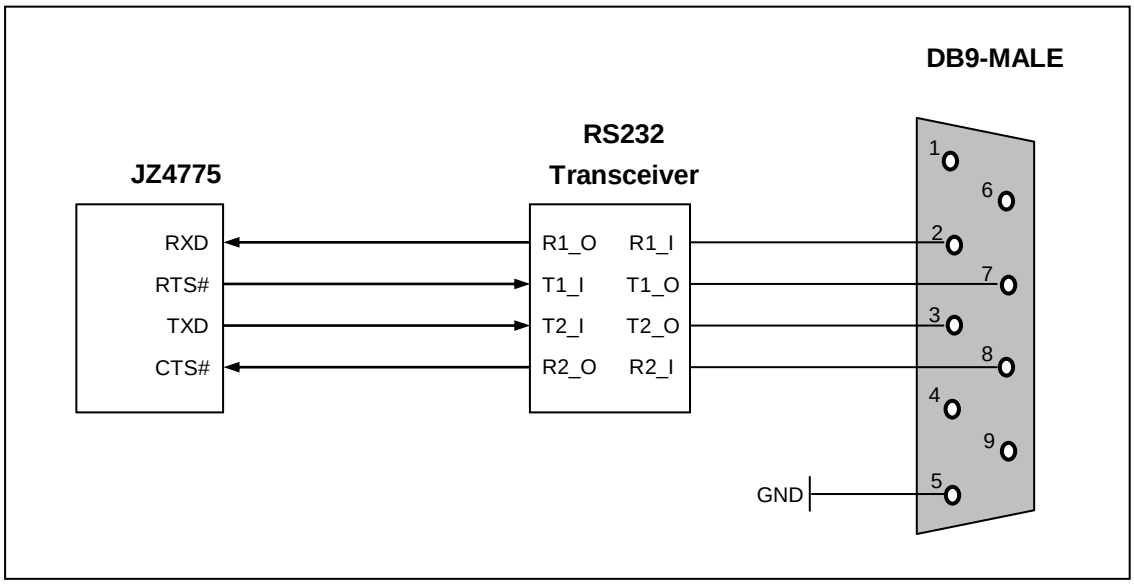


Figure 14-4 RS232 Serial Port Interconnection

14.3 SMB BUS

The SMB bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the SMB bus. The SMB bus requires a minimum amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

The SMB module supports SMB standard-mode and fast-mode up to 400 kHz. The interface example is shown as following figure. The SMB bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up (R1, R2=2.2K) is required on SCL and SDA. Refer to The SMB-Bus Specification for complete details on SMB bus operation.

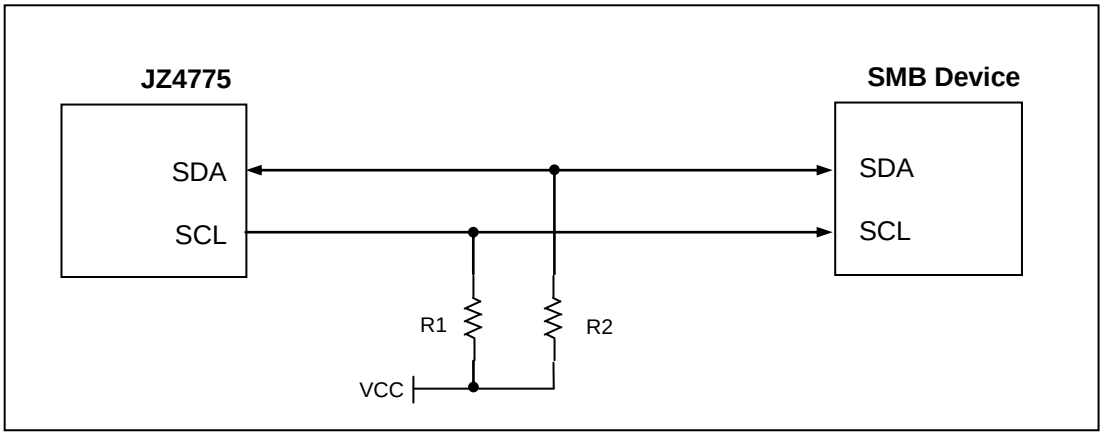


Figure 14-5 SMB Interconnection

14.4 PWM

The Pulse Width Modulator (PWM) is used to control the back light inverter or adjust bright or contrast of LCD panel and also can be used to generate tone. PWM consists of a simple free-running counter with two compared registers; each compare register performs a particular task when it matches the count value. The period comparator causes the output pin to be set and the free-running counter to reset when it matches the period value. The width comparator causes the output pin to reset when the counter value matches. JZ4775 contains eight pulse width modulators: PWM0 ~ PWM3.

14.5 GPIO

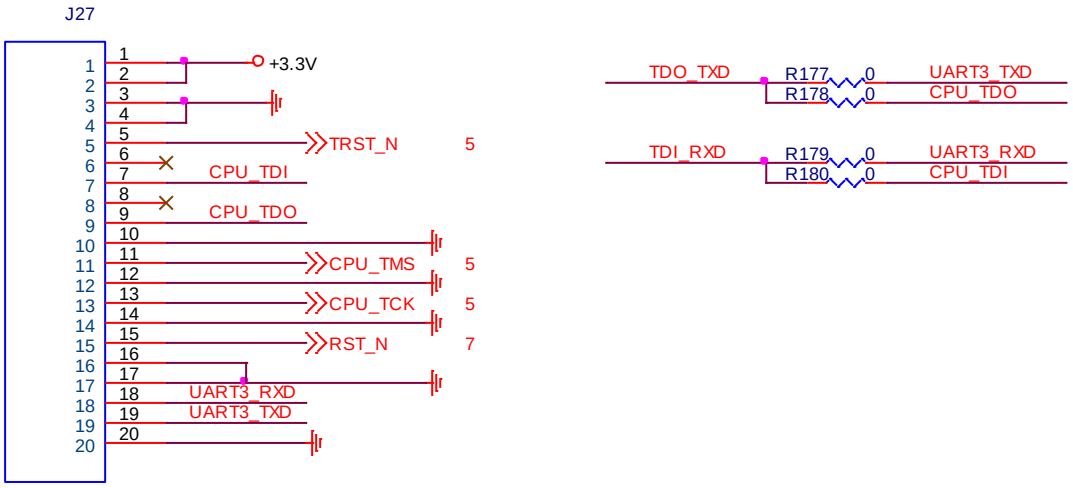
The JZ4775 processor provides 129 multiplexed General Purpose I/O Ports (GPIO) for use in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

14.6 JTAG/Debug Port

JZ4775 has a built-in JTAG/Debug port. All JTAG pins are directly connected. The following figure shows the connection of the JTAG port. Pin 15 RST_N should be connected to system reset circuit.

The header should be a 7X2 (2.54mm Pitch) male header with coat.

JDI & Uart Con



15 Platform Clock Guidelines

The JZ4775 processor contains two PLL driven by the 24-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- DDR bus clock
- Programmable clocks needed by certain peripherals

The Chip has two Phase Locked Loops (PLL) :

1. APLL mainly is used to CPU and L2CACHE, also may use the AHB0 and AHB2, other peripherals
2. MPLL mainly is used to DDR, also uses AHB0 and AHB2 APB, other peripherals

The following is the recommended circuit for main clock. When layout the board, you should keep the distance between Y2 and JZ4775 as short as possible.

The 24MHz crystal should be +/-20ppm

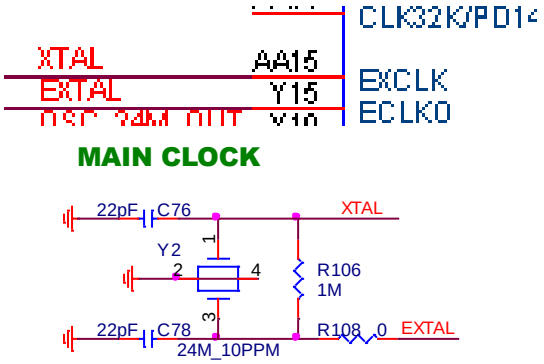


Table 15-1 Main Clock Routing Summary

Trace Impedance	Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R108, C76, and C78 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R106 = 1M ± 5% C76=C78=22pF±10% (Typical) The value of C76, C78 and R106 should be referred to the crystal's specification	Ground

16 Platform Power Guidelines

16.1 Overview

The JZ4775 processor needs four voltages: +3.3V, +1.5V for memory, +1.2V for core, +2.5V for USB OTG and HDMI. The following figure is a typical power circuit in the tablet and smart phone application.

The +1.2V need a power chip which can supply at least 1A, 1.2A is recommended.

The +1.5V current request is based on the external memory type and quantity.

And the +3.3V current request is based on the external device.

Normally, we use an 1.2A power chip for +1.5V and a 950mA power chip for +3.3V.

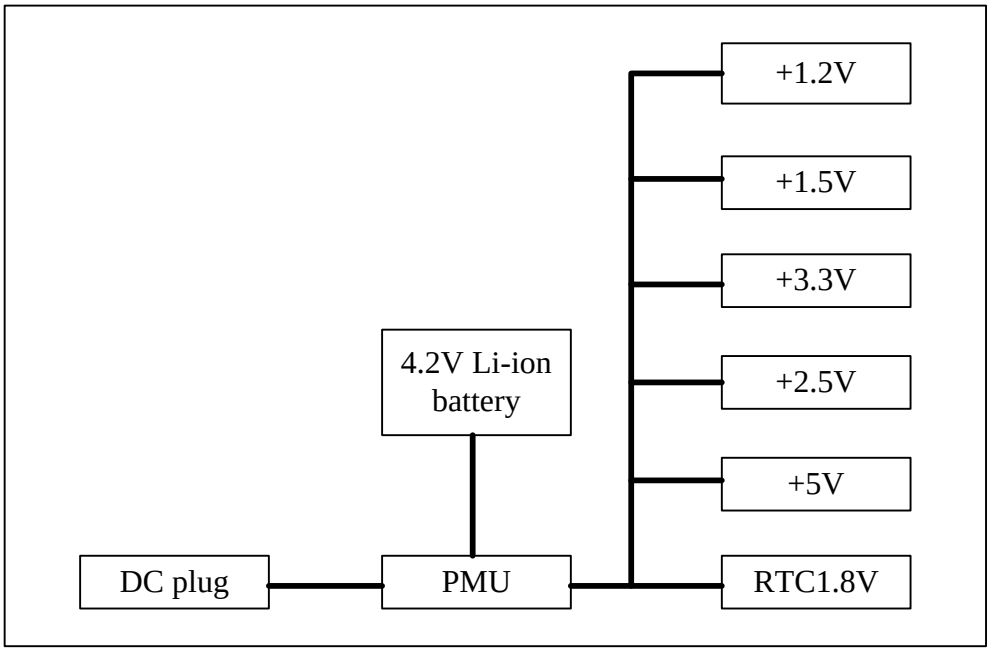
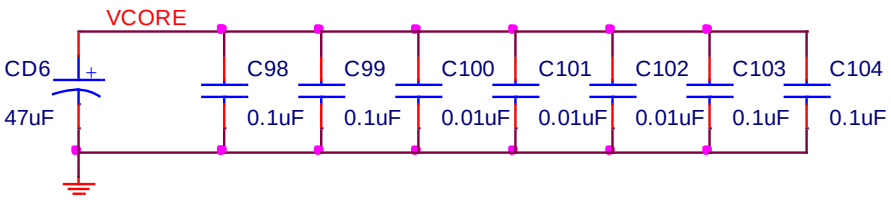
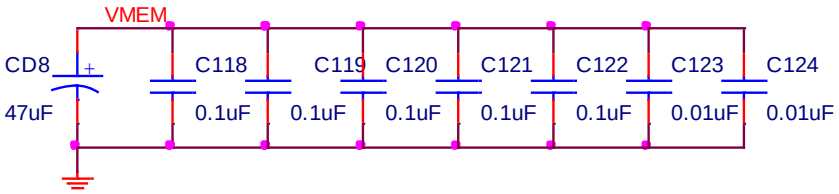


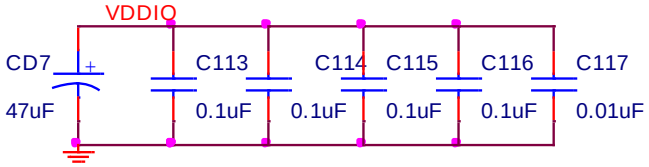
Figure 16-1 Power Architecture

16.2 Power Delivery and Decoupling

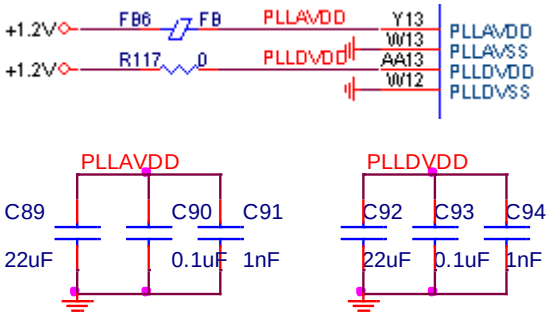
The VDDIO (+3.3V), VMEM (+1.5V) and VDDCORE (+1.2V) of JZ4775 should be decoupled with 100nF, 10nF and 1nF capacitor.



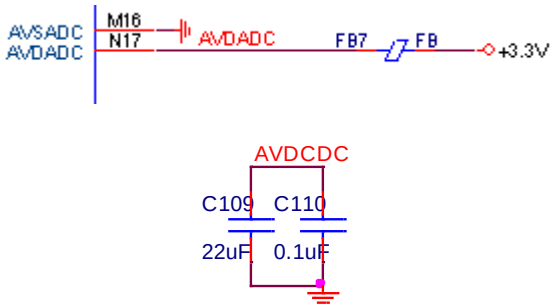




The Power of PLL should be as the following circuit.



The power of ADC should be as the following circuit.



The power of RTC should be as the following circuit. The capacitors should be placed near the Pin of power. The traces from capacitor to the Pin should be short and width.