

JZ4760B

32 Bits Microprocessor

Application Notes 01

The Difference Between JZ4760B & JZ4760

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JZ4760B 32 Bits Microprocessor

Application Notes 01

The Difference Between JZ4760B & JZ4760

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Release history

Date	Revision	Change
Sep. 2010	0.1	First release
Nov. 2010	0.2	Add Section 4 and Section 5

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1 Change from JZ4760

Compared to JZ4760, there are some improvement in JZ4760B such as smaller die size, higher performance (enough power supply for whole chip), IO driven strength controllable which is good for eliminating EMC/EMI issue, OTP available, higher internal bus efficiency which results in better support for large panel display and multi-media play, picture enhancing, more EPD panel support, frame compress/de-compress support, etc..

2 Hardware Compatibility

JZ4760B is pin-to-pin compatible with JZ4760, so the product designed with JZ4760 can be replaced by JZ4760B directly. Since the JZ4760B support OTP function, if the user want to use this function in assembly, the hardware design should be a little fine-tune. Please refer to the circuit and description as below:

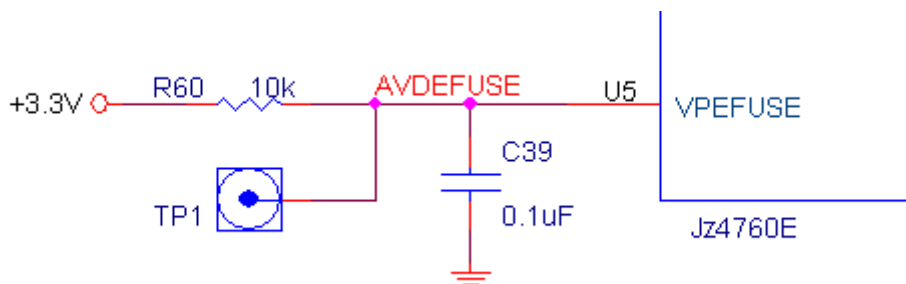


Figure 1

Note:

In figure 1, VPEFUSE connect to 3.3V power supply normally. When EFUSE programming, connect VPEFUSE to 6.5V±0.25V power supply through test point TP1.

3 Block Changing and Improving

JZ4760B has more improvement in some functions, so the system software should be modified carefully to support these new functions.

- **DDR**
 - Remove control register for write DQS control
 - Add pad control register

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- Timing improve

 - **AHB Arbiter**
 - Add priority order control
 - Bus transfer performance improve

 - **LCDC**
 - EPD(Electronic Paper Display) improving for more panel support
 - Display performance improve including output buffer enlarge, bus priority control, etc.
 - Add in frame de-compress function

 - **IPU**
 - Add picture enhance function
 - Bus priority control

 - **DMA**
 - Add another PCM interface and I2CI DMA support
 - Add DCKES and DCKEC register for clock control

 - **MDMA**
 - Add DCKES and DCKEC register for clock control

 - **OTP**
 - Add OTP memory and the controller

 - **CIM**
 - Add YCbCr data separate mode which Y/Cb/Cr can be put in different buffers in memory
 - Performance improve including data buffer enlarge from 64 to 256 level, bus priority control, etc.

 - **BCH**
 - Adjust the each error location in error report register

 - **BDMAC**
 - Support bch auto correction
 - Support Nand status read
 - Support two Nand Rb request and two chip select for interleave two plane operation
 - Add DCKES and DCKEC register for clock control

 - **NEMC**
 - Remove 2xhclk clock
 - Extend field of STRV, etc.
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- Output RDWR signal

- **Multi-Media**
 - Change TCSM1 from 48KB to 32KB
 - Change internal SRAM from 32KB to 12KB
 - Remove GPDMA2
 - Remove ME module
 - Add in GPVLC (General purpose VLC engine)
 - Improve MC (add in 6KB cache, tile reference)
 - Add in internal TLB

- **SADC**
 - Move VBAT reference control from CPM in SADC
 - Add pendown detection disable control

- **CPM**
 - Remove ½ divider from EXCLK
 - Remove divider for NEMC
 - Remove divider for GPS
 - Remove EXCLK input select for LCD
 - Add Stop/Reset function for Multi-Media for exception handling

- **TCU**
 - Add RTC clock bypass mode
 - Add 64bit OST

- **I2CI**
 - Add DMA transfer request
 - Receive and Transmit buffer enlarge from 2 to 16 level
 - Stop controllable

- **INTC**
 - Add new interrupt for another PCM, etc.

- **GPIO**
 - Add driven strength and slew rate control for part of gpio
 - Add PCM1 function multiplexer
 - Add RDWR function multiplexer
 - Add some EPD panel function multiplexer

- **PCM**
 - Add another PCM Interface and controller

- **AOSD_COMP**
 - Add module AOSD_COMP (Alpha OSD and frame compress controller)

4 Processor's ID

The register Processor Identification (CP0 Register 15, Select 0) is the same between JZ4760 and JZ4760B. There is another register should be used to identify these two processors:

- **Bit 31 of register CLKGR0 in CPM module, Address: 0x1000020**

	Jz4760	Jz4760B
Bit 31 Initial Value	0	1

5 Main Frequency

The tables below list the reference for the running frequency.

- **JZ4760**

Core voltage (Vcore)	Main Frequency
1.35V	528MHz

- **JZ4760B**

Core voltage (Vcore)	Main Frequency
TBD	528MHz
TBD	600MHz