INGENIC

RD4755_Cetus Development Board
Schematic Revision 1.3

INGENIC Semiconductor Corporation

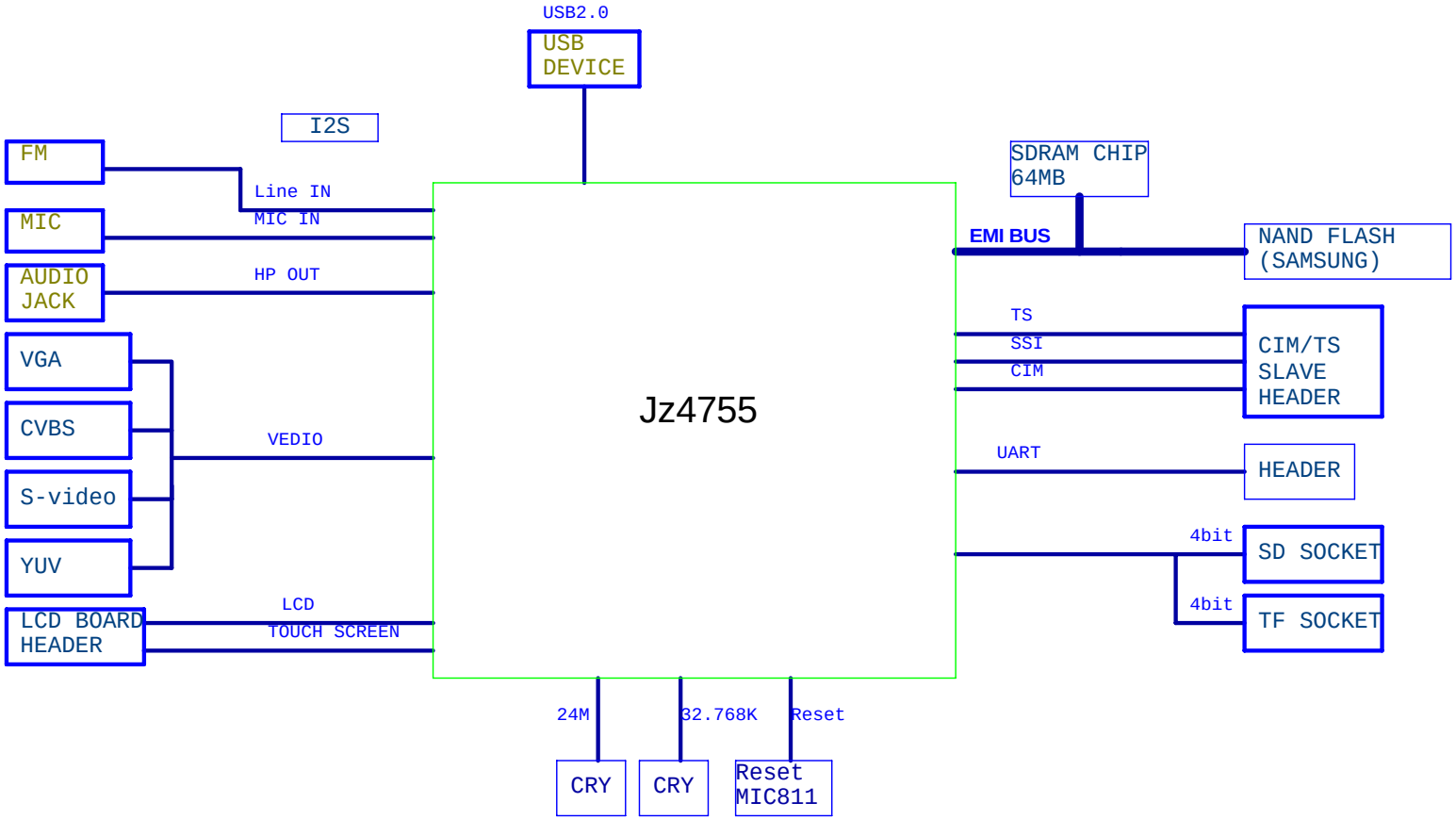
System Technology Department

INGENIC Semiconductor Co.,Ltd.

Title: RD4755_Cetus Development Board

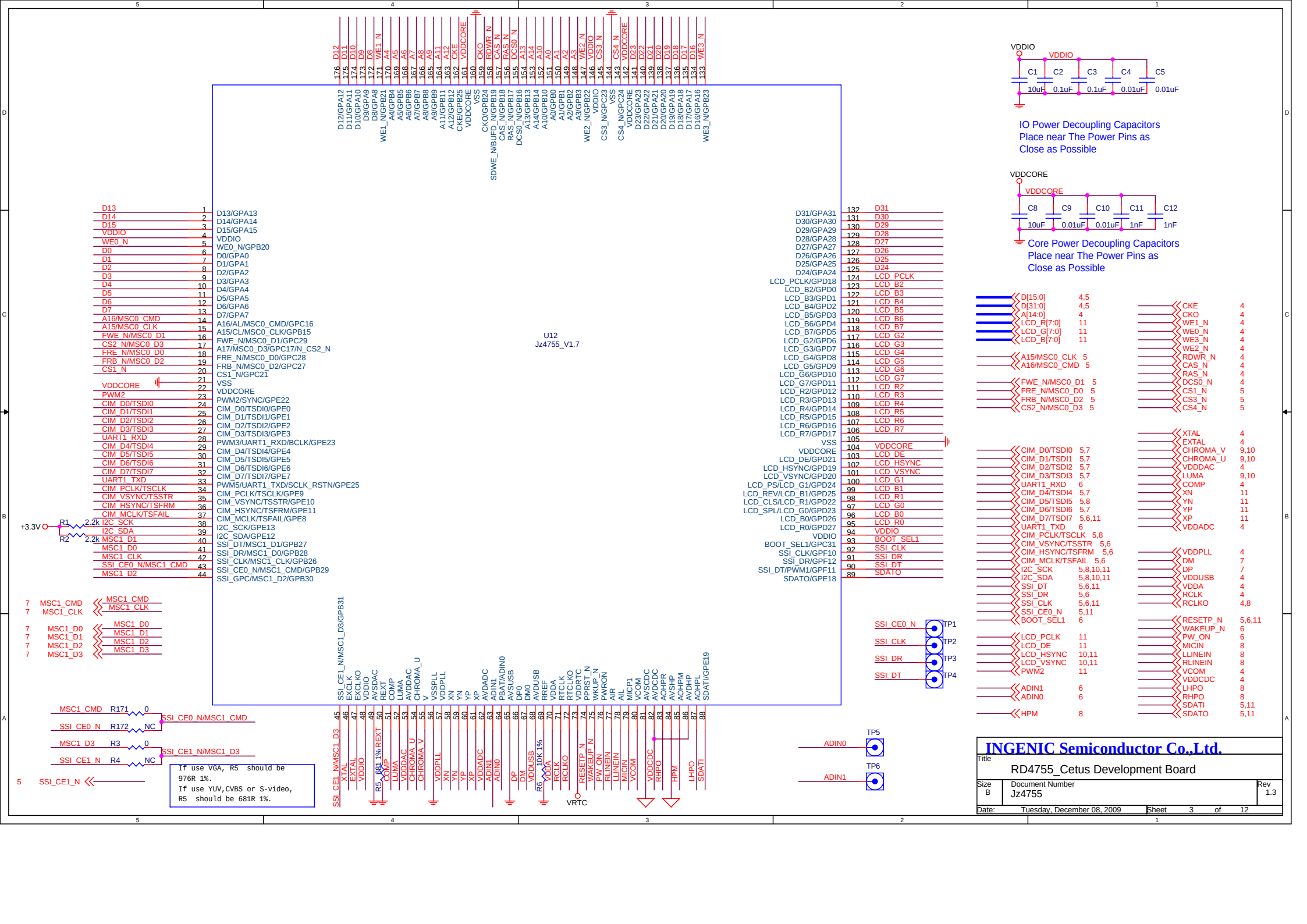
Size: B | Document Number: Cover | Rev: 1.3

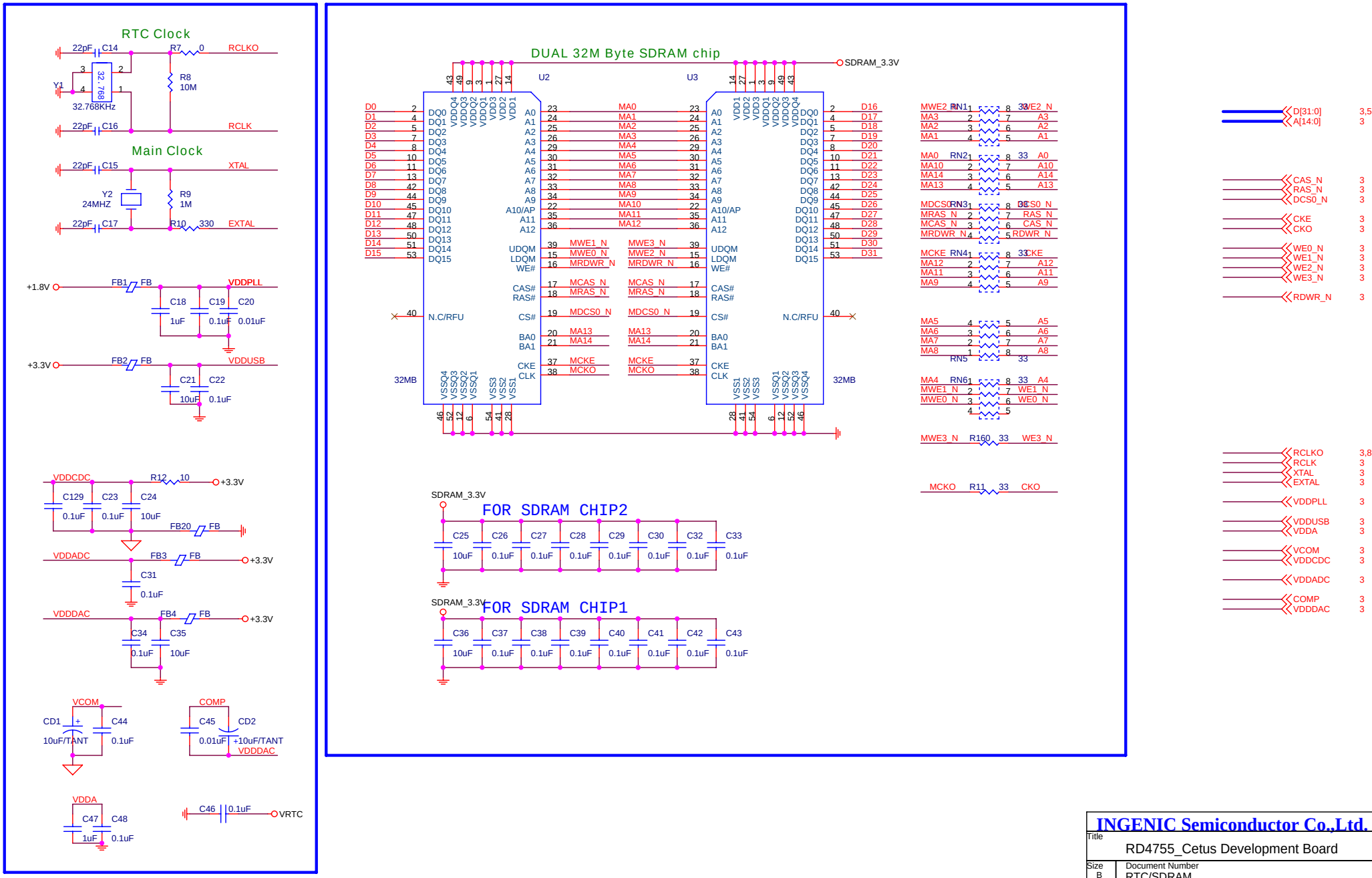
Date: Tuesday, December 08, 2009 | Sheet 1 of 12



INGENIC Semiconductor Co.,Ltd.

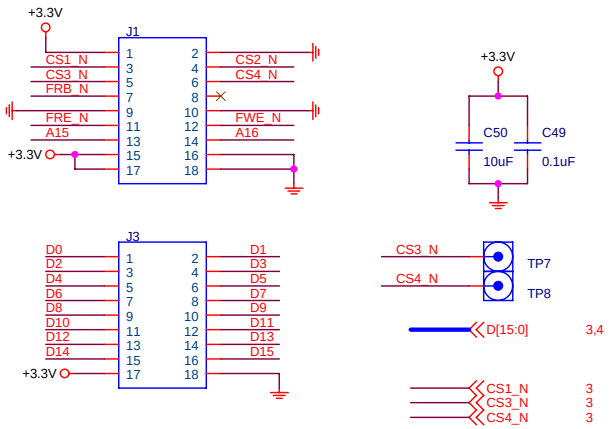
Title: RD4755_Cetus Development Board		
Size: B	Document Number: System Architecture	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 2 of 12	


U12
Jz4755_V1.7
D13/GPA13
D14/GPA14
D15/GPA15
VDDIO
WE0_N/GPB20
D0/GPA0
D1/GPA1
D2/GPA2
D3/GPA3
D4/GPA4
D5/GPA5
D6/GPA6
D7/GPA7
A16/AL/MSC0_CMD/GPC16
A15/CL/MSC0_CLK/GPB15
FWE_N/MSC0_D1/GPC29
A17/MSC0_D3/GPC17/N_CS2_N
FRE_N/MSC0_D0/GPC28
FRB_N/MSC0_D2/GPC27
CS1_N/GPC21
VSS
VDDCORE
PWM2/SYNC/GPE22
CIM_D0/TSDI0/GPE0
CIM_D1/TSDI1/GPE1
CIM_D2/TSDI2/GPE2
CIM_D3/TSDI3/GPE3
PWM3/UART1_RXD/BCLK/GPE23
CIM_D4/TSDI4/GPE4
CIM_D5/TSDI5/GPE5
CIM_D6/TSDI6/GPE6
CIM_D7/TSDI7/GPE7
PWM5/UART1_TXD/SCLK_RSTN/GPE25
CIM_PCLK/TSCLK/GPE9
CIM_VSYNC/TSSTR/GPE10
CIM_HSYNC/TSFRM/GPE11
CIM_MCLK/TSFAIL/GPE8
I2C_SCK/GPE13
I2C_SDA/GPE12
SSI_DT/MSC1_D1/GPB27
SSI_DR/MSC1_D0/GPB28
SSI_CLK/MSC1_CLK/GPB26
SSI_CE0_N/MSC1_CMD/GPB29
SSI_GPC/MSC1_D2/GPB30
D31/GPA31
D30/GPA30
D29/GPA29
D28/GPA28
D27/GPA27
D26/GPA26
D25/GPA25
D24/GPA24
LCD_PCLK/GPD18
LCD_B2/GPD0
LCD_B3/GPD1
LCD_B4/GPD2
LCD_B5/GPD3
LCD_B6/GPD4
LCD_B7/GPD5
LCD_G2/GPD6
LCD_G3/GPD7
LCD_G4/GPD8
LCD_G5/GPD9
LCD_G6/GPD10
LCD_G7/GPD11
LCD_R2/GPD12
LCD_R3/GPD13
LCD_R4/GPD14
LCD_R5/GPD15
LCD_R6/GPD16
LCD_R7/GPD17
VSS
VDDCORE
LCD_DE/GPD21
LCD_HSYNC/GPD19
LCD_VSYNC/GPD20
LCD_PS/LCD_G1/GPD24
LCD_REV/LCD_B1/GPD25
LCD_CLS/LCD_R1/GPD22
LCD_SPL/LCD_G0/GPD23
LCD_B0/GPD26
LCD_R0/GPD27
VDDIO
BOOT_SEL1/GPC31
SSI_CLK/GPF10
SSI_DR/GPF12
SSI_DT/PWM1/GPF11
SDATO/GPE18
SSI_CE1_N/MSC1_D3/GPB31
EXCLK
EXCLKO
VDDIO
AVSDAC
REXT
COMP
LUMA
AVDDAC
CHROMA_U
V
VSSPLL
VDDPLL
XN
YN
YP
XP
AVDADC
ADIN1
PBAT/ADIN0
AVSUSB
DP0
DM0
AVDUSB
RREF
VDDA
RTCLK
RTCLKO
VDDRTC
PRSTT_N
WAKUP_N
PWRON
AIR
AIL
MICP1
VCOM
AVSCDC
AVDCDC
AOHPR
AVSHP
AOHPM
AVDHP
AOHPL
SDATI/GPE19
XTAL
EXTAL
VDDIO
R5 681 1%
COMP
LUMA
VDDDAC
CHROMA_U
CHROMA_V
VDDPLL
XN
YN
YP
XP
VDDADC
ADIN1
ADIN0
DP
DM
VDDUSB
R6 10K 1%
VDDA
RCLK
RCLKO
RESETP_N
WAKEUP_N
PW_ON
RLINEIN
LLINEIN
MICIN
VCOM
VDDCDC
RHPO
HPM
LHPO
SDATI
VRTC
VDDIO
C1 10uF
C2 0.1uF
C3 0.1uF
C4 0.01uF
C5 0.01uF
IO Power Decoupling Capacitors
Place near The Power Pins as
Close as Possible
VDDCORE
C8 10uF
C9 0.01uF
C10 0.01uF
C11 1nF
C12 1nF
Core Power Decoupling Capacitors
Place near The Power Pins as
Close as Possible
D[15:0] 4,5
D[31:0] 4,5
A[14:0] 4
LCD_R[7:0] 11
LCD_G[7:0] 11
LCD_B[7:0] 11
A15/MSC0_CLK 5
A16/MSC0_CMD 5
FWE_N/MSC0_D1 5
FRE_N/MSC0_D0 5
FRB_N/MSC0_D2 5
CS2_N/MSC0_D3 5
CKE 4
CKO 4
WE1_N 4
WE0_N 4
WE3_N 4
WE2_N 4
RDWR_N 4
CAS_N 4
RAS_N 4
DCS0_N 4
CS1_N 5
CS3_N 5
CS4_N 5
CIM_D0/TSDI0 5,7
CIM_D1/TSDI1 5,7
CIM_D2/TSDI2 5,7
CIM_D3/TSDI3 5,7
UART1_RXD 6
CIM_D4/TSDI4 5,7
CIM_D5/TSDI5 5,8
CIM_D6/TSDI6 5,7
CIM_D7/TSDI7 5,6,11
UART1_TXD 6
CIM_PCLK/TSCLK 5,8
CIM_VSYNC/TSSTR 5,6
CIM_HSYNC/TSFRM 5,6
CIM_MCLK/TSFAIL 5,6
I2C_SCK 5,8,10,11
I2C_SDA 5,8,10,11
SSI_DT 5,6,11
SSI_DR 5,6
SSI_CLK 5,6,11
SSI_CE0_N 5,11
BOOT_SEL1 6
LCD_PCLK 11
LCD_DE 11
LCD_HSYNC 10,11
LCD_VSYNC 10,11
PWM2 11
ADIN1 6
ADIN0 6
HPM 8
XTAL 4
EXTAL 4
CHROMA_V 9,10
CHROMA_U 9,10
VDDDAC 4
LUMA 9,10
COMP 4
XN 11
YN 11
YP 11
XP 11
VDDADC 4
VDDPLL 4
DM 7
DP 7
VDDUSB 4
VDDA 4
RCLK 4
RCLKO 4,8
RESETP_N 5,6,11
WAKEUP_N 6
PW_ON 6
MICIN 8
LLINEIN 8
RLINEIN 8
VCOM 4
VDDCDC 4
LHPO 8
RHPO 8
SDATI 5,11
SDATO 5,11
+3.3V
R1 2.2k
R2 2.2k
I2C_SCK
I2C_SDA
MSC1_D1
MSC1_D0
MSC1_CLK
SSI_CE0_N/MSC1_CMD
MSC1_D2
7 MSC1_CMD
7 MSC1_CLK
7 MSC1_D0
7 MSC1_D1
7 MSC1_D2
7 MSC1_D3
MSC1_CMD R171 0
SSI_CE0_N R172 NC
MSC1_D3 R3 0
SSI_CE1_N R4 NC
5 SSI_CE1_N
If use VGA, R5 should be 976R 1%.
If use YUV,CVBS or S-video, R5 should be 681R 1%.
SSI_CE0_N
SSI_CLK
SSI_DR
SSI_DT
TP1
TP2
TP3
TP4
ADIN0
ADIN1
TP5
TP6
INGENIC Semiconductor Co.,Ltd.
Title
RD4755_Cetus Development Board
Size B
Document Number
Jz4755
Rev 1.3
Date: Tuesday, December 08, 2009
Sheet 3 of 12

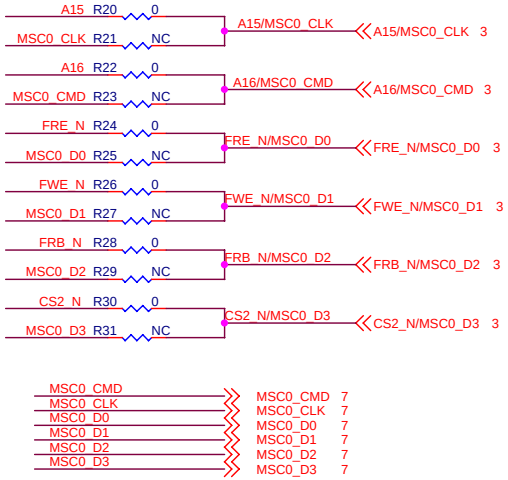


INGENIC Semiconductor Co.,Ltd.		
Title: RD4755_Cetus Development Board		
Size: B	Document Number: RTC/SDRAM	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 4 of 12	

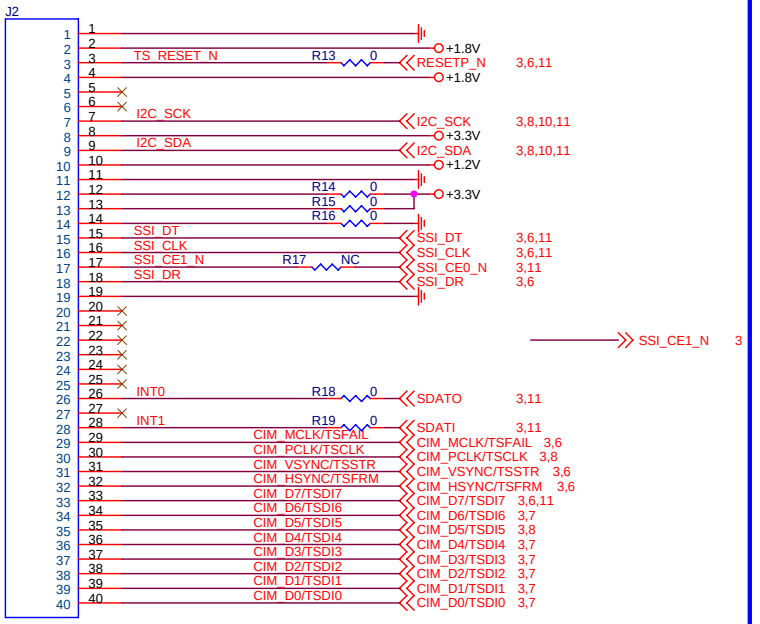
NAND Flash Socket

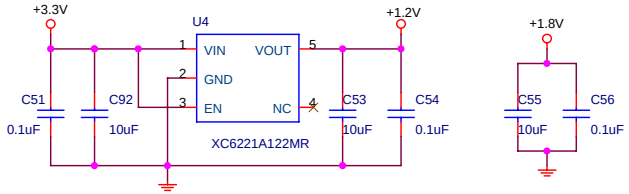


Note:Nand Flash signals are multiplex with SD:MSC0 signals.



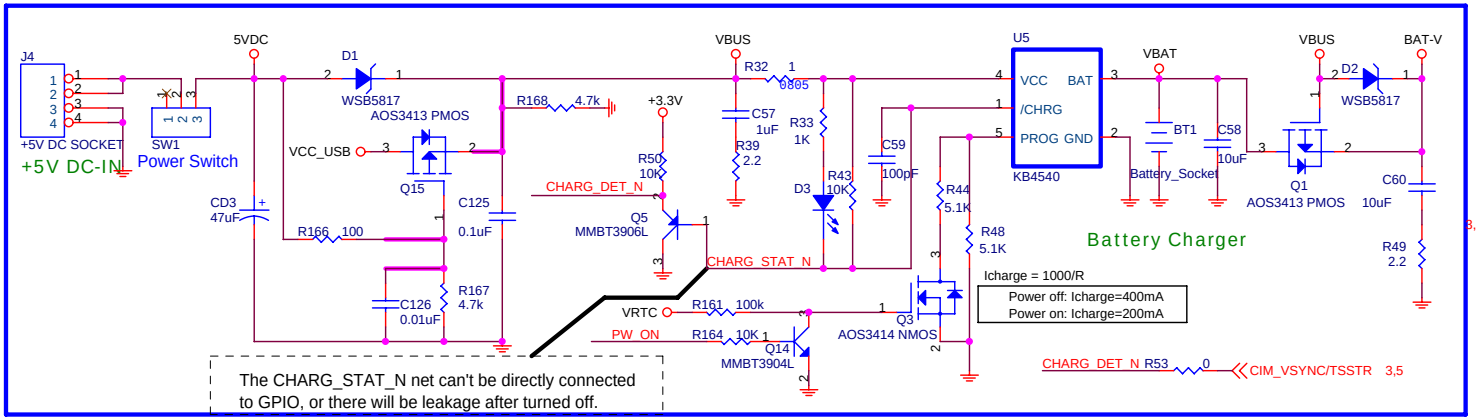
TS/Camera Interface Connector

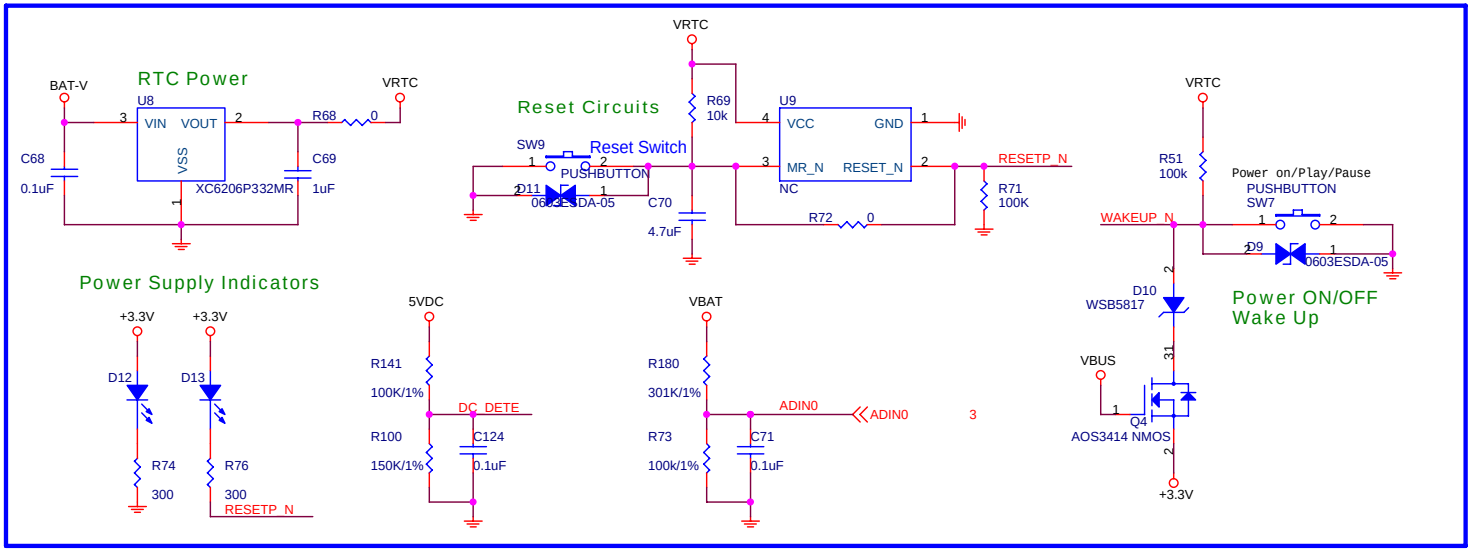


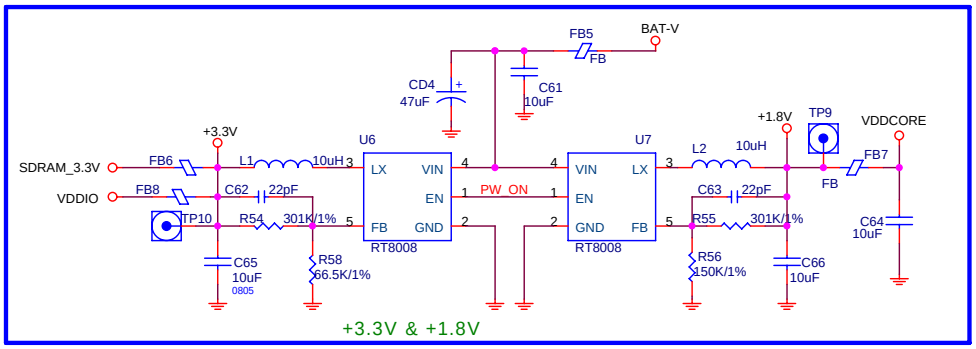


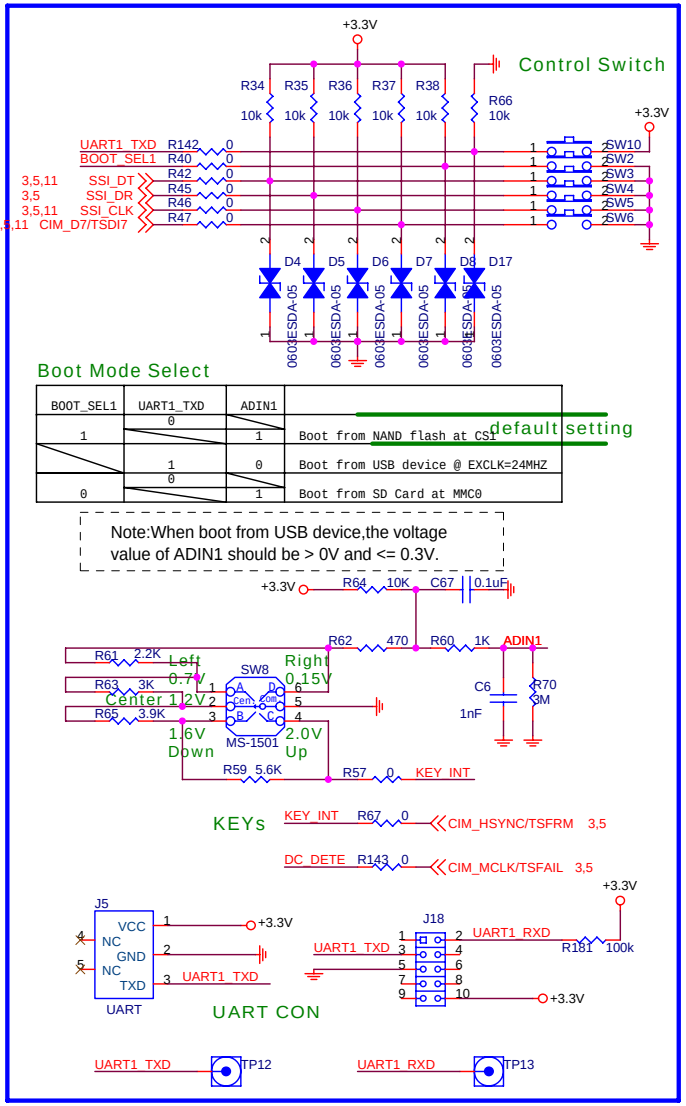
INGENIC Semiconductor Co.,Ltd.

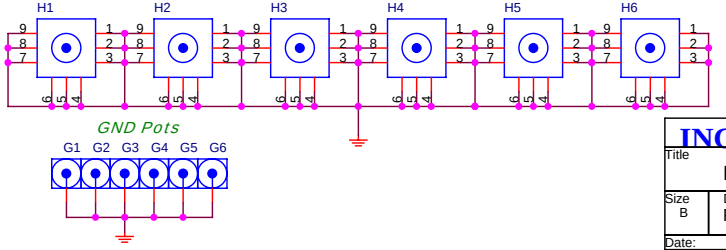
Title: RD4755_Cetus Development Board		
Size: B	Document Number: Static Memory/TS/Camera	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 5 of 12	







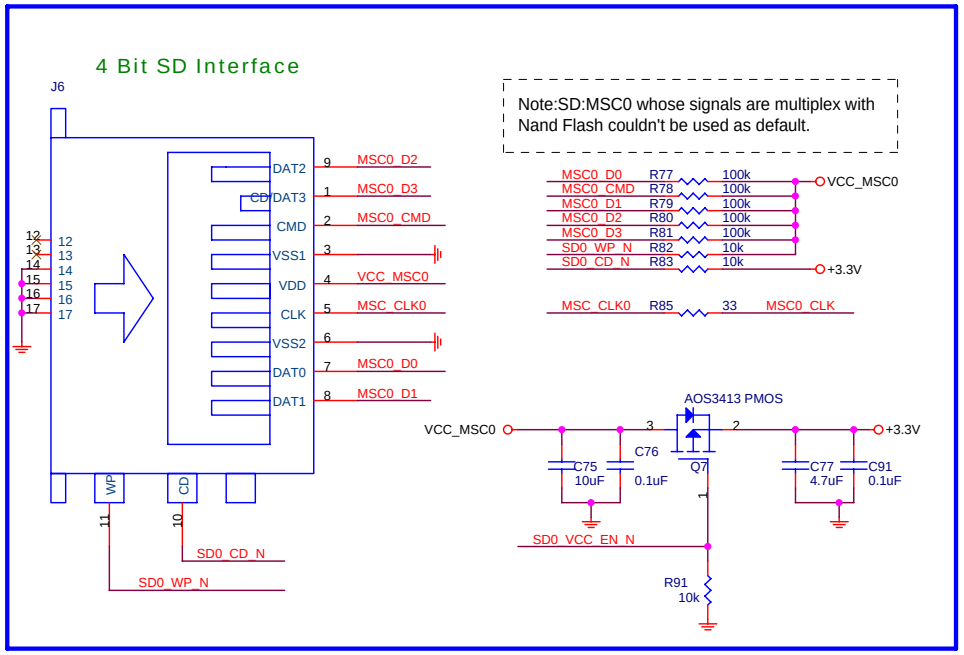


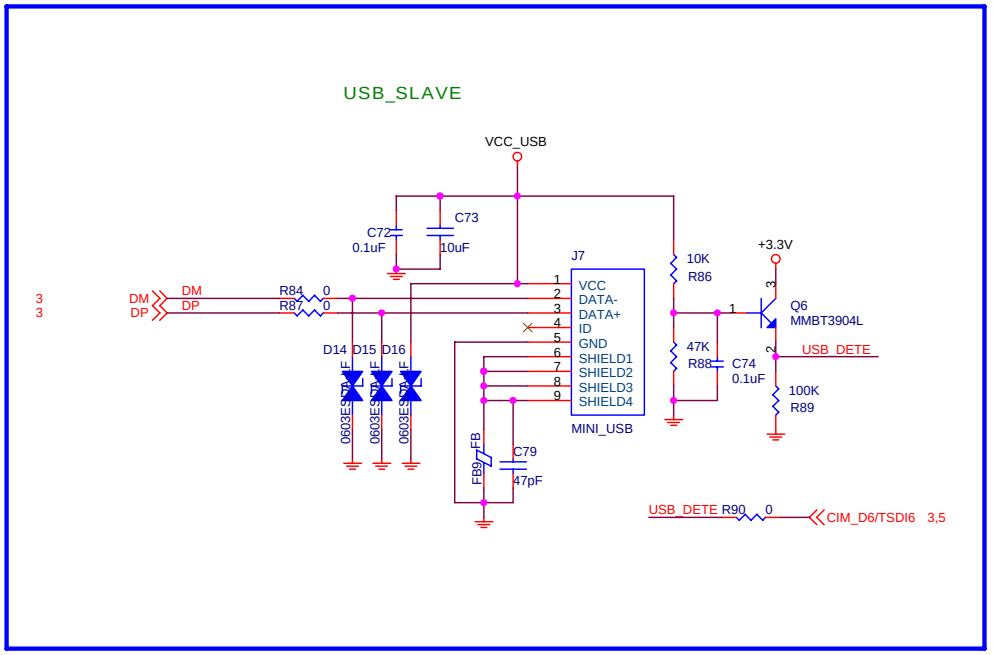


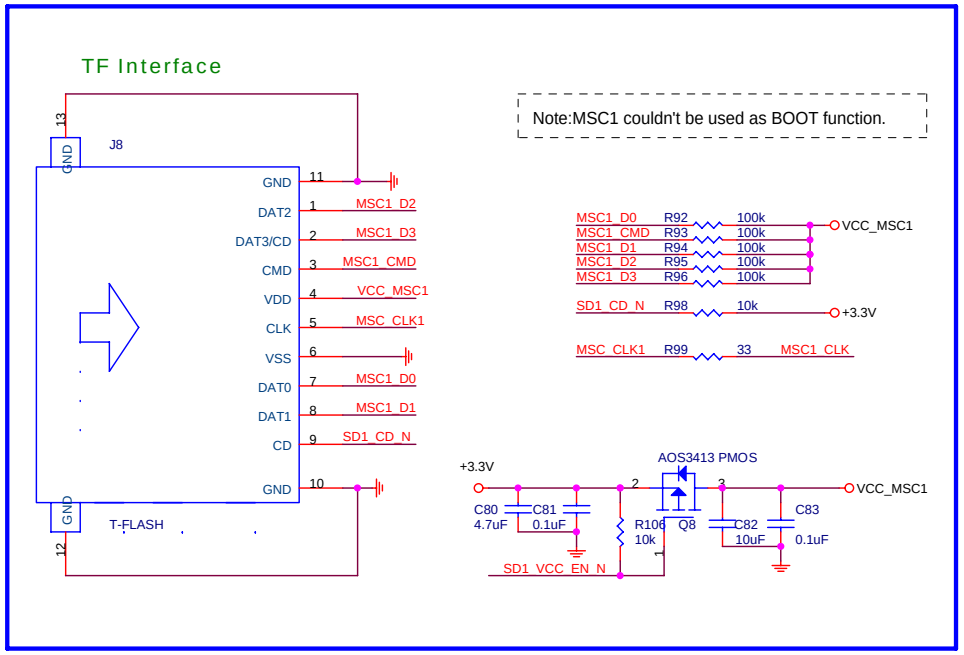
BOOT_SEL1	UART1_TXD	ADIN1	
1	0	1	Boot from NAND flash at CS1
	1	0	Boot from USB device @ EXCLK=24MHZ
0	0	1	Boot from SD Card at MMC0

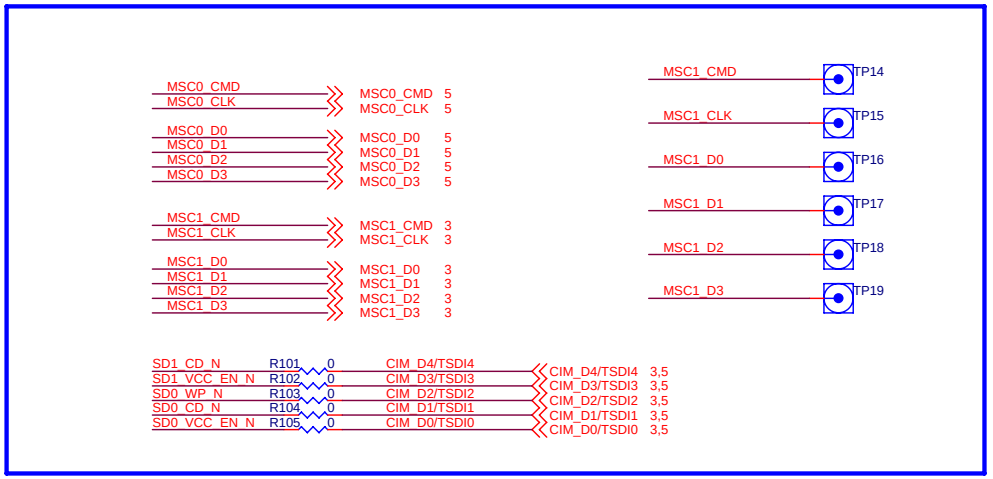
INGENIC Semiconductor Co.,Ltd.

Title	RD4755_Cetus Development Board	
Size B	Document Number POWER/Boot/Reset	Rev 1.3
Date: Tuesday, December 08, 2009	Sheet 6 of 12	





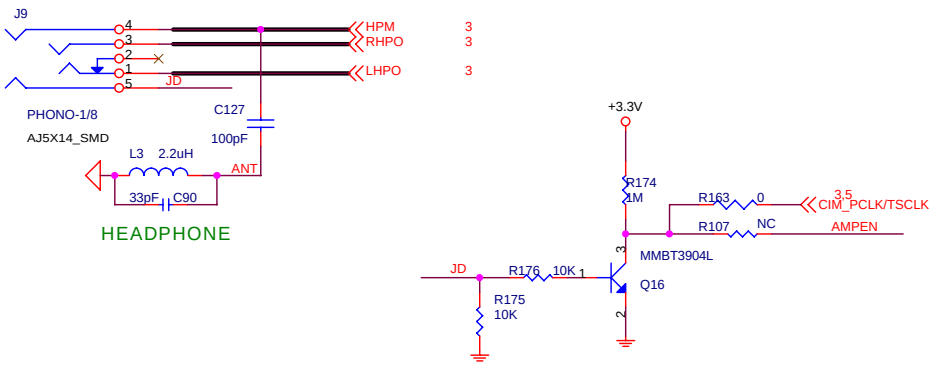




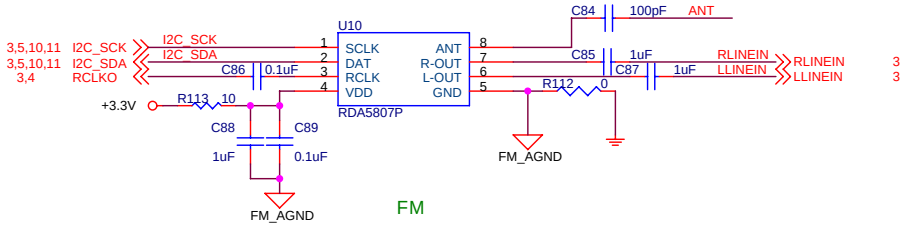
INGENIC Semiconductor Co.,Ltd.

Title: RD4755_Cetus Development Board		
Size: B	Document Number: SD/USB	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 7 of 12	

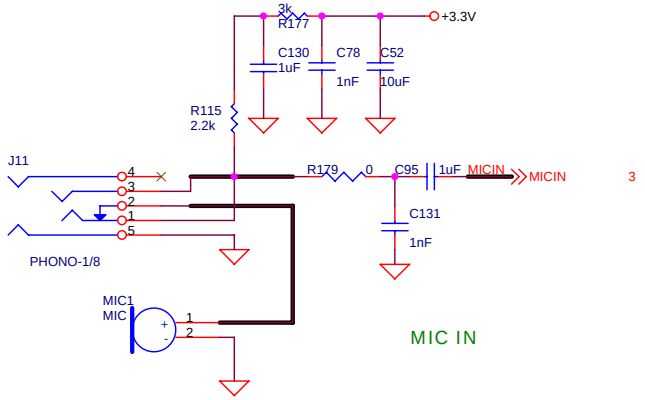
The trace between the HPM pin and the headphone jack must be as short as possible.



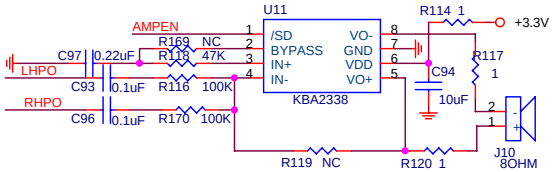
HEADPHONE



FM

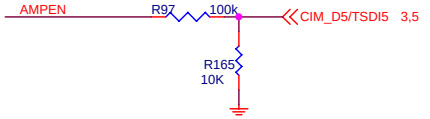


MIC IN



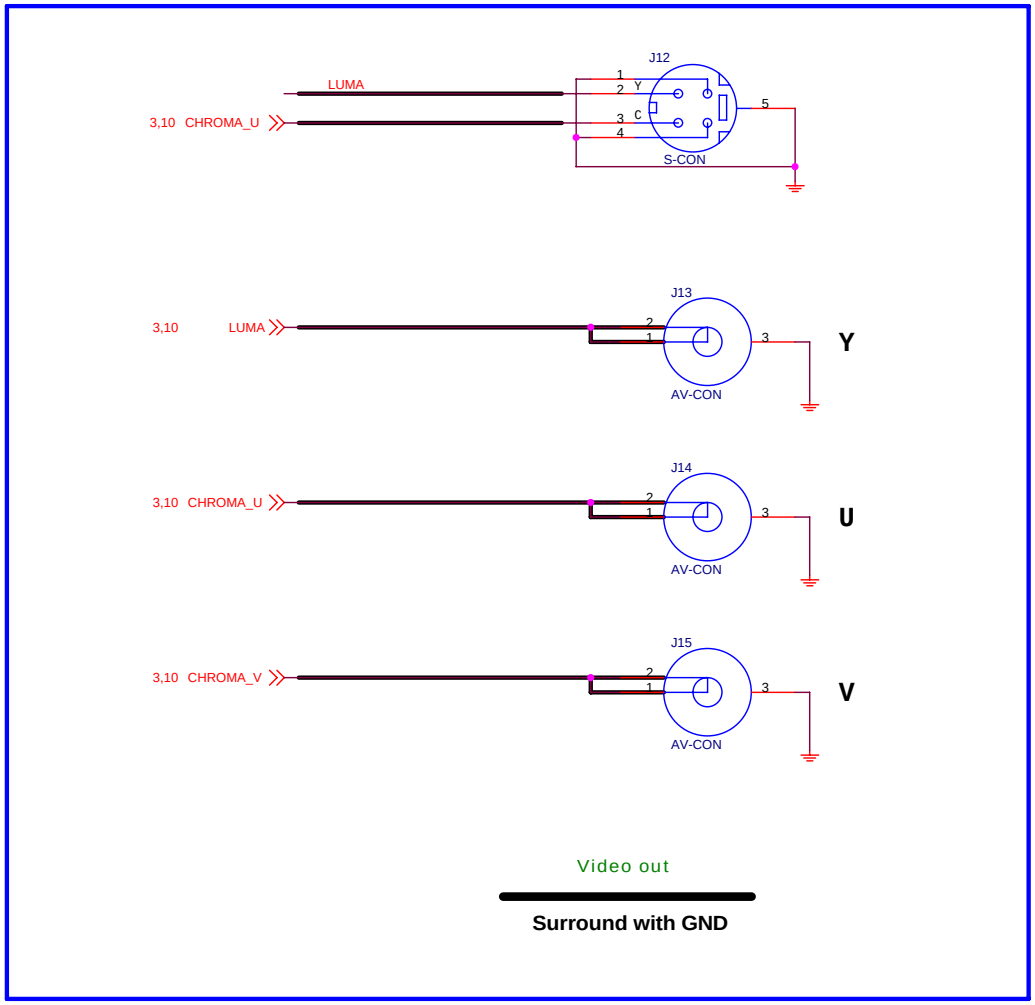
If U11 is LM4890, R169=0R,R118=0,C97=0.1uF,R119=20K.

Speaker Out Connector

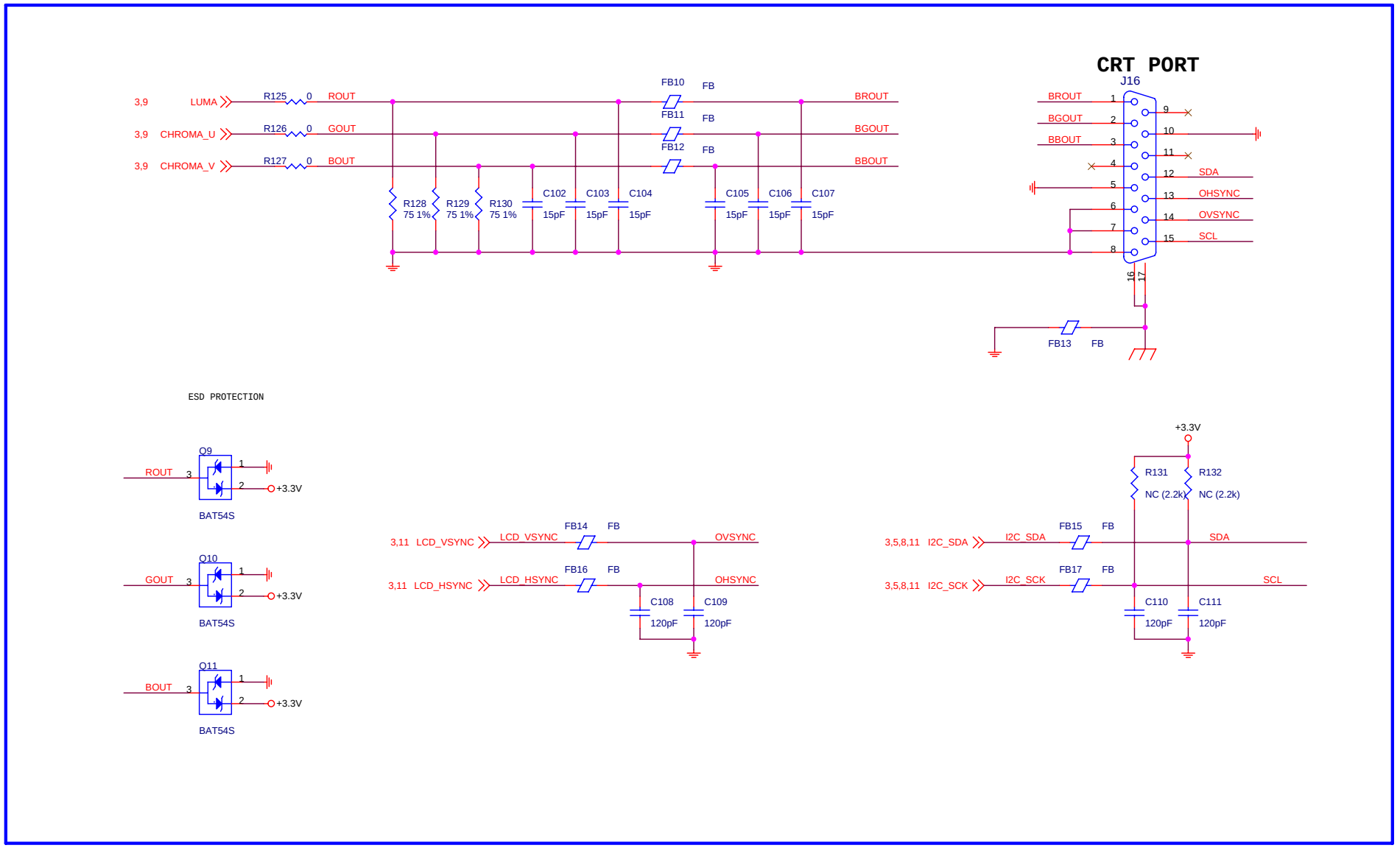


Surround with GND

INGENIC Semiconductor Co.,Ltd.		
Title: RD4755_Cetus Development Board		
Size: B	Document Number: Audio/FM	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 8 of 12	

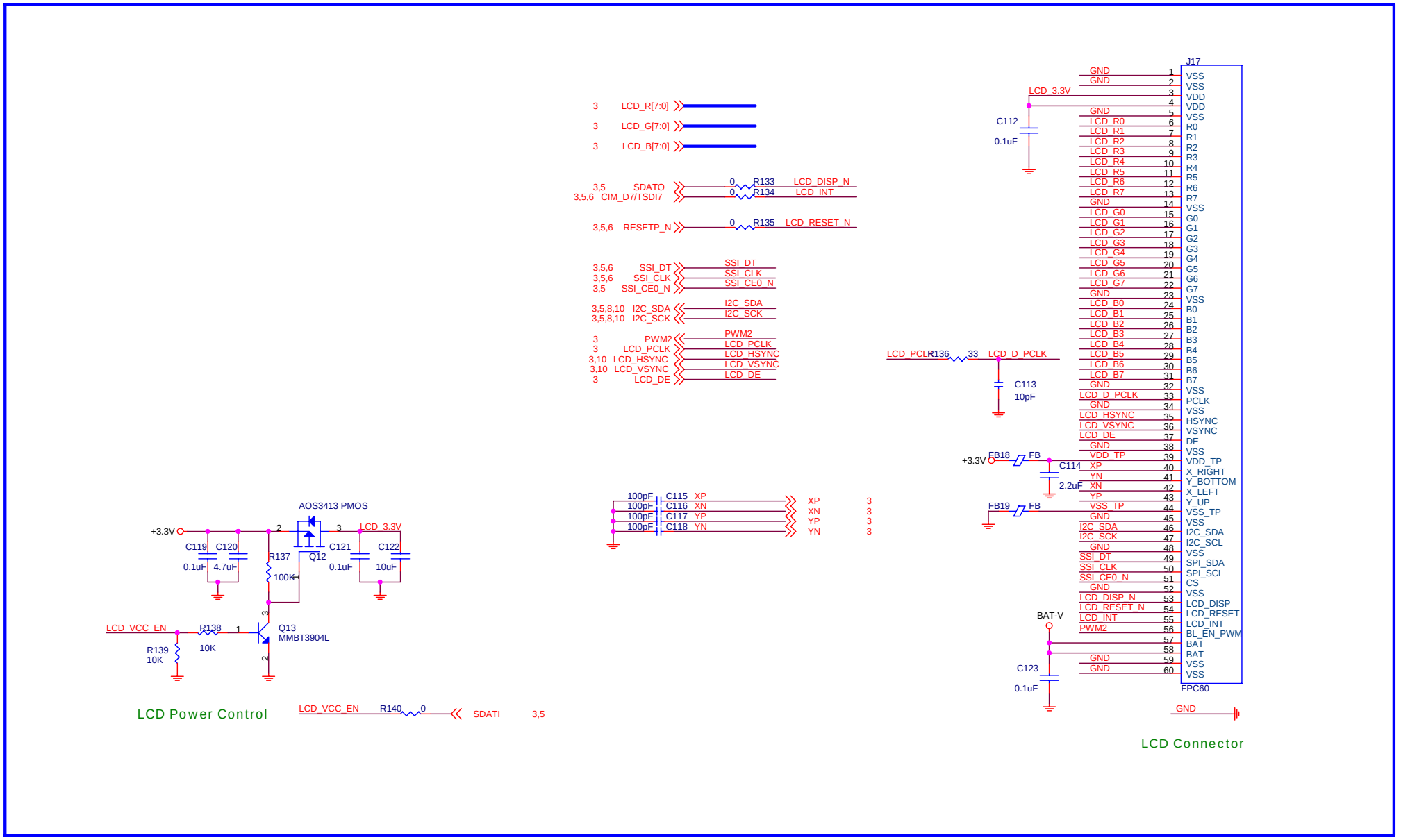


INGENIC Semiconductor Co.,Ltd.		
Title: RD4755_Cetus Development Board		
Size: B	Document Number: Video	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 9 of 12	



INGENIC Semiconductor Co.,Ltd.

Title: RD4755_Cetus Development Board		
Size: B	Document Number: VGA	Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 10 of 12	



INGENIC Semiconductor Co.,Ltd.			
Title: RD4755_Cetus Development Board			
Size: B	Document Number: LCD		Rev: 1.3
Date: Tuesday, December 08, 2009	Sheet 11 of 12		

Data	Revision	Change
Mar. 09. 2009	Rev1.0	1. First Revision
Apr. 15. 2009	Rev1.1	1. PAGE06: Delete R41,Q2,R52. 2. PAGE06 :Change the Icharge control circuit. 3. PAGE06: Change the BAT detect circuit. 4. PAGE06: Change the control circuit of power supply. 5. PAGE07: Change C73 from 10uF to NC, in order to avoid a BAT-V negative pulse when USB device pull out. 6. PAGE08: Change CD5,CD6 to 220uF. 7. PAGE08: Add R163 for JACK_DETE and add R165 for AMPEN. 8. PAGE08: Change the amplifier enable net's name from "AMPEN_N" to "AMPEN" 9. PAGE09: Delete R121-R124 and C98-C101 for video out balance. 10. PAGE08: Add R169 for reserve. 11. PAGE03: Exchange LHPO's and RHPO's PIN numbers in Jz4755 source package. 12. PAGE03: Exchange AIL's and AIR's PIN numbers in Jz4755 source package. 13. PAGE08: Delete R108-R111. 14. PAGE08: Add FB20,FB21 for EMI. 15. PAGE08: Add R170.
Apr. 27. 2009	Rev1.2	1. PAGE03: Change the audio pins' number in Jz4755 source package. 2. PAGE03: ADD R171 and R172 to select SSI_CE0_N or MSC1_CMD. 3. PAGE06: Change the net of R47.1 from SSI_CE0_N to CIM_D7/TSDI7. 4. PAGE08: Change HPOUT circuit.
May. 04. 2009	Rev1.2.1	1. PAGE04: ADD R173 for AGND partition.
Aug. 14. 2009	Rev1.3	1. PAGE03: Change the Jz4755 decouple capcitors. 2. PAGE04: Add C129 for VDDCDC's decouple. 3. PAGE06: Change BAT detect circuit for protecting ADIN0. 4. PAGE06: ADD R181 for UART1_RXD. 5. PAGE08: Change the JACK_DETE circuit. 6. PAGE08: Change the MIC IN circuit. 7. PAGE08: Change R173 to FB20. 8. PAGE08: Change R97 to 100k. 9. PAGE08: Change R174 to 1M.

INGENIC Semiconductor Co.,Ltd.

Title: RD4755_Cetus Development Board

Size: B | Document Number: History | Rev: 1.3

Date: Tuesday, December 08, 2009 | Sheet 12 of 12