JZ4755A

Mobile Application Processor

Data Sheet

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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1 Overview

JZ4755A is a multimedia application processor targeting for multimedia rich and mobile devices like PMP, mobile digital TV, and GPS. This SOC introduces an innovative dual-core architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices.

The CPU (Central Processing Unit) core, equipped with 16K instruction cache and 16K data cache operating at 400MHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst processor engine. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption.

The VPU (Video Processing Unit) core is powered with another XBurst processor engine. The SIMD instruction set implemented by XBurst engine, in together with the on chip video accelerating engine and post processing unit, delivers doubled video performance comparing with the single core implementation.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit/8-bit/12-bit ECC MLC NAND flash memory for cost sensitive applications.

On-chip modules such as LCD controller, audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. TV encoder unit and 3 channels 10-bits DACs provide composite/S-video/component TV signal output in PAL or NTSC format. In addition, XVGA output up to 1024x768 is provided. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB 2.0 device, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

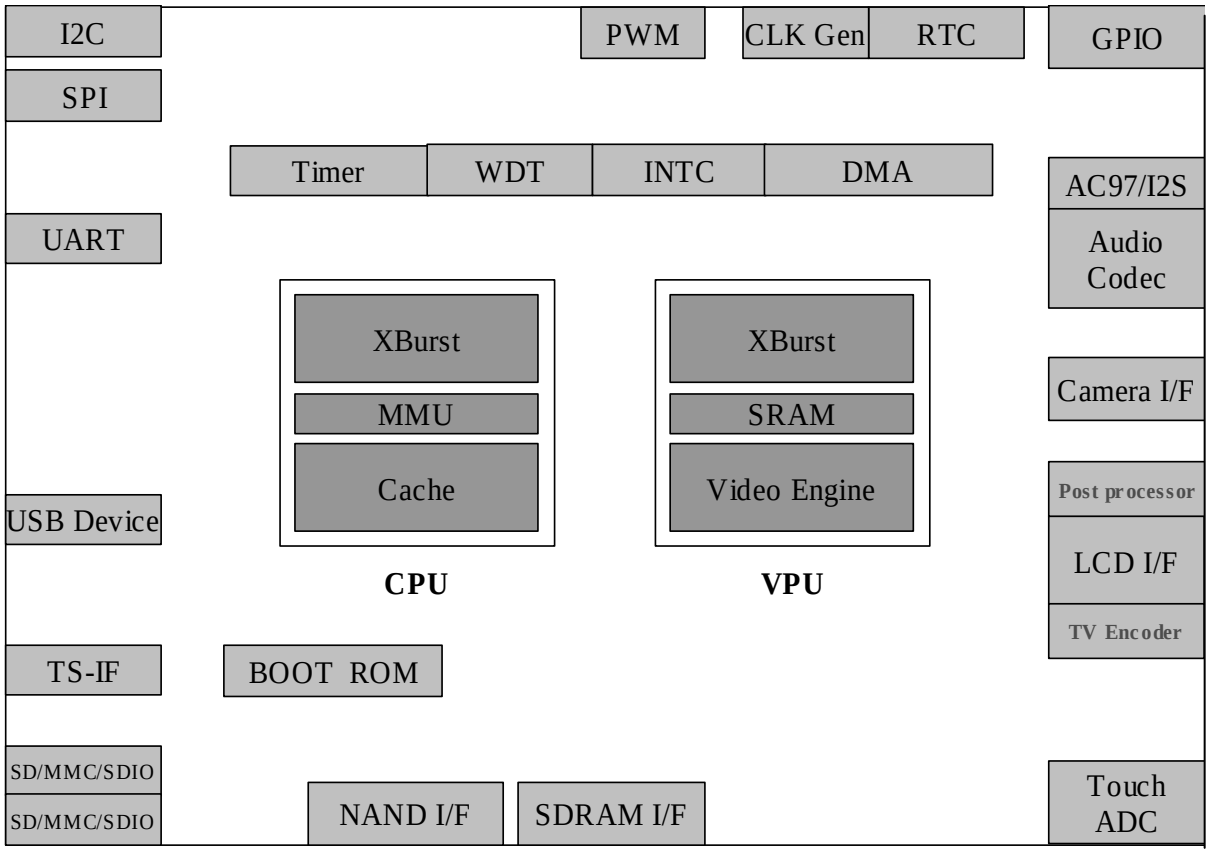


Figure 1-1 JZ4755A Diagram

1.2 Features

1.2.1 CPU Core

- XBurst CPU
  - XBurst® RISC instruction set to support Linux and WinCE
  - XBurst® SIMD instruction set to support multimedia acceleration
  - XBurst® 8-stage pipeline micro-architecture up to 360MHz
- MMU
  - 32-entry dual-pages joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16K instruction cache
  - 16K data cache
- Hardware debug support
- 16kB tight coupled memory

1.2.2 VPU core

- XBurst CPU for video processing
  - XBurst® RISC instruction set to support Linux and WinCE
  - XBurst® SIMD instruction set to support multimedia acceleration
  - XBurst® 8-stage pipeline micro-architecture up to 360MHz
- Video acceleration engine
  - Motion compensation
  - Motion estimation
  - De-block
  - DCT/IDCT for 4x4 block
- 32kB tight coupled memory

1.2.3 Memory Sub-systems

- NAND flash interface
  - Support 4-bit/8-bit/12-bit MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM iInterface
  - Standard SDRAM and Mobile SDRAM
  - Programmable size and base address
  - 16-bit data bus width
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions

- Supports power-down mode to minimize the power consumption of SDRAM
- Supports page mode
- 1 Chip select

- BCH Controller
  - Implement data ECC encoding and decoding
- Direct memory access controller
  - Eight independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
- The XBurst processor system supports little endian only

1.2.4 AHB Bus Arbiter

- Provide a fair chance for each AHB master to possess the AHB bus
- Fulfill the back-to-back feature of AHB protocol
- Divide two master groups with different privileges supports two arbitrating methods: Round-robin possession for masters in the same group, Preemptive possession for masters with higher privileges

1.2.5 System Devices

- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 24MHz clock
  - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, HCLK, HHCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
  - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling

- Unmasked interrupts can wake up the chip in sleep or standby mode

- Timer and counter unit with PWM output
  - Provide six separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Four PWM outputs
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (ext ernal clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset

1.2.6 Audio/Display/UI Interfaces

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 24-bit data bus
  - Support 1,2,4,8 pins STN panel, 16bit, 18bit and 24bit TFT and 8bit I/F TFT
  - Display size up to 1280×1024 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)
  - Support delta RGB
  - One single color background and two foreground OSD
- TV encoder
  - Support NTSC or PAL
  - Support CVBS or S-video or Component signals
  - 3 channel 10 bits DAC
- Image post processor
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert
- Camera interface module
  - Input image size up to 4096×4096 pixels
  - Supports CCIR656 data format
  - Bayer RGB, YCbCr 4:2:2 and YCbCr 4:4:4 data format

  - 32×32 image data receive FIFO with DMA support
- On-chip audio CODEC
  - 24-bit DAC, SNR: 90dB
  - 24-bit ADC, SNR: 85dB
  - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
  - L/R channels line input
  - MIC input
  - L/R channels headphone output amplifier support up to 16ohm load
  - Capacitor-coupled or capacitor-less
- AC97/I2S controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the on-chip CODEC
  - Support off-chip CODEC
- SADC
  - 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage input
  - 1 generic input channel

1.2.7 On-chip Peripherals

- General-Purpose I/O ports
  - Total GPIO pin number is 124
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up
- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- Synchronous serial interface
  - Up to 50MHz speed
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation

  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode
- USB 2.0 device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported
  - Embedded USB 2.0 PHY
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Support automatic boot up from MSC0, which has 4-bit data bus
  - MSC1 with 4-bit data bus
  - Compliant with “The MultiMediaCard System Specification version 4.2”
  - Compliant with “SD Memory Card Specification version 2.0” and “SDIO Card Specification version 1.0” with 1 command channel and 4 data channels
  - Up to 320 Mbps data rate in MSC0
  - Up to 320 Mbps data rate in MSC1
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 32x8bit FIFO for transmit and 32x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate
  - UART function up to 3.7Mbps baudrate
  - Hardware flow control
- Transport stream slave interface
  - 8-bit or 1-bit data bus selectable
  - Support PID filtering

1.2.8 Bootrom

- 8kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	0.16um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	LQFP176, 20mm x 20mm x 1.4mm, 0.4mm pitch
Operating frequency	400MHz

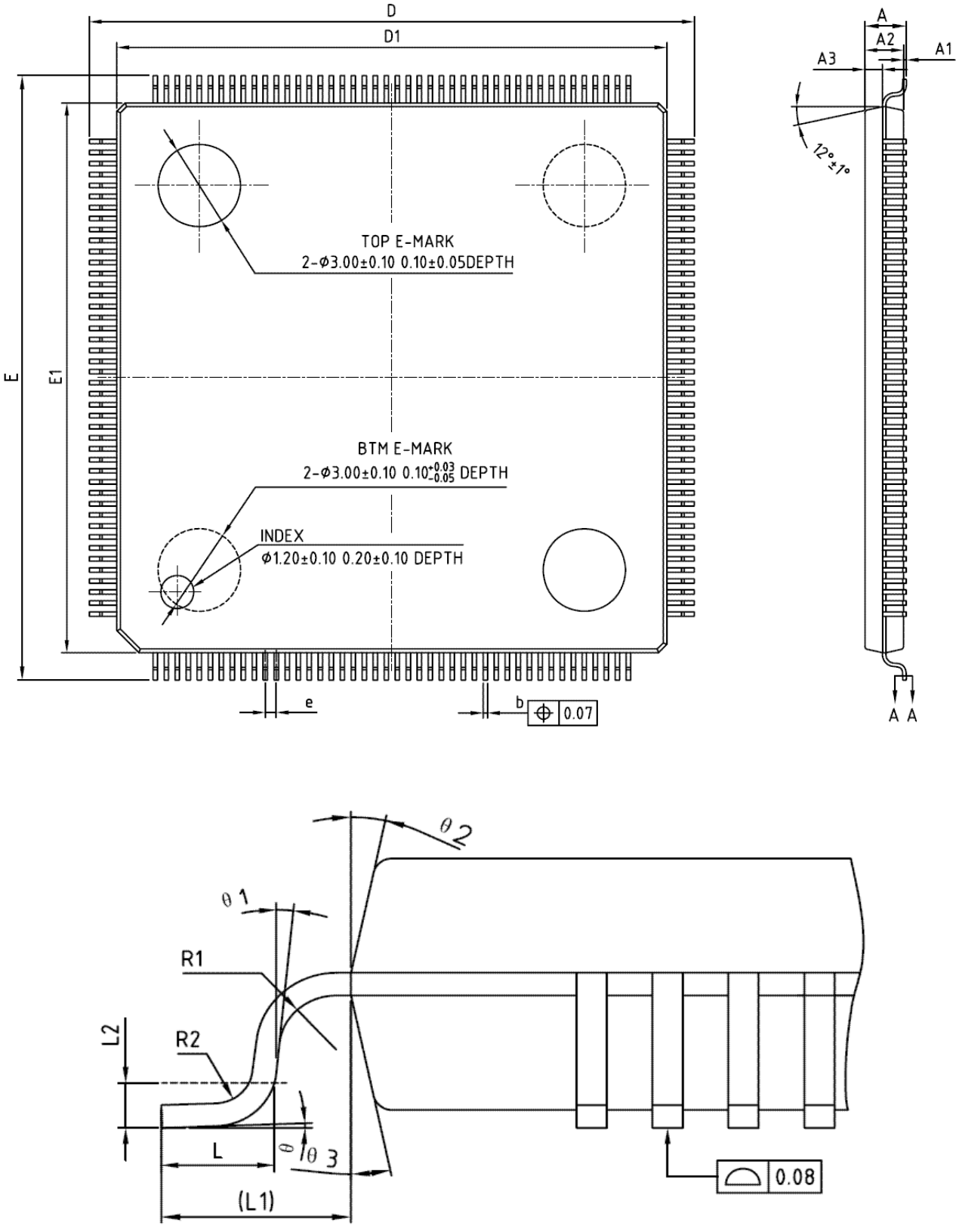
2 Packaging and Pinout Information

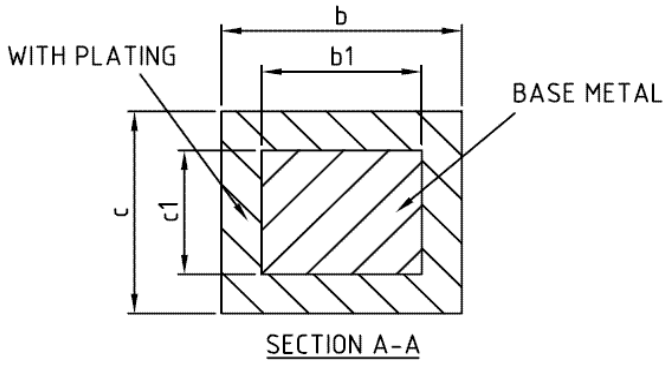
2.1 Overview

JZ4755A's package is LQFP176, which is 20mm x 20mm x 1.4mm outline, 0.4mm pitch, show in "2.2 JZ4755A Package".

The detailed pin description is listed in Table 2-1 ~ Table 2-16.

2.2 JZ4755A Package





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.23
b1	0.13	0.16	0.19
c	0.127	—	0.18
c1	0.119	0.127	0.135
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	—	—
R2	0.08	—	—
θ	0°	—	7°
θ 1	0°	—	—
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BFC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

2.3 Pin Description [1][2]

2.3.1 Pin for parallel interfaces

Table 2-1 EMC SDRAM Pins (39; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	6	12mA, pullup-pe	D0: SDRAM data bus bit 0, NAND/NOR/SRAM data bus bit 0 PA0: GPIO group A bit 0	VDDIO
D1 PA1	IO IO	7	12mA, pullup-pe	D1: SDRAM data bus bit 1, NAND/NOR/SRAM data bus bit 1 PA1: GPIO group A bit 1	VDDIO
D2 PA2	IO IO	8	12mA, pullup-pe	D2: SDRAM data bus bit 2, NAND/NOR/SRAM data bus bit 2 PA2: GPIO group A bit 2	VDDIO
D3 PA3	IO IO	9	12mA, pullup-pe	D3: SDRAM data bus bit 3, NAND/NOR/SRAM data bus bit 3 PA3: GPIO group A bit 3	VDDIO
D4 PA4	IO IO	10	12mA, pullup-pe	D4: SDRAM data bus bit 4, NAND/NOR/SRAM data bus bit 4 PA4: GPIO group A bit 4	VDDIO
D5 PA5	IO IO	11	12mA, pullup-pe	D5: SDRAM data bus bit 5, NAND/NOR/SRAM data bus bit 5 PA5: GPIO group A bit 5	VDDIO
D6 PA6	IO IO	12	12mA, pullup-pe	D6: SDRAM data bus bit 6, NAND/NOR/SRAM data bus bit 6 PA6: GPIO group A bit 6	VDDIO
D7 PA7	IO IO	13	12mA, pullup-pe	D7: SDRAM data bus bit 7, NAND/NOR/SRAM data bus bit 7 PA7: GPIO group A bit 7	VDDIO
D8 PA8	IO IO	172	12mA, pullup-pe	D8: SDRAM data bus bit 8, NAND/NOR/SRAM data bus bit 8 PA8: GPIO group A bit 8	VDDIO
D9 PA9	IO IO	173	12mA, pullup-pe	D9: SDRAM data bus bit 9, NAND/NOR/SRAM data bus bit 9 PA9: GPIO group A bit 9	VDDIO
D10 PA10	IO IO	174	12mA, pullup-pe	D10: SDRAM data bus bit 10, NAND/NOR/SRAM data bus bit 10 PA10: GPIO group A bit 10	VDDIO
D11 PA11	IO IO	175	12mA, pullup-pe	D11: SDRAM data bus bit 11, NAND/NOR/SRAM data bus bit 11 PA11: GPIO group A bit 11	VDDIO
D12 PA12	IO IO	176	12mA, pullup-pe	D12: SDRAM data bus bit 12, NAND/NOR/SRAM data bus bit 12 PA12: GPIO group A bit 12	VDDIO
D13 PA13	IO IO	1	12mA, pullup-pe	D13: SDRAM data bus bit 13, NAND/NOR/SRAM data bus bit 13 PA13: GPIO group A bit 13	VDDIO
D14 PA14	IO IO	2	12mA, pullup-pe	D14: SDRAM data bus bit 14, NAND/NOR/SRAM data bus bit 14 PA14: GPIO group A bit 14	VDDIO
D15 PA15	IO IO	3	12mA, pullup-pe	D15: SDRAM data bus bit 15, NAND/NOR/SRAM data bus bit 15 PA15: GPIO group A bit 15	VDDIO
A0 PB0	O IO	151	12mA, pullup-pe	A0: SDRAM address bus bit 0, NOR/SRAM address bus bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	150	12mA, pullup-pe	A1: SDRAM address bus bit 1, NOR/SRAM address bus bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	149	12mA, pullup-pe	A2: SDRAM address bus bit 2, NOR/SRAM address bus bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	148	12mA, pullup-pe	A3: SDRAM address bus bit 3, NOR/SRAM address bus bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	170	12mA, pullup-pe	A4: SDRAM address bus bit 4, NOR/SRAM address bus bit 4 PB4: GPIO group B bit 4	VDDIO
A5 PB5	O IO	169	12mA, pullup-pe	A5: SDRAM address bus bit 5, NOR/SRAM address bus bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	168	12mA, pullup-pe	A6: SDRAM address bus bit 6, NOR/SRAM address bus bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	167	12mA, pullup-pe	A7: SDRAM address bus bit 7, NOR/SRAM address bus bit 7 PB7: GPIO group B bit 7	VDDIO
A8 PB8	O IO	166	12mA, pullup-pe	A8: SDRAM address bus bit 8, NOR/SRAM address bus bit 8 PB8: GPIO group B bit 8	VDDIO

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
A9 PB9	O IO	165	12mA, pullup-pe	A9: SDRAM address bus bit 9, NOR/SRAM address bus bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	152	12mA, pullup-pe	A10: SDRAM address bus bit 10, NOR/SRAM address bus bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	164	12mA, pullup-pe	A11: SDRAM address bus bit 11, NOR/SRAM address bus bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	163	12mA, pullup-pe	A12: SDRAM address bus bit 12, NOR/SRAM address bus bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	154	12mA, pullup-pe	A13: SDRAM address bus bit 13, NOR/SRAM address bus bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	153	12mA, pullup-pe	A14: SDRAM address bus bit 14, NOR/SRAM address bus bit 14 PB14: GPIO group B bit 14	VDDIO
DCS0_ PB16	O IO	155	8mA, pullup-pe	DCS0_: SDRAM chip select 0 PB16: GPIO group B bit 16	VDDIO
RAS_ PB17	O IO	156	8mA, pullup-pe	RAS_: SDRAM row address strobe PB17: GPIO group B bit 17	VDDIO
CAS_ PB18	O IO	157	8mA, pullup-pe	CAS_: SDRAM column address strobe PB18: GPIO group B bit 18	VDDIO
SDWE_ & BUFD_ PB19	O IO	158	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB19: GPIO group B bit 19	VDDIO
WE0_ PB20	O IO	5	8mA, pullup-pe	WE0_: SDRAM/NOR/SRAM byte 0 write enable PB20: GPIO group B bit 20	VDDIO
WE1_ PB21	O IO	171	8mA, pullup-pe	WE1_: SDRAM/NOR/SRAM byte 1 write enable PB21: GPIO group B bit 21	VDDIO
CKO PB24	O IO	159	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CKE PB25	O IO	162	8mA, pullup-pe	CKE: SDRAM clock enable PB25: GPIO group B bit 25	VDDIO

Table 2-2 EMC Static Memory, MSC 0 and TSSI data Pins (9; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
A15/CL MSC0_CLK PB15	O O IO	15	2mA, pullup-pe	A15/CL: NOR/SRAM address bit 15, used as NAND flash command latch MSC0_CLK: MSC (MMC/SD) 0 clock output PB15: GPIO group B bit 15	VDDIO
A16/AL MSC0_CMD PC16	O IO IO	14	2mA, pullup-pe	A16/AL: NOR/SRAM address bit 16, used as NAND flash address latch MSC0_CMD: MSC (MMC/SD) 0 command PC16: GPIO group C bit 16	VDDIO
A17 MSC0_D3 PC17	O IO IO	17	2mA, pullup-pe	A17: NOR/SRAM address bit 17, used as NAND CS2_ MSC0_D3: MSC (MMC/SD) 0 data bit 3 PC17: GPIO group C bit 17	VDDIO
CS1_ PC21	O IO	20	2mA, pullup-pe	CS1_: NAND/NOR/SRAM chip select 1 PC21: GPIO group C bit 21	VDDIO
CS3_ PC23	O IO	145	4mA, pullup-pe	CS3_: NAND/NOR/SRAM chip select 3 PC23: GPIO group C bit 23	VDDIO
CS4_ PC24	O IO	143	4mA, pullup-pe	CS4_: NAND/NOR/SRAM chip select 4 PC24: GPIO group C bit 24	VDDIO
PC27/FRB MSC0_D2	IO IO	19	2mA, pullup-pe	PC27/FRB: GPIO group C bit 27, used for NAND FRB (ready/busy) MSC0_D2: MSC (MMC/SD) 0 data bit 2	VDDIO
FRE_ MSC0_D0 PC28	O IO IO	18	2mA, pullup-pe	FRE_: NAND read enable MSC0_D0: MSC (MMC/SD) 0 data bit 0 PC28: GPIO group C bit 28	VDDIO

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
FWE_ MSC0_D1 PC29	O IO IO	16	2mA, pullup-pe	FWE_: NAND write enable MSC0_D1: MSC (MMC/SD) 0 data bit 1 PC29: GPIO group C bit 29	VDDIO

Table 2-3 LCDC Pins (28; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
LCD_B0 PD26	O IO	96	4mA, pullup-pe	LCD_B0: LCD blue data bit 0 PD26: GPIO group D bit 26	VDDIO
LCD_REV LCD_B1 PD25	O O IO	99	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT LCD_B1: Blue data bit 1, used in 24-bit data bus PD25: GPIO group D bit 25	VDDIO
LCD_B2 PD0	O IO	123	4mA, pullup-pe	LCD_B2: LCD blue data bit 2 PD0: GPIO group D bit 0	VDDIO
LCD_B3 PD1	O IO	122	4mA, pullup-pe	LCD_B3: LCD blue data bit 3 PD1: GPIO group D bit 1	VDDIO
LCD_B4 PD2	O IO	121	4mA, pullup-pe	LCD_B4: LCD blue data bit 4 PD2: GPIO group D bit 2	VDDIO
LCD_B5 PD3	O IO	120	4mA, pullup-pe	LCD_B5: LCD blue data bit 5 PD3: GPIO group D bit 3	VDDIO
LCD_B6 PD4	O IO	119	4mA, pullup-pe	LCD_B6: LCD blue data bit 6 PD4: GPIO group D bit 4	VDDIO
LCD_B7 PD5	O IO	118	4mA, pullup-pe	LCD_B7: LCD blue data bit 7 PD5: GPIO group D bit 5	VDDIO
LCD_SPL LCD_G0 PD23	O O IO	97	4mA, pullup-pe	LCD_SPL: LCD SPL output LCD_G0: Green data bit 0, used in 24-bit data bus PD23: GPIO group D bit 23	VDDIO
LCD_PS LCD_G1 PD24	O O IO	100	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT LCD_G1: Green data bit 1, used in 24-bit data bus PD24: GPIO group D bit 24	VDDIO
LCD_G2 PD6	O IO	117	4mA, pullup-pe	LCD_G2: LCD green data bit 2 PD6: GPIO group D bit 6	VDDIO
LCD_G3 PD7	O IO	116	4mA, pullup-pe	LCD_G3: LCD green data bit 3 PD7: GPIO group D bit 7	VDDIO
LCD_G4 PD8	O IO	115	4mA, pullup-pe	LCD_G4: LCD green data bit 4 PD8: GPIO group D bit 8	VDDIO
LCD_G5 PD9	O IO	114	4mA, pullup-pe	LCD_G5: LCD green data bit 5 PD9: GPIO group D bit 9	VDDIO
LCD_G6 PD10	O IO	113	4mA, pullup-pe	LCD_G6: LCD green data bit 6 PD10: GPIO group D bit 10	VDDIO
LCD_G7 PD11	O IO	112	4mA, pullup-pe	LCD_G7: LCD green data bit 7 PD11: GPIO group D bit 11	VDDIO
LCD_R0 PD27	O IO	95	4mA, pullup-pe	LCD_R0: LCD red data bit 0 PD27: GPIO group D bit 27	VDDIO
LCD_CLS LCD_R1 PD22	O O IO	98	4mA, pullup-pe	LCD_CLS: LCD CLS output LCD_R1: Red data bit 1, used in 24-bit data bus PD22: GPIO group D bit 22	VDDIO
LCD_R2 PD12	O IO	111	4mA, pullup-pe	LCD_R2: LCD red data bit 2 PD12: GPIO group D bit 12	VDDIO
LCD_R3 PD13	O IO	110	4mA, pullup-pe	LCD_R3: LCD red data bit 3 PD13: GPIO group D bit 13	VDDIO
LCD_R4 PD14	O IO	109	4mA, pullup-pe	LCD_R4: LCD red data bit 4 PD14: GPIO group D bit 14	VDDIO
LCD_R5 PD15	O IO	108	4mA, pullup-pe	LCD_R5: LCD red data bit 5 PD15: GPIO group D bit 15	VDDIO

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
LCD_R6 PD16	O IO	107	4mA, pullup-pe	LCD_R6: LCD red data bit 6 PD16: GPIO group D bit 16	VDDIO
LCD_R7 PD17	O IO	106	4mA, pullup-pe	LCD_R7: LCD red data bit 7 PD17: GPIO group D bit 17	VDDIO
LCD_PCLK PD18	IO IO	124	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PD18: GPIO group D bit 18	VDDIO
LCD_HSYN PD19	IO IO	102	4mA, pullup-pe	LCD_HSYN: LCD line clock/horizontal sync PD19: GPIO group D bit 19	VDDIO
LCD_VSYN PD20	IO IO	101	4mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PD20: GPIO group D bit 20	VDDIO
LCD_DE PD21	O IO	103	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PD21: GPIO group D bit 21	VDDIO

Table 2-4 CIM and TSSI Pins (12; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
CIM_D0 TSDI0 PE0	I I IO	24	2mA, pullup-pe	CIM_D0: CIM data input bit 0 TSDI0: TS slave interface input data bus PE0: GPIO group E bit 0	VDDIO
CIM_D1 TSDI1 PE1	I I IO	25	2mA, pullup-pe	CIM_D1: CIM data input bit 1 TSDI1: TS slave interface input data bus PE1: GPIO group E bit 1	VDDIO
CIM_D2 TSDI2 PE2	I I IO	26	2mA, pullup-pe	CIM_D2: CIM data input bit 2 TSDI2: TS slave interface input data bus PE2: GPIO group E bit 2	VDDIO
CIM_D3 TSDI3 PE3	I I IO	27	2mA, pullup-pe	CIM_D3: CIM data input bit 3 TSDI3: TS slave interface input data bus PE3: GPIO group E bit 3	VDDIO
CIM_D4 TSDI4 PE4	I I IO	29	2mA, pullup-pe	CIM_D4: CIM data input bit 4 TSDI4: TS slave interface input data bus PE4: GPIO group E bit 4	VDDIO
CIM_D5 TSDI5 PE5	I I IO	30	2mA, pullup-pe	CIM_D5: CIM data input bit 5 TSDI5: TS slave interface input data bus PE5: GPIO group E bit 5	VDDIO
CIM_D6 TSDI6 PE6	I I IO	31	2mA, pullup-pe	CIM_D6: CIM data input bit 6 TSDI6: TS slave interface input data bus PE6: GPIO group E bit 6	VDDIO
CIM_D7 TSDI7 PE7	I I IO	32	2mA, pullup-pe	CIM_D7: CIM data input bit 7 TSDI7: TS slave interface input data bus PE7: GPIO group E bit 7	VDDIO
CIM_MCLK TSFAIL PE8	O	37	4mA, pullup-pe	CIM_MCLK: CIM master clock output TSFAIL: TS interface error package indicator input PE8: GPIO group E bit 8	VDDIO
CIM_PCLK TSCLK PE9	I I IO	34	2mA, pullup-pe	CIM_PCLK: CIM pixel clock input TSCLK: TS interface clock input PE9: GPIO group E bit 9	VDDIO
CIM_VSYN TSSTR PE10	I I IO	35	2mA, pullup-pe	CIM_VSYN: CIM VSYNC input TSSTR: TS interface frame start input PE10: GPIO group E bit 10	VDDIO
CIM_HSYN TSFRM PE11	I I IO	36	2mA, pullup-pe	CIM_HSYN: CIM HSYNC input TSFRM: TS interface frame valid input PE11: GPIO group E bit 11	VDDIO

2.3.2 Pin for serial interfaces

Table 2-5 SSI/MSC1 Pins (6; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
SSI_CLK MSC1_CLK PB26	O O IO	42	4mA, pullup-pe	SSI_CLK: SSI clock output MSC1_CLK: MSC (MMC/SD) 1 clock output PB26: GPIO group B bit 26	VDDIO
SSI_DT MSC1_D1 PB27	O IO IO	40	4mA, pullup-pe	SSI_DT: SSI data output MSC1_D1: MSC (MMC/SD) 1 data bit 1 PB27: GPIO group B bit 27	
SSI_DR MSC1_D0 PB28	I IO IO	41	4mA, pullup-pe	SSI_DR: SSI data input MSC1_D0: MSC (MMC/SD) 1 data bit 0 PB28: GPIO group B bit 28	
SSI_CE0_ MSC1_CMD PB29	O O IO	43	4mA, pullup-pe	SSI_CE0_: SSI chip enable 0 MSC1_CMD: MSC (MMC/SD) 1 command PB29: GPIO group B bit 29	
SSI_GPC MSC1_D2 PB30	O IO IO	44	4mA, pullup-pe	SSI_GPC: SSI general-purpose control signal MSC1_D2: MSC (MMC/SD) 1 data bit 2 PB30: GPIO group B bit 30	
SSI_CE1_ MSC1_D3 PB31	O IO IO	45	4mA, pullup-pe	SSI_CE1_: SSI chip enable 1 MSC1_D3: MSC (MMC/SD) 1 data bit 3 PB31: GPIO group B bit 31	

Table 2-6 SSI Pins (3; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
SSI_CLK PF10	O IO	92	4mA, pullup-pe	SSI_CLK: SSI clock output PF10: GPIO group F bit 10	VDDIO
SSI_DT PWM1 PF11	O O IO	90	4mA, pullup-pe	SSI_DT: SSI data output PWM1: PWM 1 output. It can run in sleep mode in RTCLK clock PF11: GPIO group F bit 11	
SSI_DR PF12	I IO	91	4mA, pullup-pe	SSI_DR: SSI data input PF12: GPIO group F bit 12	

Table 2-7 I2C Pins (2; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
I2C_SDA PE12	IO IO	39	4mA, pullup-pe	I2C_SDA: I2C serial data PE12: GPIO group E bit 12	VDDIO
I2C_SCK PE13	IO IO	38	4mA, pullup-pe	I2C_SCK: I2C serial clock PE13: GPIO group E bit 13	VDDIO

Table 2-8 UART 1, AIC and TCU/PWM Pins (5; all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
SDATO PE18	I IO	89	2mA, pullup-pe	SDATO: AC97/I2S serial data output PE18: GPIO group E bit 18	VDDIO
SDATI PE19	O IO	88	2mA, pullup-pe	SDATI: AC97/I2S serial data input PE19: GPIO group E bit 19	VDDIO
PWM2 SYNC	O IO	23	2mA, pullup-pe	PWM2: PWM 2 output. It can run in sleep mode in RTCLK clock SYNC: AC97 frame SYNC or I2S Left/Right	VDDIO

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
PE22	IO			PE22: GPIO group E bit 22	
PWM3 UART1_RxD BCLK PE23	O I IO IO	28	2mA, pullup-pe	PWM3: PWM 3 output UART1_RxD: UART 1 Receiving data BCLK: AC97/I2S bit clock PE23: GPIO group E bit 23	VDDIO
PWM5 UART1_TxD SCLK_RSTN PE25	O O O IO	33	2mA, pullup-pe	PWM5: PWM 7 output UART1_TxD: UART 1 transmitting data SCLK_RSTN: I2S system clock output or AC97 reset output PE25: GPIO group E bit 25. This pin is used for KEY_INT and to indicate USB boot	VDDIO

2.3.3 Pin for system

Table 2-9 System Pins (1, all GPIO shared)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
BOOT_SEL1 PC31	I IO	93	2mA, Schmitt, pullup-pe	BOOT_SEL1: Boot select bit 1 PC31: GPIO group C bit 31	VDDIO

2.3.4 Pin for analog interfaces and corresponding power/ground

Table 2-10 Audio CODEC Pins (11)

Pin Names	IO	Pin Location	Pin Description	Power
AOHPL	AO	87	AOHPL: Left headphone out	AVD_{CDC}
AOHPR	AO	83	AOHPR: Right headphone out	AVD_{CDC}
AOHPM	AIO	85	AOHPM: Headphone common mode output and sense input. In capacitor-less mode, the headphone left channel and right channel ground should be connected to this pin. Please make the trace between this pin and the headphone jack as short as possible.	AVD_{CDC}
MICP1	AI	79	MICP1: Microphone 1 input or input positive	AVD_{CDC}
LLINEIN	AI	78	LLINEIN: Left line input (AIL1)	AVD_{CDC}
RLINEIN	AI	77	RLINEIN: Right line input (AIR1)	AVD_{CDC}
VCOM	AO	80	VCOM: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise?	AVD_{CDC}
AVDHP	P	86	AVDHP: Headphone amplifier power, 3.3V (VDDAO, double PAD)	-
AVSHP	P	84	AVSHP: Headphone amplifier ground (VSSAO, double PAD)	-
AVDCDC	P	82	AVDCDC: CODEC analog power, 3.3V (VDDA + VREFP)	-
AVSCDC	P	81	AVSCDC: CODEC analog ground (VSSA + VREFN)	-

Table 2-11 USB device 2.0 Pins (6)

Pin Names	IO	Pin Location	Pin Description	Power
DP0	AIO	66	DP0: USB 2.0 device data plus	AVD_{USB}
DM0	AIO	67	DM0: USB 2.0 device data minus	AVD_{USB}
RREF	AIO	69	RREF: External Reference for USB 2.0 device. Connect a 10kΩ external reference	AVD_{USB}

Pin Names	IO	Pin Location	Pin Description	Power
			resistor, with 1% tolerance to analog ground AVSUSB	
VDDA	AIO	70	VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground AVSUSB	AVD_{USB}
AVDUSB	P	68	AVDUSB: USB analog power, 3.3V	-
AVSUSB	P	65	AVSUSB: USB analog ground	-

Table 2-12 SAR ADC Pins (7)

Pin Names	IO	Pin Location	Pin Description	Power
XP	AI	61	XP: Touch screen X+ input	AVD_{AD}
XN	AI	58	XN: Touch screen X- input	AVD_{AD}
YP	AI	60	YP: Touch screen Y+ input	AVD_{AD}
YN	AI	59	YN: Touch screen Y- input	AVD_{AD}
PBAT/ADIN0	AI	64	ADIN0: Battery voltage input or ADC general purpose input 0	AVD_{AD}
ADIN1	AI	63	ADIN1: ADC general purpose input 1	AVD_{AD}
AVDAD	P	62	AVDAD: ADC analog power, 3.3 V	-

Table 2-13 Video DAC Pins (7)

Pin Names	IO	Pin Location	Pin Description	Power
LUMA	AO	52	LUMA: DAC analog output for CVBS or luminance of S-Video	AVD_{DA}
CHROMA_U	AO	54	CHROMA_U: DAC analog output Chrominance of S-Video or component U	AVD_{DA}
V	AO	55	V: DAC analog output of component V	AVD_{DA}
AVDDA	P	53	AVDDA: Power supply for LUMA and CHROMA output, 3.3 V (IO1:AVD33R, IO2:AVD33G, IO3:AVDD, VDWELL)	-
AVSDA	P	49	AVSDA: Ground for LUMA and CHROMA output (IO1/IO2: AVS33R, AVS33G, AVSS, VSSUB)	-
REXT	AO	50	REXT: For external resistor. REXT(ohm)=VREFIN(V)*7.31 /IOFS(A)	
COMP	AIO	51	COMP: Compensation pin. This pin should be connected with 0.01uf ceramic cap parallel with a 10uf tantalum cap to AVDDAO externally	

Table 2-14 CPM Pins (4)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
EXCLK	AI	46	10~30 MHz Oscillator, OSC on/off	EXCLK: 24MHz OSC input or 24MHz clock input	VDDIO
EXCLKO	AO	47		EXCLKO: OSC output	VDDIO
VDDPLL	P	57		VDDPLL: PLL analog power, 1.8V	-
VSSPLL	P	56		VSSPLL: PLL analog ground	-

Table 2-15 RTC Pins (6, 1 with GPIO input: PE30)

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
RTCLK	AI	71	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	72		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}

Pin Names	IO	Pin Location	IO Cell Char.	Pin Description	Power
PWRON	AO	76	~2mA	PWRON: Power on/off control of main power, high active	VDD_{RTC}
WKUP_ PE30	AI AI	75	Schmitt	WKUP_: Wakeup signal after main power down PE30: GPIO group E bit 30, input/interrupt only	VDD_{RTC}
PPRST_	AI	74	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	73		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

2.3.5 Pin for IO and core power/ground

Table 2-16 IO/Core power supplies (12)

Pin Names	IO	Pin Location	Pin Description	Power
VDDIO	P	4 48 94 146	VDDIO: IO digital power, 3.3V	-
VSS	P	21 105 144 160	VSS: IO and CORE digital ground	-
VDDCORE	P	22 104 142 161	VDDCORE: CORE digital power, 1.8V	-

2.3.6 Pin not connected

Table 2-17 Not connected Pins (18)

Pin Names	IO	Pin Location	Pin Description	Power
NC	-	134 135 136 137 138 139 140 141 125 126 127 128 129 130 131 132 147 133	NC: not connected pins	-

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12Ma.
   b Pull-up: The IO cell contains a pull-up resistor.
   c Pull-down: The IO cell contains a pull-down resistor.
   d Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   e Schmitt: The IO cell is Schmitt trig input.

2 For any GPIO shared pin except CKO/PB24, the reset state is GPIO input with internal pull-up. The CKO/PB24 is initialed to CKO functions with internal pull-up.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
AVDUSB power supplies voltage	-0.3	3.9	V
AVDCDC power supplies voltage	-0.3	4.0	V
AVDHP power supplies voltage	-0.3	4.0	V
AVDAD power supplies voltage	-0.3	4.0	V
AVDDA power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to AVDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to AVDAD supplied non-supply pins except PBAT	-0.5	4.0	V
Input voltage to AVDDA supplied non-supply pins	-0.5	4.0	V
Input voltage of PBAT	-0.5	6.0	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from AVDAD supplied non-supply pins	-0.5	4.0	V
Output voltage from AVDDA supplied non-supply pins	-0.5	4.0	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{USB}	AVDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	AVDCDC voltage	3.0	3.3	3.6	V
V_{HP}	AVDHP voltage	3.0	3.3	3.6	V
V_{ADC}	AVDAD voltage	3.0	3.3	3.6	V
V_{DAC}	AVDDA voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-IO}	Input high voltage	2.0		3.6	V
V_{IL-IO}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-UF}	Input voltage range for full speed applications	0		V_{USB}	V
V_{I-UH}	Input voltage range for high speed applications	120		400	mV

Table 3-5 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{I-PBAT1}$	PBAT input voltage range when measuring low voltage battery	0		2.5	V
$V_{I-PBAT2}$	PBAT input voltage range when measuring high voltage battery	0		5	V
$V_{I-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V
V_{I-TSC}	XN/XP/YN/YP input voltage range	0		V_{ADC}	

Table 3-6 Recommended operating conditions for AVDCDC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
$V_{ILH-CDC}$	Input voltage range	0		V_{CDC}	V

Table 3-7 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-RTC}	Input high voltage	2.0		3.6	V
V_{IL-RTC}	Input low voltage	-0.3		0.8	V

Table 3-8 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-9 DC characteristics for VDDIO supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point		1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point		0.88	0.94	0.99	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		50	65	100	kΩ
R_{PD}	Pull-down Resistor		40	56	107	kΩ
C_{IO}	Capacitance of the pins		4	5	10	pF
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.4V for cells of	2mA	2.2	3.7	4.6	mA
		4mA	4.4	7.4	9.2	mA
		8mA	8.9	14.7	18.4	mA
		12mA	13.3	22.1	27.5	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = 2.4V for cells of	2mA	2.5	5.1	7.9	mA
		4mA	5.0	10.2	15.9	mA
		8mA	10.0	20.4	31.7	mA
		12mA	15.0	30.6	47.6	mA

Table 3-10 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-U20}	Output high voltage	1.5		V_{USB}	V
V_{OL-U20}	Output low voltage	0		0.4	V

Table 3-11 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-ADC}	XN/XP/YN/YP output high voltage	0.9 * V_{ADC}		V_{ADC}	V
V_{OL-ADC}	XN/XP/YN/YP output low voltage	0		0.1 * V_{ADC}	V
R_{BAT}	BAT input resister		9.3		kΩ
R_{PDADC}	Internal pull down resister		10.4		kΩ

Table 3-12 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH-RTC}	Output high voltage	2.0		3.6	V
V_{OL-RTC}	Output low voltage	-0.3		0.8	V

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4755A processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-13.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1 VDDRTC

2 VDDA: AVDCDC, AVDHP

3 All other 3.3V VDDs (VDD33): VDDIO, AVDAD, AVDDA, AVDUSB

4 All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

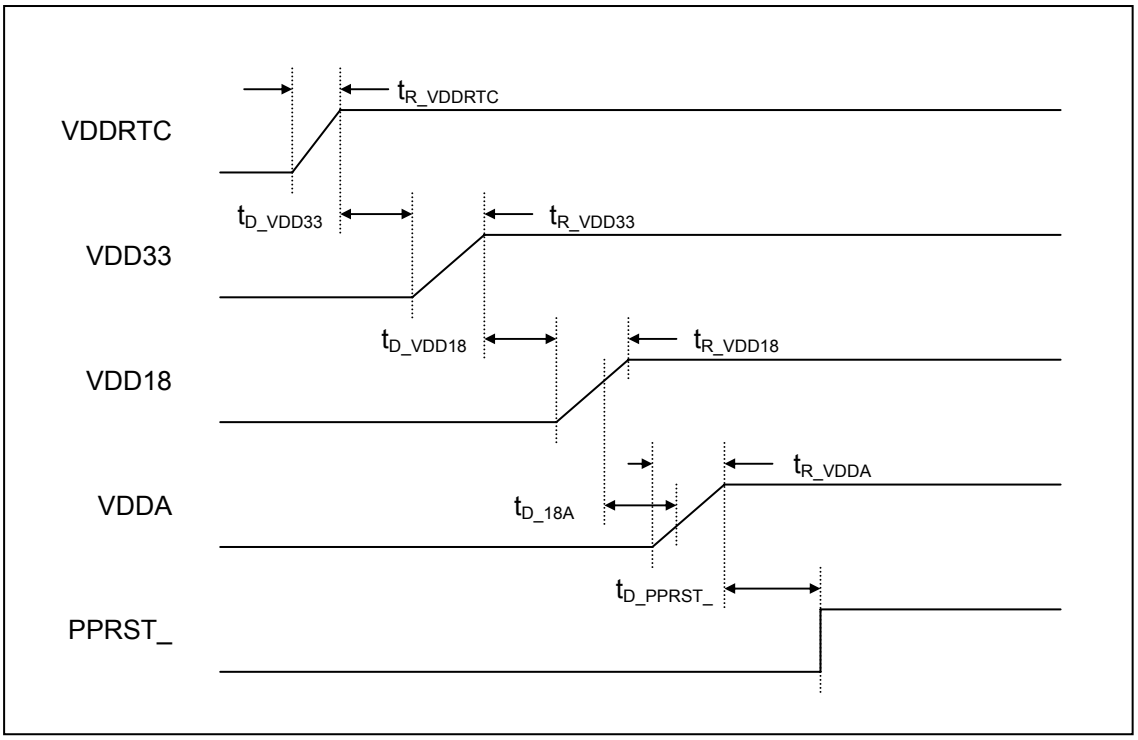


Figure 3-1 Power-On Timing Diagram

Table 3-13 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33 applies	$-t_{R\_VDDRTC}$	–	–	ms[1]
t_{R_VDD33}	VDD33 rise/stabilization time	0	–	100	ms
t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	$-t_{R\_VDD33}/2$	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0	–	100	ms
t_{D_18A}	Delay between VDD18 (actually VDDcore) arriving 1.5V and VDDA arriving 1V	0.01	–	10	ms
t_{R_VDDA}	VDDA rise/stabilization time	0	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDDA stable and PPRST_ deasserted	0.1	–	–	ms

NOTES:

1 VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.

2 VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.4.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except CKO pin, are put to GPIO input function with the internal pull-up set to on. The CKO pin is set to CKO function with the internal pull-up set to on. The PWRON is output 0. The 32768Hz/24MHz oscillators are on. The USB 2.0 PHY, the CODEC DAC/ADC, the

SAR-ADCs and the video DAC are put in suspend mode.

3.4.3 BOOT

JZ4755A supports 3 different boot sources depending on BOOT_SEL1, PE25 and ADIN1 pins values. Table 3-14 lists them.

Table 3-14 Boot from 3 boot sources

BOOT_SEL1	Other Condition (PE25's internal pull up is disabled)	Boot From
1	PE25 is low or ADIN1 channel > 381	NAND flash
1	PE25 is high and ADIN1 channel <= 381	USB2.0 device @EXCLK=24MHz
0	PE25 is low or ADIN1 channel > 381	SD card: MSC0
0	PE25 is high and ADIN1 channel <= 381	USB2.0 device @EXCLK=24MHz