1 PMon

1.1 Overview

Pmon is a simple performance monitor. In JZ4750, following performance relative real-time events can be monitored.

- I-cache miss count
- D-cache miss count
- Total instruction count
- Useless instruction count
- Pipeline freeze count
- CPU clock count

1.2 Fundamental

When PMon is enabled (set value 1 to config7.bit8), one preset event pair determined by config7.bit15~bit12 will be continuously monitored until PMon is disabled (set value 0 to config7.bit8). Please refer to PMon registers' description for detail information of available event pairs in JZ4750.

1.3 Registers Descriptions

PMon Control and Status

PMON_CSR **CP0 Register 16, select 7**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																PEVENT				Reserved			PME	Reserved					ALLOC	BTBV	BTBE
Rst	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	0	0	0	0	?	?	?	0	?	?	?	?	?	0	0	0

Bits	Name	Description	R/W
31:16	Reserved	Write is ignored, read as zero	R
15:12	PEVENT	Event pair encoding 0: freeze count, cpu clock count; 1: icc-miss count, dcc-miss count 2: useless insn count, total insn count; 3~15: reserved	RW
11:9	Reserved	Write is ignored, read as zero	R
8	PME	Performance monitor enable. 0: disable, 1: enable	RW
7:3	Reserved	Write is ignored, read as zero	R
2	ALLOC	Allocate hint of PREF instruction. 0: enabled (default); 1: disabled	RW
1	BTBV	BTB invalid. Writing 1 to this bit to invalidates BTB; read as zero	W
0	BTBE	BTB enable. 0: enabled (default); 1: disabled	RW

Event Pair Count High

PMON_HIGH **CP0 Register 16, select 4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LH																RH															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:16	LH	High 16-bit of the count number for the left one of event pair	RW
15:0	RH	High 16-bit of the count number for the right one of event pair	RW

Event Pair Left Count

PMON_LC **CP0 Register 16, select 5**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LC																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	LC	Low 32-bit of the count number for the left one of event pair	RW

Event Pair Right Count

PMON_RC **CP0 Register 16, select 6**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RC																															
RST	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description	R/W
31:0	RC	Low 32-bit of the count number for the right one of event pair	RW