JZ4750

Mobile Application Processor

Data Sheet

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1 Overview

JZ4750 is a highly integrated SOC solution for multimedia rich and general embedded products like PMP, GPS navigator and smart phone.

At the heart of JZ4750 is XBurst processor engine. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption.

The SIMD instruction set implemented by XBurst core, in together with the on chip video accelerating engine and post processing unit, provides enhanced video decoding capability.

The memory interface of JZ4750 supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory and 4-bit/8-bit/12-bit MLC MLC NAND flash memory for cost sensitive applications.

On-chip modules such as LCD controller, audio CODEC, multi-channel SAR-ADC, AC97/I2S controller, PCM interface and camera interface offer designers a rich suite of peripherals for multimedia application. TV encoder unit and 2 channels 10-bits DACs provide composite/S-video TV signal output in PAL or NTSC format. WLAN, Bluetooth and expansion options are supported through the USB 1.1, high speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB 2.0 device, UART, SPI and general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

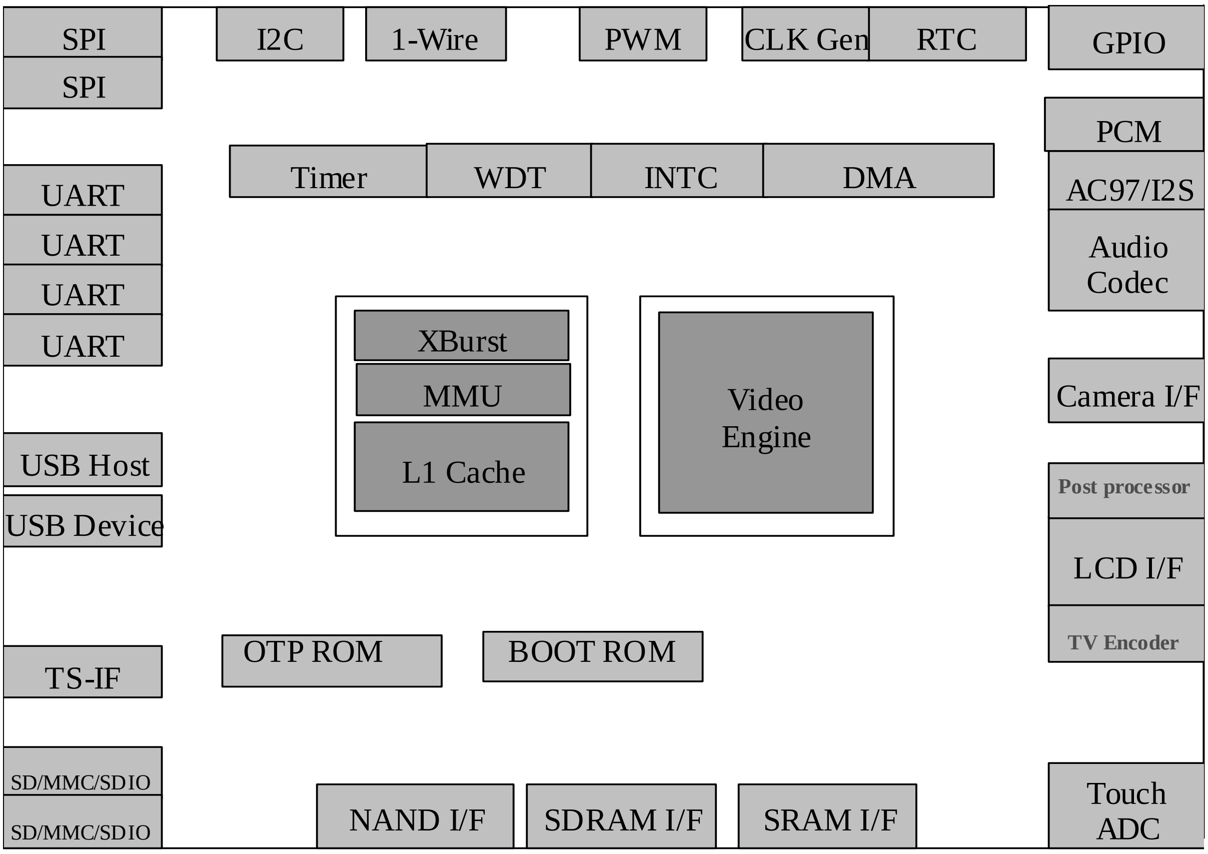


Figure 1-1 JZ4750 Diagram

1.2 Features

1.2.1 CPU Core

- XBurst CPU
  - XBurst® RISC instruction set to support Linux and WinCE
  - XBurst® SIMD instruction set to support multimedia acceleration
  - XBurst® 8-stage pipeline micro-architecture up to 360MHz
- MMU
  - 32-entry dual-pages joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- Cache
  - 16K instruction cache
  - 16K data cache
- 16KB tight coupled memory

1.2.2 Video Accelerator

- Motion compensation
- Motion estimation
- De-block
- DCT/IDCT for 4x4 block

1.2.3 Memory Sub-systems

- Static memory interface
  - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
  - Four chip-select pin for static memory, each can be configured separately
  - Support 8, 16 or 32 bits data width
  - The size and base address of static memory banks are programmable
- NAND flash interface
  - Support 4-bit/8-bit/12-bit MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM interface
  - Standard SDRAM and Mobile SDRAM
  - 1 banks with programmable size and base address
  - 32-bit and 16-bit data bus width
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode

- 2 Chip selects
- Can be pin shared or separated with/from NAND-static memory

- BCH Controller
  - Implement data ECC encoding and decoding
- Direct memory access controller
  - Twelve independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
  - External DMA supported
- OTP Module
  - Up to 8 independent fuse banks (32 bytes)
  - Data Retention : 10 Years @85°C
  - Standby Current < 1uA
- The JZ4750 processor system supports little endian only

1.2.4 AHB Bus Arbiter

- Provide a fair chance for each AHB master to possess the AHB bus
- Fulfill the back-to-back feature of AHB protocol
- Divide two master groups with different privileges supports two arbitrating methods: Round-robin possession for masters in the same group, Preemptive possession for masters with higher privileges

1.2.5 System Devices

- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 24MHz clock
  - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power

  - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
  - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output
  - Provide six separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Six PWM outputs
- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset

1.2.6 Audio/Display/UI Interfaces

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 24-bit data bus
  - Support 1,2,4,8 pins STN panel, 16bit, 18bit and 24bit TFT and 8bit I/F TFT
  - Display size up to 1280×1024 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)
  - Support delta RGB
  - One single color background and two foreground OSD
- TV encoder
  - Support NTSC or PAL
  - Support CVBS or S-video signals
  - 2 channel 10 bits DAC
- Image post processor
  - Video frame resize

- Color space conversion: 420/444/422 YUV to RGB convert
- Camera interface module
  - Input image size up to 4096×4096 pixels
  - Supports CCIR656 data format
  - Bayer RGB, YCbCr 4:2:2 and YCbCr 4:4:4 data format
  - 32×32 image data receive FIFO with DMA support
- On-chip audio CODEC
  - 24-bit DAC, SNR: 90dB
  - 24-bit ADC, SNR: 85dB
  - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
  - L/R channels line input
  - MIC input
  - L/R channels headphone output amplifier support up to 16ohm load
  - Capacitor-coupled or capacitor-less
- AC97/I2S controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the on-chip CODEC
  - Support off-chip CODEC
- PCM
  - Short frame sync, long frame sync and multi-slot modes supported
  - Slave and master operation modes
  - 8/16 bit sample size
  - DMA transfer
- SADC
  - 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
  - XP/XN, YP/YN inputs for touch screen
  - Battery voltage input
  - 1 generic input channel

1.2.7 On-chip Peripherals

- General-Purpose I/O ports
  - Total 179 GPIOs
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up

- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- Two synchronous serial interfaces
  - Up to 50MHz speed
  - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
  - Configurable 2 - 17 (or multiples of them) bits data transfer
  - Full-duplex/transmit-only/receive-only operation
  - Supports normal transfer mode or Interval transfer mode
  - Programmable transfer order: MSB first or LSB first
  - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
  - Programmable divider/prescaler for SSI clock
  - Back-to-back character transmission/reception mode
- One-wire bus interface
  - Overdrive and regular speed
  - Master only
  - LSB first
  - Bit or byte operate modes
- USB 1.1 host interface
  - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible
- USB 2.0 device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported
  - Embedded USB 2.0 PHY
- Two MMC/SD/SDIO controllers
  - One with 8-bit data bus and another with 4-bit data bus
  - Compliant with "The MultiMediaCard System Specification version 4.2"
  - Compliant with "SD Memory Card Specification version 2.0" and "SDIO Card Specification version 1.0" with 1 command channel and 4 data channels
  - Up to 320 Mbps data rate
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- Four UARTs
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 16x8bit FIFO for transmit and 16x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions
  - Support slow infrared asynchronous interface (IrDA)
  - IrDA function up to 115200bps baudrate

- UART function up to 921.6Kbps baudrate
- Hardware flow control
- Transport stream slave interface
  - 8-bit or 1-bit data bus selectable
  - Support PID filtering

1.2.8 Bootrom

- 8kB Boot ROM

1.3 Characteristic

Item	Characteristic
Process Technology	0.18um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	BGA256, 14mm x 14mm x 1.4mm, 0.8mm pitch
Operating frequency	360MHz

2 Packaging and Pinout Information

2.1 Overview

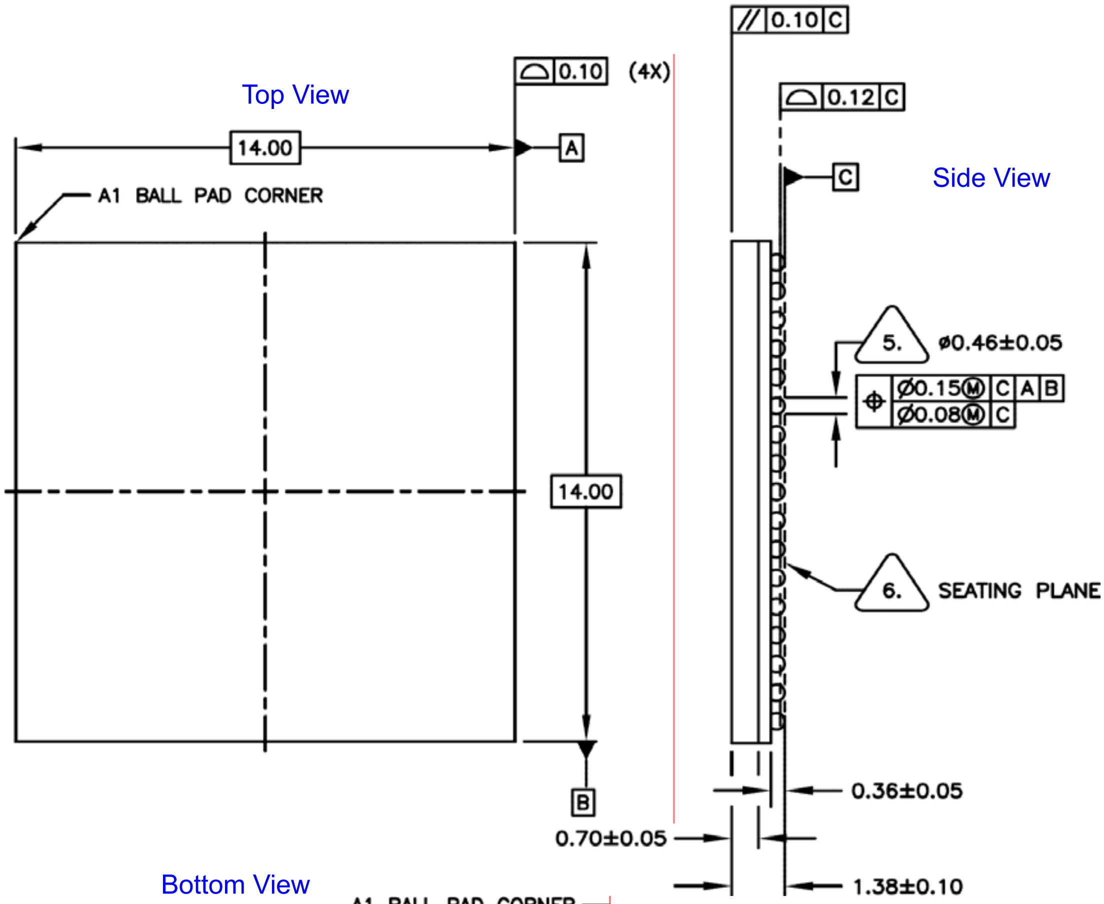
JZ4750 processor is offered in 256-pin LFBGA package, which is 14mm x 14mm x 1.4mm outline, 17 x 17 matrix ball grid array and 0.8mm pitch, show in Figure 2-1. The JZ4750 pin to ball assignment is show in Figure 2-2.

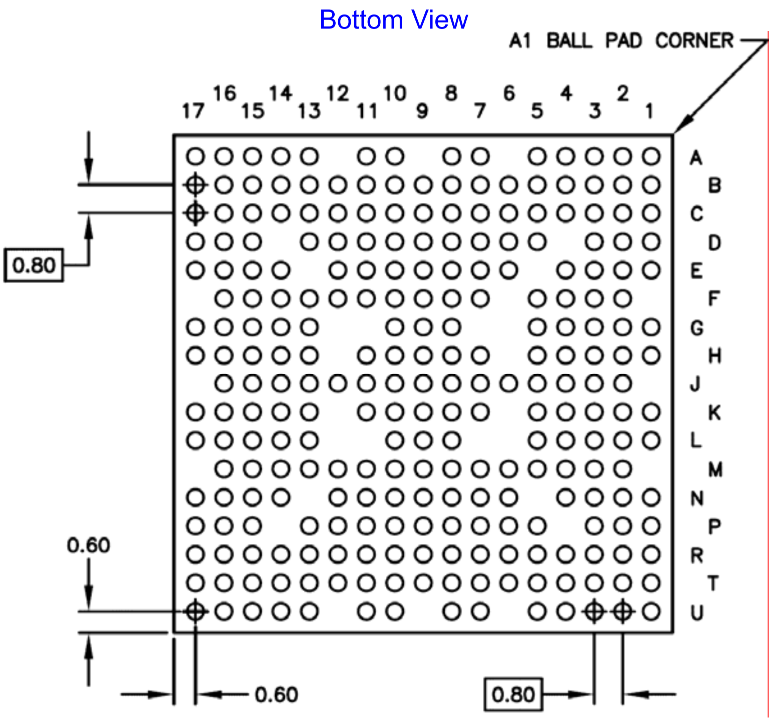
The detailed pin description is listed in Table 2-1 ~ Table 2-20.

2.2 Solder Process

JZ4750 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 JZ4750 Package





NOTES:

1. ⚠5 Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
2. ⚠6 Primary datum C and seating plane are defined by the spherical crowns of the solder balls
3. Package outline – 17 x 17 matrix, 14.00mm x 14.00mm x 1.38mm, 0.70mm mold cap, 0.46mm ball, 0.80mm pitch, laminate substrate

Figure 2-1 JZ4750 package outline drawing

JZ4750 Ball Assignment Rev1.3

BGA256, 14mm x 14mm x 1.4mm, 0.8pitch, Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	D15	D13	D11	D8	A6		CKO	A0		A9	D16		D22	D26	D28	D30	SD0_A20	A
B	D1	D14	D12	D9	A14	A4	A8	DCS1	A3	CKE	D19	D21	D23	WE3	D29	SD1_A21	SD2_A22	B
C	D3	D2	D0	D10	WE1	A2	A13	A12	A5	CAS	D17	D20	D25	D27	D31	SD3_A23	SD4_A24	C
D	D5	D4	WE0		MSC1_CMD	MSC1_D3	MSC1_D2	DCS0	A7	RAS	WE2	D18	D24		SD5_A25	SD6	SD7	D
E	D7	MSC1_CLK	D6	SSI1_DT		MSC1_D1	MSC1_D0	A10	A11	A1	SDWE	SA2_A19		SA1_A18	SA0_A17	FWE	FRE	E
F		SSI1_CLK	SSI1_CE0	SSI_CE1	SSI1_DR		VSSIO	VDDIO_L	VDDIO_L	VSSIO	A16_AL	A15_CL	FRB	WR	RD	CS4		F
G	LCD_SPL	UART3_RXD	UART3_TXD	UART3_CTS	UART3_RTS			VDDIO_L	VSSIO	VSS CORE			CS3	CS2	CS1	SD15_TSD7	SD14_TSD6	G
H	LCD_CLS	LCD_DE	LCD_D17	LCD_REV	LCD_PS		VDDIO_L	VSSIO	VDD CORE	VDD CORE	VSS CORE		SD13_TSD5	SD12_TSD4	SD11_TSD3	SD10_TSD2	SD9_TSD1	H
J		LCD_VSYN	LCD_D16	LCD_D15	LCD_D14	VSSIO	VDDIO_L	VSSIO	VSS CORE	VDD CORE	VSS CORE	VDD CORE	SD8_TSD0	TSFAIL	TSFRM	TSSTR		J
K	LCD_HSYN	LCD_PCLK	LCD_D13	LCD_D12	LCD_D11		VDDIO	VDDIO	VSS CORE	VDD CORE	VDD CORE		TSCLK	MSC0_CMD	MSC0_CLK	MSC0_D7	MSC0_D6	K
L	LC D_D10	LCD_D9	LCD_D8	LCD_D7	LCD_D6			VDDIO	VSSIO	VSS CORE			MSC0_D5	MSC0_D4	MSC0_D3	MSC0_D2	MSC0_D1	L
M		LCD_D5	LCD_D4	LCD_D3	LCD_D2	LCD_D1	LCD_D0	SSI0_CE0	SSI0_GPC	SSI0_CE1	UART2_RXD	UART2_TXD	MSC0_D0	PWM3	PWM4	PWM5		M
N	AVDDA	LUMA	AVSDA	TEST_TE		UART1_CTS	PWM0	PWM1	TDO	SSI0_DT	SSI0_DR	SSI0_CLK		PWM2	CIM_D7	CIM_D5	CIM_MCLK	N
P	COMP	CHROMA	BOOT_SEL0		UART1_RTS	XP	RREF	PWRON	TDI	TRST	AIL	AIR	TCK		CIM_D6	CIM_D4	CIM_PCLK	P
R	REXT	UART1_TXD	UART1_RXD	BOOT_SEL1	AVSAD	PBAT	AVDUSB	AVSUSB	VDDRTC	TMS	MICBIAS	MICP	AOHPM	AOHPMS	WAIT	CIM_D3	CIM_D2	R
T	I2C_SCK	EXCLK	VSSPLL	YN	XN	ADIN1	DP0	DP1	VDDA	RTCLK	WKUP	AVSCDC	AVSHP	AVDHP	AOHPR	CIM_D1	CIM_HSYN	T
U	I2C_SDA	EXCLKO	VDDPLL	YP	AVDAD		DM0	DM1		RTCLKO	PPRST		VCOM	AVDCDC	AOHPL	CIM_D0	CIM_VSYN	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2-2 JZ4750 pin to ball assignment

2.4 Pin Description [1][2]

2.4.1 Pin for parallel interfaces

Table 2-1 EMC SDRAM Pins (58; all GPIO shared: PA0~31, PB0~14,16~25, PE28)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	C3	12mA, pullup-pe	D0: SDRAM data bus bit 0, static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIOL
D1 PA1	IO IO	B1	12mA, pullup-pe	D1: SDRAM data bus bit 1, static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIOL
D2 PA2	IO IO	C2	12mA, pullup-pe	D2: SDRAM data bus bit 2, static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIOL
D3 PA3	IO IO	C1	12mA, pullup-pe	D3: SDRAM data bus bit 3, static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIOL
D4 PA4	IO IO	D2	12mA, pullup-pe	D4: SDRAM data bus bit 4, static memory data bus bit 4 PA4: GPIO group A bit 4	VDDIOL
D5 PA5	IO IO	D1	12mA, pullup-pe	D5: SDRAM data bus bit 5, static memory data bus bit 5 PA5: GPIO group A bit 5	VDDIOL
D6 PA6	IO IO	E3	12mA, pullup-pe	D6: SDRAM data bus bit 6, static memory data bus bit 6 PA6: GPIO group A bit 6	VDDIOL
D7 PA7	IO IO	E1	12mA, pullup-pe	D7: SDRAM data bus bit 7, static memory data bus bit 7 PA7: GPIO group A bit 7	VDDIOL
D8 PA8	IO IO	A4	8mA, pullup-pe	D8: SDRAM data bus bit 8, static memory data bus bit 8 PA8: GPIO group A bit 8	VDDIOL
D9 PA9	IO IO	B4	8mA, pullup-pe	D9: SDRAM data bus bit 9, static memory data bus bit 9 PA9: GPIO group A bit 9	VDDIOL
D10 PA10	IO IO	C4	8mA, pullup-pe	D10: SDRAM data bus bit 10, static memory data bus bit 10 PA10: GPIO group A bit 10	VDDIOL
D11 PA11	IO IO	A3	8mA, pullup-pe	D11: SDRAM data bus bit 11, static memory data bus bit 11 PA11: GPIO group A bit 11	VDDIOL
D12 PA12	IO IO	B3	8mA, pullup-pe	D12: SDRAM data bus bit 12, static memory data bus bit 12 PA12: GPIO group A bit 12	VDDIOL
D13 PA13	IO IO	A2	8mA, pullup-pe	D13: SDRAM data bus bit 13, static memory data bus bit 13 PA13: GPIO group A bit 13	VDDIOL
D14 PA14	IO IO	B2	8mA, pullup-pe	D14: SDRAM data bus bit 14, static memory data bus bit 14 PA14: GPIO group A bit 14	VDDIOL
D15 PA15	IO IO	A1	8mA, pullup-pe	D15: SDRAM data bus bit 15, static memory data bus bit 15 PA15: GPIO group A bit 15	VDDIOL
D16 PA16	IO IO	A11	8mA, pullup-pe	D16: SDRAM data bus bit 16, static memory data bus bit 16 PA16: GPIO group A bit 16	VDDIOL
D17 PA17	IO IO	C11	8mA, pullup-pe	D17: SDRAM data bus bit 17, static memory data bus bit 17 PA17: GPIO group A bit 17	VDDIOL
D18 PA18	IO IO	D12	8mA, pullup-pe	D18: SDRAM data bus bit 18, static memory data bus bit 18 PA18: GPIO group A bit 18	VDDIOL
D19 PA19	IO IO	B11	8mA, pullup-pe	D19: SDRAM data bus bit 19, static memory data bus bit 19 PA19: GPIO group A bit 19	VDDIOL
D20 PA20	IO IO	C12	8mA, pullup-pe	D20: SDRAM data bus bit 20, static memory data bus bit 20 PA20: GPIO group A bit 20	VDDIOL
D21 PA21	IO IO	B12	8mA, pullup-pe	D21: SDRAM data bus bit 21, static memory data bus bit 21 PA21: GPIO group A bit 21	VDDIOL
D22 PA22	IO IO	A13	8mA, pullup-pe	D22: SDRAM data bus bit 22, static memory data bus bit 22 PA22: GPIO group A bit 22	VDDIOL
D23 PA23	IO IO	B13	8mA, pullup-pe	D23: SDRAM data bus bit 23, static memory data bus bit 23 PA23: GPIO group A bit 23	VDDIOL

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D24 PA24	IO IO	D13	8mA, pullup-pe	D24: SDRAM data bus bit 24, static memory data bus bit 24 PA24: GPIO group A bit 24	VDDIOL
D25 PA25	IO IO	C13	8mA, pullup-pe	D25: SDRAM data bus bit 25, static memory data bus bit 25 PA25: GPIO group A bit 25	VDDIOL
D26 PA26	IO IO	A14	8mA, pullup-pe	D26: SDRAM data bus bit 26, static memory data bus bit 26 PA26: GPIO group A bit 26	VDDIOL
D27 PA27	IO IO	C14	8mA, pullup-pe	D27: SDRAM data bus bit 27, static memory data bus bit 27 PA27: GPIO group A bit 27	VDDIOL
D28 PA28	IO IO	A15	8mA, pullup-pe	D28: SDRAM data bus bit 28, static memory data bus bit 28 PA28: GPIO group A bit 28	VDDIOL
D29 PA29	IO IO	B15	8mA, pullup-pe	D29: SDRAM data bus bit 29, static memory data bus bit 29 PA29: GPIO group A bit 29	VDDIOL
D30 PA30	IO IO	A16	8mA, pullup-pe	D30: SDRAM data bus bit 30, static memory data bus bit 30 PA30: GPIO group A bit 30	VDDIOL
D31 PA31	IO IO	C15	8mA, pullup-pe	D31: SDRAM data bus bit 31, static memory data bus bit 31 PA31: GPIO group A bit 31	VDDIOL
A0 PB0	O IO	A8	12mA, pullup-pe	A0: SDRAM/Static memory address bus bit 0 PB0: GPIO group B bit 0	VDDIOL
A1 PB1	O IO	E10	12mA, pullup-pe	A1: SDRAM/Static memory address bus bit 1 PB1: GPIO group B bit 1	VDDIOL
A2 PB2	O IO	C6	12mA, pullup-pe	A2: SDRAM/Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIOL
A3 PB3	O IO	B9	12mA, pullup-pe	A3: SDRAM/Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIOL
A4 PB4	O IO	B6	12mA, pullup-pe	A4: SDRAM/Static memory address bus bit 4 PB4: GPIO group B bit 4	VDDIOL
A5 PB5	O IO	C9	12mA, pullup-pe	A5: SDRAM/Static memory address bus bit 5 PB5: GPIO group B bit 5	VDDIOL
A6 PB6	O IO	A5	12mA, pullup-pe	A6: SDRAM/Static memory address bus bit 6 PB6: GPIO group B bit 6	VDDIOL
A7 PB7	O IO	D9	12mA, pullup-pe	A7: SDRAM/Static memory address bus bit 7 PB7: GPIO group B bit 7	VDDIOL
A8 PB8	O IO	B7	12mA, pullup-pe	A8: SDRAM/Static memory address bus bit 8 PB8: GPIO group B bit 8	VDDIOL
A9 PB9	O IO	A10	12mA, pullup-pe	A9: SDRAM/Static memory address bus bit 9 PB9: GPIO group B bit 9	VDDIOL
A10 PB10	O IO	E8	12mA, pullup-pe	A10: SDRAM/Static memory address bus bit 10 PB10: GPIO group B bit 10	VDDIOL
A11 PB11	O IO	E9	12mA, pullup-pe	A11: SDRAM/Static memory address bus bit 11 PB11: GPIO group B bit 11	VDDIOL
A12 PB12	O IO	C8	12mA, pullup-pe	A12: SDRAM/Static memory address bus bit 12 PB12: GPIO group B bit 12	VDDIOL
A13 PB13	O IO	C7	12mA, pullup-pe	A13: SDRAM/Static memory address bus bit 13 PB13: GPIO group B bit 13	VDDIOL
A14 PB14	O IO	B5	12mA, pullup-pe	A14: SDRAM/Static memory address bus bit 14 PB14: GPIO group B bit 14	VDDIOL
DCS0_ PB16	O IO	D8	8mA, pullup-pe	DCS0_: SDRAM chip select 0 PB16: GPIO group B bit 16	VDDIOL
DCS1_ PE28	O IO	B8	8mA, pullup-pe	DCS1_: SDRAM chip select 1 PE28: GPIO group E bit 28	VDDIOL
RAS_ PB17	O IO	D10	8mA, pullup-pe	RAS_: SDRAM row address strobe PB17: GPIO group B bit 17	VDDIOL
CAS_ PB18	O IO	C10	8mA, pullup-pe	CAS_: SDRAM column address strobe PB18: GPIO group B bit 18	VDDIOL

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SDWE_ & BUFD_ PB19	O IO	E11	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB19: GPIO group B bit 19	VDDIOL
WE0_ PB20	O IO	D3	8mA, pullup-pe	WE0_: SDRAM/Static memory byte 0 write enable PB20: GPIO group B bit 20	VDDIOL
WE1_ PB21	O IO	C5	8mA, pullup-pe	WE1_: SDRAM/Static memory byte 1 write enable PB21: GPIO group B bit 21	VDDIOL
WE2_ PB22	O IO	D11	8mA, pullup-pe	WE2_: SDRAM/Static memory byte 2 write enable PB22: GPIO group B bit 22	VDDIOL
WE3_ PB23	O IO	B14	8mA, pullup-pe	WE3_: SDRAM/Static memory byte 3 write enable PB23: GPIO group B bit 23	VDDIOL
CKO PB24	O IO	A7	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIOL
CKE PB25	O IO	B10	8mA, pullup-pe	CKE: SDRAM clock enable PB25: GPIO group B bit 25	VDDIOL

Table 2-2 EMC Static Memory Pins (31; all GPIO shared: PB15, PC0~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 A20 PC0	IO O IO	A17	4mA, pullup-pe	SD0: Static memory data bus bit 0 A20: Static memory address bus bit 0 PC0: GPIO group C bit 0	VDDIO
SD1 A21 PC1	IO O IO	B16	4mA, pullup-pe	SD1: Static memory data bus bit 1 A21: Static memory address bus bit 1 PC1: GPIO group C bit 1	VDDIO
SD2 A22 PC2	IO O IO	B17	4mA, pullup-pe	SD2: Static memory data bus bit 2 A22: Static memory address bus bit 2 PC2: GPIO group C bit 2	VDDIO
SD3 A23 PC3	IO O IO	C16	4mA, pullup-pe	SD3: Static memory data bus bit 3 A23: Static memory address bus bit 3 PC3: GPIO group C bit 3	VDDIO
SD4 A24 PC4	IO O IO	C17	4mA, pullup-pe	SD4: Static memory data bus bit 4 A24: Static memory address bus bit 4 PC4: GPIO group C bit 4	VDDIO
SD5 A25 PC5	IO O IO	D15	4mA, pullup-pe	SD5: Static memory data bus bit 5 A25: Static memory address bus bit 5 PC5: GPIO group C bit 5	VDDIO
SD6 PC6	IO IO	D16	4mA, pullup-pe	SD6: Static memory data bus bit 6 PC6: GPIO group C bit 6	VDDIO
SD7 PC7	IO IO	D17	4mA, pullup-pe	SD7: Static memory data bus bit 7 PC7: GPIO group C bit 7	VDDIO
SD8 TSDI0 PC8	IO I IO	J13	2mA, pullup-pe	SD8: Static memory data bus bit 8 TSDI0: TS interface input data bus bit 0 PC8: GPIO group C bit 8	VDDIO
SD9 TSDI1 PC9	IO I IO	H17	2mA, pullup-pe	SD9: Static memory data bus bit 9 TSDI1: TS interface input data bus bit 1 PC9: GPIO group C bit 9	VDDIO
SD10 TSDI2 PC10	IO I IO	H16	2mA, pullup-pe	SD10: Static memory data bus bit 10 TSDI2: TS interface input data bus bit 2 PC10: GPIO group C bit 10	VDDIO
SD11 TSDI3 PC11	IO I IO	H15	2mA, pullup-pe	SD11: Static memory data bus bit 11 TSDI3: TS interface input data bus bit 3 PC11: GPIO group C bit 11	VDDIO
SD12 TSDI4 PC12	IO I IO	H14	2mA, pullup-pe	SD12: Static memory data bus bit 12 TSDI4: TS interface input data bus bit 4 PC12: GPIO group C bit 12	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD13 TSDI5 PC13	IO I IO	H13	2mA, pullup-pe	SD13: Static memory data bus bit 13 TSDI5: TS interface input data bus bit 5 PC13: GPIO group C bit 13	VDDIO
SD14 TSDI6 PC14	IO I IO	G17	2mA, pullup-pe	SD14: Static memory data bus bit 14 TSDI6: TS interface input data bus bit 6 PC14: GPIO group C bit 14	VDDIO
SD15 TSDI7 PC15	IO I IO	G16	2mA, pullup-pe	SD15: Static memory data bus bit 15 TSDI7: TS interface input data bus bit 7 PC15: GPIO group C bit 15	VDDIO
A15_3 CL PB15	O O IO	F12	2mA, pullup-pe	A15_3: Static memory address bus bit 15 or bit 3 CL: NAND flash command latch PB15: GPIO group B bit 15	VDDIO
A16_4 AL PC16	O O IO	F11	2mA, pullup-pe	A16_4: Static memory address bus bit 16 or bit 4 AL: NAND flash address latch PC16: GPIO group C bit 16	VDDIO
SA0 A17 PC17	O O O	E15	2mA, pullup-pe	SA0: Static memory address bus bit 0 A17: Static memory address bus bit 17 PC17: GPIO group C bit 17	VDDIO
SA1 A18 PC18	O O IO	E14	2mA, pullup-pe	SA1: Static memory address bus bit 1 A18: Static memory address bus bit 18 PC18: GPIO group C bit 18, sometimes output only[3]	VDDIO
SA2 A19 PC19	O O IO	E12	2mA, pullup-pe	SA2: Static memory address bus bit 2 A19: Static memory address bus bit 19 PC19: GPIO group C bit 19, sometimes output only[3]	VDDIO
WAIT_ PC20	I IO	R15	2mA, pullup-pe	WAIT_: Slow static memory/device wait signal PC20: GPIO group C bit 20	VDDIO
CS1_ PC21	O IO	G15	2mA, pullup-pe	CS1_: Static memory chip select 1 PC21: GPIO group C bit 21	VDDIO
CS2_ PC22	O IO	G14	2mA, pullup-pe	CS2_: Static memory chip select 2 PC22: GPIO group C bit 22	VDDIO
CS3_ PC23	O IO	G13	2mA, pullup-pe	CS3_: Static memory chip select 3 PC23: GPIO group C bit 23	VDDIO
CS4_ PC24	O IO	F16	2mA, pullup-pe	CS4_: Static memory chip select 4 PC24: GPIO group C bit 24	VDDIO
RD_ PC25	O IO	F15	2mA, pullup-pe	RD_: Static memory read strobe PC25: GPIO group C bit 25	VDDIO
WR_ PC26	O IO	F14	2mA, pullup-pe	WR_: Static memory write strobe PC26: GPIO group C bit 26	VDDIO
PC27 (FRB)	IO	F13	2mA, pullup-pe	PC27: GPIO group C bit 27. If NAND flash is used, it should connect to NAND FRB (NAND flash ready/busy)	VDDIO
FRE_ PC28	O IO	E17	2mA, pullup-pe	FRE_: NAND flash read enable PC28: GPIO group C bit 28	VDDIO
FWE_ PC29	O IO	E16	2mA, pullup-pe	FWE_: NAND flash write enable PC29: GPIO group C bit 29	VDDIO

Table 2-3 LCDC Pins (26; all GPIO shared: PD0~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_D0 PD0	O IO	M7	4mA, pullup-pe	LCD_D0: LCD data bus bit 0 PD0: GPIO group D bit 0	VDDIO
LCD_D1 PD1	O IO	M6	4mA, pullup-pe	LCD_D1: LCD data bus bit 1 PD1: GPIO group D bit 1	VDDIO
LCD_D2 PD2	O IO	M5	4mA, pullup-pe	LCD_D2: LCD data bus bit 2 PD2: GPIO group D bit 2	VDDIO
LCD_D3 PD3	O IO	M4	4mA, pullup-pe	LCD_D3: LCD data bus bit 3 PD3: GPIO group D bit 3	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_D4 PD4	O IO	M3	4mA, pullup-pe	LCD_D4: LCD data bus bit 4 PD4: GPIO group D bit 4	VDDIO
LCD_D5 PD5	O IO	M2	4mA, pullup-pe	LCD_D5: LCD data bus bit 5 PD5: GPIO group D bit 5	VDDIO
LCD_D6 PD6	O IO	L5	4mA, pullup-pe	LCD_D6: LCD data bus bit 6 PD6: GPIO group D bit 6	VDDIO
LCD_D7 PD7	O IO	L4	4mA, pullup-pe	LCD_D7: LCD data bus bit 7 PD7: GPIO group D bit 7	VDDIO
LCD_D8 PD8	O IO	L3	4mA, pullup-pe	LCD_D8: LCD data bus bit 8 PD8: GPIO group D bit 8	VDDIO
LCD_D9 PD9	O IO	L2	4mA, pullup-pe	LCD_D9: LCD data bus bit 9 PD9: GPIO group D bit 9	VDDIO
LCD_D10 PD10	O IO	L1	4mA, pullup-pe	LCD_D10: LCD data bus bit 10 PD10: GPIO group D bit 10	VDDIO
LCD_D11 PD11	O IO	K5	4mA, pullup-pe	LCD_D11: LCD data bus bit 11 PD11: GPIO group D bit 11	VDDIO
LCD_D12 PD12	O IO	K4	4mA, pullup-pe	LCD_D12: LCD data bus bit 12 PD12: GPIO group D bit 12	VDDIO
LCD_D13 PD13	O IO	K3	4mA, pullup-pe	LCD_D13: LCD data bus bit 13 PD13: GPIO group D bit 13	VDDIO
LCD_D14 PD14	O IO	J5	4mA, pullup-pe	LCD_D14: LCD data bus bit 14 PD14: GPIO group D bit 14	VDDIO
LCD_D15 PD15	O IO	J4	4mA, pullup-pe	LCD_D15: LCD data bus bit 15 PD15: GPIO group D bit 15	VDDIO
LCD_D16 PD16	O IO	J3	4mA, pullup-pe	LCD_D16: LCD data bus bit 16 PD16: GPIO group D bit 16	VDDIO
LCD_D17 PD17	O IO	H3	4mA, pullup-pe	LCD_D17: LCD data bus bit 17 PD17: GPIO group D bit 17	VDDIO
LCD_PCLK PD18	IO IO	K2	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PD18: GPIO group D bit 18	VDDIO
LCD_HSYN PD19	IO IO	K1	4mA, pullup-pe	LCD_HSYN: LCD line clock/horizontal sync PD19: GPIO group D bit 19	VDDIO
LCD_VSYN PD20	IO IO	J2	4mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PD20: GPIO group D bit 20	VDDIO
LCD_DE PD21	O IO	H2	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PD21: GPIO group D bit 21	VDDIO
LCD_CLS LCD_D_R1 PD22	O O IO	H1	4mA, pullup-pe	LCD_CLS: LCD CLS output LCD_D_R1: Red data bit 1, used in 24-bit data bus PD22: GPIO group D bit 22	VDDIO
LCD_SPL LCD_D_G0 PD23	O O IO	G1	4mA, pullup-pe	LCD_SPL: LCD SPL output LCD_D_G0: Green data bit 0, used in 24-bit data bus PD23: GPIO group D bit 23	VDDIO
LCD_PS LCD_D_G1 PD24	O O IO	H5	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT LCD_D_G1: Green data bit 1, used in 24-bit data bus PD24: GPIO group D bit 24	VDDIO
LCD_REV LCD_D_B1 PD25	O O IO	H4	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT LCD_D_B1: Blue data bit 1, used in 24-bit data bus PD25: GPIO group D bit 25	VDDIO

Table 2-4 CIM Pins (12; all GPIO shared: PE0~11)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_D0 PE0	I IO	U16	2mA, pullup-pe	CIM_D0: CIM data input bit 0 PE0: GPIO group E bit 0	VDDIO
CIM_D1	I	T16	2mA,	CIM_D1: CIM data input bit 1	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PE1	IO		pullup-pe	PE1: GPIO group E bit 1	
CIM_D2 PE2	I IO	R17	2mA, pullup-pe	CIM_D2: CIM data input bit 2 PE2: GPIO group E bit 2	VDDIO
CIM_D3 PE3	I IO	R16	2mA, pullup-pe	CIM_D3: CIM data input bit 3 PE3: GPIO group E bit 3	VDDIO
CIM_D4 PE4	I IO	P16	2mA, pullup-pe	CIM_D4: CIM data input bit 4 PE4: GPIO group E bit 4	VDDIO
CIM_D5 PE5	I IO	N16	2mA, pullup-pe	CIM_D5: CIM data input bit 5 PE5: GPIO group E bit 5	VDDIO
CIM_D6 PE6	I IO	P15	2mA, pullup-pe	CIM_D6: CIM data input bit 6 PE6: GPIO group E bit 6	VDDIO
CIM_D7 PE7	I IO	N15	2mA, pullup-pe	CIM_D7: CIM data input bit 7 PE7: GPIO group E bit 7	VDDIO
CIM_MCLK PE8	O IO	N17	4mA, pullup-pe	CIM_MCLK: CIM master clock output PE8: GPIO group E bit 8	VDDIO
CIM_PCLK PE9	I IO	P17	2mA, pullup-pe	CIM_PCLK: CIM pixel clock input PE9: GPIO group E bit 9	VDDIO
CIM_VSYN PE10	I IO	U17	2mA, pullup-pe	CIM_VSYN: CIM VSYNC input PE10: GPIO group E bit 10	VDDIO
CIM_HSYN PE11	I IO	T17	2mA, pullup-pe	CIM_HSYN: CIM HSYNC input PE11: GPIO group E bit 11	VDDIO

2.4.2 Pin for serial interfaces

Table 2-5 MSC (MMC/SD) 0/1, Ext. DMA, UART 0 Pins (16; all GPIO shared: PF0~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 PF0	IO IO	M13	4mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 PF0: GPIO group F bit 0	VDDIO
MSC0_D1 PF1	IO IO	L17	4mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 PF1: GPIO group F bit 1	VDDIO
MSC0_D2 DREQ PF2	IO I IO	L16	4mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 DREQ: External DMA request input PF2: GPIO group F bit 2	VDDIO
MSC0_D3 DACK PF3	IO O IO	L15	4mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 DACK: External DMA acknowledge output PF3: GPIO group F bit 3	VDDIO
MSC0_D4 UART0_RxD PF4	IO I IO	L14	4mA, pullup-pe	MSC0_D4: MSC (MMC/SD) 0 data bit 4 UART0_RxD: UART 0 Receiving data PF4: GPIO group F bit 4	VDDIO
MSC0_D5 UART0_TxD PF5	IO O IO	L13	4mA, pullup-pe	MSC0_D5: MSC (MMC/SD) 0 data bit 5 UART0_TxD: UART 0 transmitting data PF5: GPIO group F bit 5	VDDIO
MSC0_D6 UART0_CTS _ PF6	IO I IO	K17	4mA, pullup-pe	MSC0_D6: MSC (MMC/SD) 0 data bit 6 UART0_CTS_: UART 0 CTS_ input PF6: GPIO group F bit 6	VDDIO
MSC0_D7 UART0_RTS _ PF7	IO O IO	K16	4mA, pullup-pe	MSC0_D7: MSC (MMC/SD) 0 data bit 7 UART0_RTS_: UART 0 RTS_ output PF7: GPIO group F bit 7	VDDIO
MSC0_CLK PF8	O IO	K15	4mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output PF8: GPIO group F bit 8	VDDIO
MSC0_CMD PF9	IO IO	K14	4mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command PF9: GPIO group F bit 9	VDDIO
MSC1_D0 PF10	IO IO	E7	4mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 PF10: GPIO group F bit 10	VDDIO
MSC1_D1 PF11	IO IO	E6	4mA, pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 PF11: GPIO group F bit 11	VDDIO
MSC1_D2 PF12	IO IO	D7	4mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 PF12: GPIO group F bit 12	VDDIO
MSC1_D3 PF13	IO IO	D6	4mA, pullup-pe	MSC1_D3: MSC (MMC/SD) 1 data bit 3 PF13: GPIO group F bit 13	VDDIO
MSC1_CLK PF14	O IO	E2	4mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output PF14: GPIO group F bit 14	VDDIO
MSC1_CMD PF15	IO IO	D5	4mA, pullup-pe	MSC1_CMD: MSC (MMC/SD) 1 command PF15: GPIO group F bit 15	VDDIO

Table 2-6 SSI 0 Pins (6; all GPIO shared: PB26~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_CLK PB26	O IO	N12	4mA, pullup-pe	SSI0_CLK: SSI 0 clock output PB26: GPIO group B bit 26	VDDIO
SSI0_DT PB27	O IO	N10	4mA, pullup-pe	SSI0_DT: SSI 0 data output PB27: GPIO group B bit 27	VDDIO
SSI0_DR PB28	I IO	N11	4mA, pullup-pe	SSI0_DR: SSI 0 data input PB28: GPIO group B bit 28	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_CE0_ PB29	O IO	M8	4mA, pullup-pe	SSI0_CE0_: SSI 0 chip enable 0 PB29: GPIO group B bit 29	VDDIO
SSI0_GPC PB30	O IO	M9	4mA, pullup-pe	SSI0_GPC: SSI 0 general-purpose control signal PB30: GPIO group B bit 30	VDDIO
SSI0_CE1_ PB31	O IO	M10	4mA, pullup-pe	SSI0_CE1_: SSI 0 chip enable 1 PB31: GPIO group B bit 31	VDDIO

Table 2-7 SSI 1, Pins (5; all GPIO shared: PD26~30)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI1_CLK PD26	O IO	F2	4mA, pullup-pe	SSI1_CLK: SSI 1 clock output PD26: GPIO group D bit 26	VDDIO
SSI1_DT PD27	O IO	E4	4mA, pullup-pe	SSI1_DT: SSI 1 data output PD27: GPIO group D bit 27	VDDIO
SSI1_DR PD28	I IO	F5	4mA, pullup-pe	SSI1_DR: SSI 1 data input PD28: GPIO group D bit 28	VDDIO
SSI1_CE0_ PD29	O IO	F3	4mA, pullup-pe	SSI1_CE0_: SSI 1 chip enable 0 PD29: GPIO group D bit 29	VDDIO
SSI1_CE1_ PD30	O IO	F4	4mA, pullup-pe	SSI1_CE1_: SSI 1 chip enable 1 PD30: GPIO group D bit 30	VDDIO

Table 2-8 I2C Pins (2; all GPIO shared: PE12~13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
I2C_SDA PE12	IO IO	U1	4mA, pullup-pe	I2C_SDA: I2C serial data PE12: GPIO group E bit 12	VDDIO
I2C_SCK PE13	IO IO	T1	4mA, pullup-pe	I2C_SCK: I2C serial clock PE13: GPIO group E bit 13	VDDIO

Table 2-9 UART 1/2, PCM, WIRE1, AIC and TCU/PWM Pins (12; all GPIO shared: PE16~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD PE16	I IO	R3	2mA, pullup-pe	UART1_RxD: UART 1 Receiving data PE16: GPIO group E bit 16	VDDIO
UART1_TxD PE17	O IO	R2	2mA, pullup-pe	UART1_TxD: UART 1 transmitting data PE17: GPIO group E bit 17	VDDIO
UART1_CTS_ PCM_DIN PE18	I I IO	N6	2mA, pullup-pe	UART1_CTS_: UART 1 CTS_ input PCM_DIN: PCM data input PE18: GPIO group E bit 18	VDDIO
UART1_RTS_ PCM_DOUT PE19	O O IO	P5	2mA, pullup-pe	UART1_RTS_: UART 1 RTS_ output PCM_DOUT: PCM data output PE19: GPIO group E bit 19	VDDIO
PWM0 PCM_CLK PE20	O IO IO	N7	2mA, pullup-pe	PWM0: PWM 0 output PCM_CLK: PCM clock PE20: GPIO group E bit 20	VDDIO
PWM1 PCM_SYN PE21	O IO IO	N8	2mA, pullup-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PCM_SYN: PCM sync PE21: GPIO group E bit 21	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM2 SCLK_RSTN PE22	O O IO	N14	2mA, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock SCLK_RSTN: I2S system clock output or AC97 reset output PE22: GPIO group E bit 22	VDDIO
PWM3 BCLK PE23	O IO IO	M14	2mA, pullup-pe	PWM3: PWM 3 output BCLK: AC97/I2S bit clock PE23: GPIO group E bit 23	VDDIO
PWM4 SYNC PE24	O IO IO	M15	2mA, pullup-pe	PWM4: PWM 6 output SYNC: AC97 frame SYNC or I2S Left/Right PE24: GPIO group E bit 24	VDDIO
PWM5 OWI PE25	O IO IO	M16	2mA, pullup-pe	PWM5: PWM 7 output OWI: One wire interface PE25: GPIO group E bit 25	VDDIO
SDATO UART2_TxD PE26	O O IO	M12	2mA, pullup-pe	SDATO: AC97/I2S serial data output UART2_TxD: UART 2 transmitting data PE26: GPIO group E bit 26	VDDIO
SDATI UART2_RxD PE27	I I IO	M11	2mA, pullup-pe	SDATI: AC97/I2S serial data input UART2_RxD: UART 2 Receiving data PE27: GPIO group E bit 27	VDDIO

Table 2-10 UART 3 Pins (4; all GPIO shared: PF16~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART3_RxD PF16	I IO	G2	2mA, pullup-pe	UART3_RxD: UART 3 Receiving data PF16: GPIO group F bit 16	VDDIO
UART3_TxD PF17	O IO	G3	2mA, pullup-pe	UART3_TxD: UART 3 transmitting data PF17: GPIO group F bit 17	VDDIO
UART3_CTS_ LCD_D_R0 PF18	I O IO	G4	4mA, pullup-pe	UART3_CTS_: UART 3 CTS_ input LCD_D_R0: Red data bit 0, used in 24-bit data bus PF18: GPIO group F bit 18	VDDIO
UART3_RTS_ LCD_D_B0 PF19	O O IO	G5	4mA, pullup-pe	UART3_RTS_: UART 3 RTS_ output LCD_D_B0: Blue data bit 0, used in 24-bit data bus PF19: GPIO group F bit 19	VDDIO

Table 2-11 TSSI Control Pins (4; all GPIO shared: PF20~23)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TSCLK PF20	I IO	K13	2mA, pullup-pe	TSCLK: TS interface clock input PF20: GPIO group F bit 20	VDDIO
TSSTR PF21	I IO	J16	2mA, pullup-pe	TSSTR: TS interface frame start input PF21: GPIO group F bit 21	VDDIO
TSFRM PF22	I IO	J15	2mA, pullup-pe	TSFRM: TS interface frame valid input PF22: GPIO group F bit 22	VDDIO
TSFAIL PF23	I IO	J14	2mA, pullup-pe	TSFAIL: TS interface error package indicator input PF23: GPIO group F bit 23	VDDIO

2.4.3 Pin for system/misc/UART2

Table 2-12 JTAG/UART Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	P10	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK UART2_RTS_	I O	P13	2mA, Schmitt, pulldown-pe	TCK: JTAG clock UART2_RTS_: UART 2 RTS_ output, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
TMS UART2_CTS_	I I	R10	Schmitt, pullup-pe	TMS: JTAG mode select UART2_CTS_: UART 2 CTS_ input, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
TDI UART2_RxD	I I	P9	Schmitt, pullup-pe	TDI: JTAG serial data input UART2_RxD: UART 2 Receiving data, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO
TDO UART2_TxD	O O	N9	4mA	TDO: JTAG serial data output UART2_TxD: UART 2 transmitting data, PE31 is used to select between JTAG and UART, reset to JTAG	VDDIO

Table 2-13 System Pins (3, 2 GPIO shared: PC30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
BOOT_SEL0 PC30	I O	P3	2mA, Schmitt	BOOT_SEL0: Boot select bit 0 PC30: GPIO group C bit 30, reset to BOOT_SEL0	VDDIO
BOOT_SEL1 PC31	I IO	R4	2mA, Schmitt	BOOT_SEL1: Boot select bit 1 PC31: GPIO group C bit 31, reset to BOOT_SEL1, reset to BOOT_SEL1	VDDIO
TEST_MODE	I	N4	Schmitt, pull-down	TEST_TE: Test mode. This pin must be set to low voltage in function	VDDIO

2.4.4 Pin for analog interfaces and corresponding power/ground

Table 2-14 Audio CODEC Pins (13)

Pin Names	IO	Loc	Pin Description	Power
AOHPL	AO	T15	AOHPL: Left headphone out	AVD_{HP}
AOHPR	AO	U15	AOHPR: Right headphone out	AVD_{HP}
AOHPM	AO	R13	HPCMO: Headphone common mode output	AVD_{HP}
AOHPMS	AI	R14	HPCMSI: Headphone common mode sense input	AVD_{HP}
MICP	AI	R12	MICP: Microphone input	AVD_{HP}
MICBIAS	AO	R11	MICBIAS: Microphone bias	AVD_{HP}
AIL	AI	P12	AIL: Left line input	AVD_{HP}
AIR	AI	P11	AIR: Right line input	AVD_{HP}
VCOM	AO	U13	VCOM: Voltage Reference Output	AVD_{HP}
AVDHP	P	T14	AVDHP: Headphone amplifier power, 3.3V	-
AVSHP	P	T13	AVSHP: Headphone amplifier ground	-
AVDCDC	P	U14	AVDCDC: CODEC analog power, 3.3V	-
AVSCDC	P	T12	AVSCDC: CODEC analog ground	-

Table 2-15 USB device 2.0 and host 1.1 Pins (8)

Pin Names	IO	Loc	Pin Description	Power
DP0	AIO	T7	DP0: USB 2.0 device data plus	AVD_{USB}
DM0	AIO	U7	DM0: USB 2.0 device data minus	AVD_{USB}
RREF	AIO	P7	RREF: External Reference for USB 2.0 device. Connect a 2.5kΩ external reference resistor, with 5% tolerance to analog ground AVSUSB	AVD_{USB}
VDDA	AIO	T9	VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground AVSUSB	AVD_{USB}
AVDUSB	P	R7	AVDUSB: USB analog power, 3.3V	-
AVSUSB	P	R8	AVSUSB: USB analog ground	-
DP1	AIO	T8	DP1: USB 1.1 host data plus	AVD_{USB}
DM1	AIO	U8	DM1: USB 1.1 host data minus	AVD_{USB}

Table 2-16 SAR ADC Pins (8)

Pin Names	IO	Loc	Pin Description	Power
XP	AI	P6	XP: Touch screen X+ input	AVD_{AD}
XN	AI	T5	XN: Touch screen X- input	AVD_{AD}
YP	AI	U4	YP: Touch screen Y+ input	AVD_{AD}
YN	AI	T4	YN: Touch screen Y- input	AVD_{AD}
PBAT/ADIN0	AI	R6	ADIN0: Battery voltage input or ADC general purpose input 0	AVD_{AD}
ADIN1	AI	T6	ADIN1: ADC general purpose input 1	AVD_{AD}
AVDAD	P	U5	AVDAD: ADC analog power, 3.3 V	-
AVSAD	P	R5	AVDAD: ADC analog ground	-

Table 2-17 Video DAC Pins (6)

Pin Names	IO	Loc	Pin Description	Power
LUMA	AO	N2	LUMA: DAC analog output for CVBS or luminance of S-Video	AVD_{DA}
CHROMA	AO	P2	CHROMA: DAC analog output Chrominance of S-Video	AVD_{DA}
AVDDA	P	N1	AVDDA: Power supply for LUMA and CHROMA output, 3.3 V (IO1:AVD33R, IO2:AVD33G, IO3:AVDD, VDWELL)	-
AVSDA	P	N3	AVSDA: Ground for LUMA and CHROMA output (IO1/IO2: AVS33R, AVS33G, AVSS, VSSUB)	-
REXT	AO	R1	REXT: For external resistor. REXT (ohm) = VREFIN(V) * 7.31 / IOFS(A) = 1.24 * 7.31 / 34.1 * 1000	AVD_{DA}
COMP	AIO	P1	COMP: Compensation pin. This pin should be connected with 0.01uf ceramic cap parallel with a 10uf tantalum cap to AVDDA externally	AVD_{DA}

Table 2-18 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	T2	10~30 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12/24/27MHz clock input	VDDIO
EXCLKO	AO	U2		EXCLKO: OSC output	VDDIO
VDDPLL	P	U3		VDDPLL: PLL analog power, 1.8V	-
VSSPLL	P	T3		VSSPLL: PLL analog ground	-

Table 2-19 RTC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	T10	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	U10		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	AO	P8	~2mA, open-drain	PWRON_: Power on/off control of main power	VDD_{RTC}
WKUP_ PE30	AI AI	T11	Schmitt	WKUP_: Wake signal after main power down PE30: GPIO group E bit 30, input/interrupt only	VDD_{RTC}
PPRST_	AI	U11	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	R9		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

2.4.5 Pin for IO and core power/ground

Table 2-20 IO/Core power supplies (27)

Pin Names	IO	Loc	Pin Description	Power
VDDIO	P	K7 K8 L8	VDDIO: IO digital power, 3.3V	-
VDDIOL	P	F8 F9 G8 H7 J7	VDDIO: IO digital power, 1.8V~3.3V	-
VSSIO	P	F7 F10 G9 H8 J6 J8 L9	VSSIO: IO digital ground	-
VDDCORE	P	H9 H10 J10 J12 K10 K11	VDDCORE: CORE digital power, 1.8V	-
VSSCORE	P	G10 H11 J9 J11 K9 L10	VSSCORE: CORE digital ground	-

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12Ma.
   b Pull-up: The IO cell contains a pull-up resistor.
   c Pull-down: The IO cell contains a pull-down resistor.
   d Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   e Schmitt: The IO cell is Schmitt trig input.

2 For any GPIO shared pin except WAIT_/PC27 and CKO/PB24, the reset state is GPIO input with internal pull-up. The WAIT_/PC27 and CKO/PB24 are initialed to WAIT_ and CKO functions with internal pull-up.

3 PC18/PC19 are sometimes used to decide the EXCLK frequency for USB boot. In this case they should be used as output only GPIO. Resisters may need to pull up/down these pins to tell which EXCLK is. Please reference to 3.5.3 for the details.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
VDDIOL power supplies voltage	-0.5	4.6	V
AVDUSB power supplies voltage	-0.3	3.9	V
AVDCDC power supplies voltage	-0.3	4.0	V
AVDHP power supplies voltage	-0.3	4.0	V
AVDAD power supplies voltage	-0.3	4.0	V
AVDDA power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to VDDIOL supplied non-supply pins	-0.5	4.6	V
Input voltage to AVDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to AVDAD supplied non-supply pins except PBAT	-0.5	4.0	V
Input voltage to AVDDA supplied non-supply pins	-0.5	4.0	V
Input voltage of PBAT	-0.5	6.0	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from VDDIOL supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from AVDAD supplied non-supply pins	-0.5	4.0	V
Output voltage from AVDDA supplied non-supply pins	-0.5	4.0	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{IOL}	VDDIOL voltage	1.62	1.8 2.5 3.3	3.63	V
V_{USB}	AVDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	AVDCDC voltage	3.0	3.3	3.6	V
V_{HP}	AVDHP voltage	3.0	3.3	3.6	V
V_{ADC}	AVDAD voltage	3.0	3.3	3.6	V
V_{DAC}	AVDDA voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO and VDDIOL@3.3V supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-IO}	Input high voltage	2.0		3.6	V
V_{IL-IO}	Input low voltage	-0.3		0.8	V
$V_{IH-IOL33}$	Input high voltage	2.0		3.6	V
$V_{IL-IOL33}$	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for VDDIOL@1.8V supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH-IOL18}$	Input high voltage	1.17	1.8	2.1	V
$V_{IL-IOL18}$	Input low voltage	-0.3		0.63	V

Table 3-5 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-UF}	Input voltage range for full speed applications	0		V_{USB}	V
V_{I-UH}	Input voltage range for high speed applications	120		400	mV

Table 3-6 Recommended operating conditions for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-U11}	Input voltage range	0		V_{USB}	V

Table 3-7 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{I-PBAT1}$	PBAT input voltage range when measuring low voltage battery	0		2.5	V
$V_{I-PBAT2}$	PBAT input voltage range when measuring high voltage battery	0		5	V
$V_{I-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V
V_{I-TSC}	XN/XP/YN/YP input voltage range	0		V_{ADC}	

Table 3-8 Recommended operating conditions for AVDCDC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
$V_{ILH-CDC}$	Input voltage range	0		V_{CDC}	V

Table 3-9 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-RTC}	Input high voltage	2.0		3.6	V
V_{IL-RTC}	Input low voltage	-0.3		0.8	V

Table 3-10 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-11 DC characteristics for VDDIO and VDDIOL@3.3V supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point		1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point		0.88	0.94	0.99	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		50	65	100	kΩ
R_{PD}	Pull-down Resistor		40	56	107	kΩ
C_{IO}	Capacitance of the pins		4	5	10	pF
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.4V for cells of	2mA	2.2	3.7	4.6	mA
		4mA	4.4	7.4	9.2	mA
		8mA	8.9	14.7	18.4	mA
		12mA	13.3	22.1	27.5	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = 2.4V for cells of	2mA	2.5	5.1	7.9	mA
		4mA	5.0	10.2	15.9	mA
		8mA	10.0	20.4	31.7	mA
		12mA	15.0	30.6	47.6	mA

Table 3-12 DC characteristics for VDDIOL@1.8V supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		0.87	0.92	0.98	V
V_{T+}	Schmitt trig low to high threshold point		0.95	0.99	1.00	V
V_{T-}	Schmitt trig high to low threshold point		0.56	0.58	0.60	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		94	148	261	kΩ
R_{PD}	Pull-down Resistor		77	135	312	kΩ
C_{IO}	Capacitance of the pins		4	5	10	pF
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.45	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		1.35			V
I_{OL-IO}	Low level output current	2mA	0.9	1.9	3.0	mA

	@ V_{OL-IO} = 0.45V for cells of	4mA	1.8	3.8	6.0	mA
		8mA	3.6	7.6	12.0	mA
		12mA	5.4	11.4	18.0	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = 1.35V for cells of	2mA	0.9	1.6	2.2	mA
		4mA	1.8	3.1	4.5	mA
		8mA	3.7	6.2	9.0	mA
		12mA	5.5	9.3	13.4	mA

Table 3-13 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-U20}	Output high voltage	1.5		V_{USB}	V
V_{OL-U20}	Output low voltage	0		0.4	V

Table 3-14 DC characteristics for USB 1.1 Host pins

Symbol	Description	Min	Typical	Max	Unit
V_{O-U11}	Output voltage range	0		V_{USB}	V
V_{DIS}	Differential input sensitivity	0.2			V
V_{CM}	Differential common mode range	0.8		2.5	V
V_{SE}	Single ended receiver threshold	0.8		2.0	V
I_{OZ-U11}	Tri-State leakage current			±10	μA
Z_{DRV}	Driver output resistance, including damping resistor	24		44	Ω
V_{OL-U11}	Static output low voltage			0.3	V
V_{OH-U11}	Static output high voltage	2.8			V

Table 3-15 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-ADC}	XN/XP/YN/YP output high voltage	0.9 * V_{ADC}		V_{ADC}	V
V_{OL-ADC}	XN/XP/YN/YP output low voltage	0		0.1 * V_{ADC}	V
R_{BAT}	BAT input resister		9.3		kΩ
R_{PDADC}	Internal pull down resister		10.4		kΩ

Table 3-16 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH-RTC}	Output high voltage	2.0		3.6	V
V_{OL-RTC}	Output low voltage	-0.3		0.8	V

3.4 Power Consumption Specifications

Power consumption depends on the operating frequency, operating voltage, program used which determines internal and external switching activities, external loading and even environment ambient. The typical power consumption of both dynamic and static for the JZ4750 processor are provided here.

Table 3-17 PLL (VDD_{PLL}) Dynamic Power Consumption

Conditions	PLL out	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL input clock = 24MHz	240MHz	6	mA
	360MHz	9	mA

Table 3-18 PLL (VDD_{PLL}) Static Power Consumption

Conditions	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL is in suspend mode	0.1	uA

Table 3-19 RTC (VDD_{RTC}) Dynamic Power Consumption

Conditions	Typical	Unit
VDDRTC = 3.3V, RTCLK = 32768Hz oscillator, Temperature = room	2	uA

Table 3-20 IO (VDD_{IO}) Dynamic Power Consumption

Conditions	SDRAM Clock	Typical	Unit
VDDIO = VDDIOL = 3.3V, VDDcore = 1.8V, Temperature = room, 32-bit SDRAM, CIM is not run, LCD run in 480 x 272 x 60, EXCLK = 24MHz oscillator, CPU clock is 3 times of SDRAM clock, run GCC program in Linux	80MHz	14	mA
	120MHz	21	mA

NOTE: IO dynamic power is greatly depends on the software environment and the hardware (board and other components) environment.

Table 3-21 IO (VDD_{IO}) Static Power Consumption

Conditions	Typical	Unit
VDDIO = VDDIOL = 3.3V, VDDcore = 1.8V, Temperature = room, oscillator stopped, No input floating, the pull-up/down is in same direction as the driving	0.1	uA

Table 3-22 CORE (VDD_{CORE}) Dynamic Power Consumption

Conditions	CPU Clock	Typical	Unit
VDDcore = 1.8V, Temperature = room, 32-bit SDRAM, CIM is not run, LCD run in 480 x 272 x 60, EXCLK = 24MHz oscillator, SDRAM clock is 1/3 of CPU clock, run GCC program in Linux	240MHz	70	mA
	360MHz	110	mA

NOTE: CORE dynamic power is greatly depends on the software environment.

Table 3-23 CORE (VDD_{CORE}) Static Power Consumption

Conditions	Typical	Unit
VDDcore = 1.8V, Temperature = room, EXCLK oscillator stopped, all clocks exception RTCLK are stopped	150	uA

Table 3-24 CODEC (AVD_{CDC} + AVD_{HP}) Dynamic Power Consumption

Conditions		Typical	Unit
AVDCDC = AVDHP = 3.3V, Temperature = room, 220uF capacitors, 16Ωheadphone load, 48k sample rate, stereo	Replay all zero samples	8	mA
	Replay full scale 1k sine wave	43	mA
	Typical replay in full volume	13	mA
	Typical replay in typical volume	8	mA
	Typical record	8	mA

Table 3-25 CODEC (AVD_{CDC} + AVD_{HP}) Static Power Consumption

Conditions	Typical	Unit
AVDCDC = AVDHP = 3.3V, Temperature = room, CODEC is in suspend mode	0.1	uA

Table 3-26 USB (AVD_{USB}) Dynamic Power Consumption

Conditions	Typical	Unit
USB 1.1 host is running only	1.7	mA
Both USB 1.1 host and USB 2.0 device is running	12	mA

Table 3-27 USB (AVD_{USB}) Static Power Consumption

Conditions	Typical	Unit
AVDUSB = 3.3V, Temperature = room, USB 2.0 device and USB 1.1 host are in suspend mode	0.1	uA

Table 3-28 ADC (AVD_{AD}) Dynamic Power Consumption

Conditions		Typical	Unit
AVDAD = 3.3V, Temperature = room, Resister between XP and XN, between YP and YN is 440Ω, pen touch in center of the touch screen, measure X, Y, Z values on every measurement	3 measure / 1ms	1.9	mA
	5 measure / 10ms	0.9	mA

Table 3-29 ADC (AVD_{AD}) Static Power Consumption

Conditions	Typical	Unit
AVDAD = 3.3V, Temperature = room, ADC is in suspend mode	0.1	uA

Table 3-30 DAC (AVD_{DA}) Dynamic Power Consumption

Conditions		Typical	Unit
AVDDA = 3.3V, Temperature = room, REXT = 75Ω	CVBS	40	mA
	S-Video	80	mA

Table 3-31 DAC (AVD_{DA}) Static Power Consumption

Conditions	Typical	Unit
AVDDA = 3.3V, Temperature = room, DAC is in suspend mode	0.1	uA

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4750 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-32.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1 VDDRTC

2 VDDA: AVDCDC, AVDHP

3 All other 3.3V VDDs and VDDIOL (VDD33): VDDIO, VDDIOL, AVDAD, AVDDA, AVDUSB

4 All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

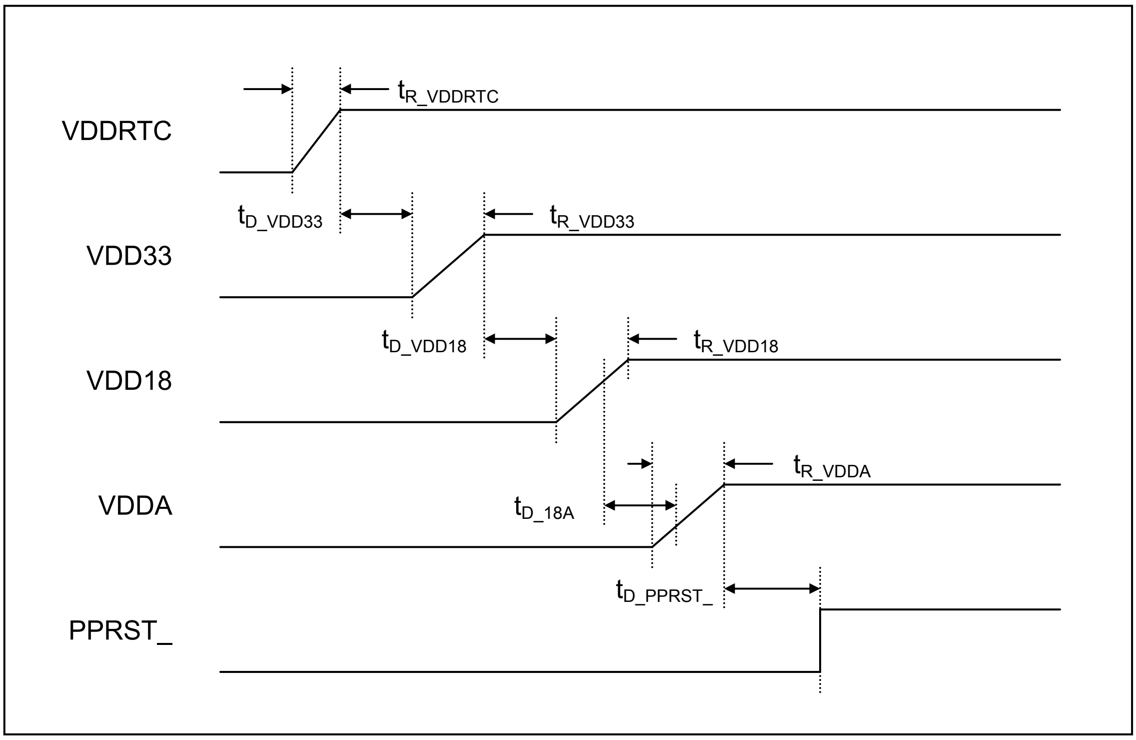


Figure 3-1 Power-On Timing Diagram

Table 3-32 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33	$-t_{R\_VDDRTC}$	–	–	ms[1]

	applies				
t_{R_VDD33}	VDD33 rise/stabilization time	0	–	100	ms
t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	$-t_{R\_VDD33}/2$	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0	–	100	ms
t_{D_18A}	Delay between VDD18 (actually VDDcore) arriving 1.5V and VDDA arriving 1V	0.01	–	10	ms
t_{R_VDDA}	VDDA rise/stabilization time	0	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDDA stable and PPRST_ deasserted	0.1	–	–	ms

NOTES:

1 VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.

2 VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except WAIT_ and CKO pins, are put to GPIO input function with the internal pull-up set to on. The WAIT_ and CKO pins are set to wait and CKO function with the internal pull-up set to on. The PWRON_ is output 0. The 32768Hz/24MHz oscillators are on. The JTAG/UART is put to JTAG function and the TDO is output high-Z (suppose TRST_ is 0). The analog devices, the USB 2.0 PHY, USB 1.1 PHY, the CODEC DAC/ADC, the SAR-ADCs and the video DAC are put in suspend mode.

3.5.3 BOOT

JZ4750 support 5 different boot sources depending on BOOT_SEL0 and BOOT_SEL1 pin values. Table 3-33 lists them.

Table 3-33 Boot from 5 boot sources

BOOT_SEL1	BOOT_SEL0	Boot Source
0	0	Boot from NOR flash at CS4 or SPI0/CE0
0	1	Boot from NAND flash at CS1
1	0	Boot from SD card from MSC0
1	1	Boot from USB device

When JZ4750 BOOT from NOR at CS4_ or from NAND at CS1_ or MSC0, some of the memory interface pins are set to function pin from the default GPIO pin and are used in executing BOOT ROM instructions. When BOOT from USB, none of any pins are used. Table 3-34 lists the cases.

Table 3-34 Pins are used and are set to function pins during BOOT

Boot Source Condition	GPIO pin state changed from RESET
USB	None
8-bits NOR flash at CS4_	PA0~7, PB0~15,19~20, PC0~5,16~20,24~26
16-bits NOR flash at CS4_	PA0~15, PB0~15,19~20, PC0~5,16~20,24~26
32-bits NOR flash at CS4_	PA0~31, PB0~15,19~20, PC0~5,16~20,24~26
8-bits NAND flash at CS1_	PB15,19 PC16,20,21,28~29, PA0~7(for shared mode) or PC0~7(for unshared mode)
16-bits NAND flash at CS1_	PB15,19 PC16,20,21,28~29, PA0~15(for shared mode) or PC0~15(for unshared mode)
MSC0	PF0,8~9
SPI0/CE0	PB26~29

In case of USB device boot, EXCLK frequency must be known. The EXCLK frequency is decided in following steps.

Step 1: If OTPBR1 is used to indicate the frequency, get frequency from it (reference to *JZ4750_E.8_otp_spec.pdf* for the details). The valid EXCLK is: 12MHz, 13MHz, 19.2MHz, 24MHz, 26MHz and 27MHz.

Step 2: Else, if RTCLK (32768Hz) is available, boot code tries to find out the frequency of 12MHz, 13MHz, 24MHz, 26MHz and 27MHz.

Step 3: If both OTPBR1 and RTCLK methods are not available, PC18 and PC19 pin states are detected to decide the frequency from 12MHz, 13MHz, 19.2MHz and 26MHz. Followings are the suggested setting:

a In case of EXCLK frequency is 12MHz, PC18 and PC19 should be left floating from outside while internal pull up makes it high.

b In case of EXCLK is one of 13MHz, 19.2MHz or 26MHz, these pins should be pull up/down by resister ≤10kΩ from outside.

EXCLK	PC18 pin	PC19 pin
13MHz	Pull down	Left float
19.2MHz	Pull down	Pull down
26MHz	Left float	Pull down