Ingenic® JZ4750

Board Design Guide

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Ingenic JZ4750

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Release history

Date	Revision	Change
Jan. 2009	1.0	First release

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Content

1 Overview

JZ4750 is a Multimedia Applications Processor designed by INGENIC®, which addresses the Mobile, Multimedia, Low power requirement electronic product. JZ4750 integrates a high performance 32-bits CPU, support many Embedded Operating Systems such as Linux™, WinCE™, etc. It also integrates SDRAM memory controller, LCD controller, Audio Codec, Camera controller, multi-channel SAR-ADC, AC97/I2S controller, PCM interface, TS interface, TV encoder, MMC/ SD/SDIO host controller, high speed SPI, I2C, USB1.1 Host, USB2.0 Device, UART, IrDA, GPIO and so on.

1.1 Introduction

This design guide provides recommendations for system designs based on the JZ4750 processor. Design issues (e.g., thermal considerations) should be addressed using specific design guides or application notes for the processor.
The design guidelines in this document are used to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into two categories:

- **Design Recommendations:** Items based on INGENIC's simulations and lab experience to date are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations:** Suggestions for platform design provide one way to meet the design recommendations. Design considerations are based on the reference platforms designed by INGENIC. They should be used as an example, but may not be applicable to particular designs.

Note: In this manual, processor means the JZ4750 processor if not specified.

The guidelines recommended in this manual are based on experience and simulation work completed by INGENIC while developing systems with JZ4750. This work is ongoing, and the recommendations and considerations are subject to change.

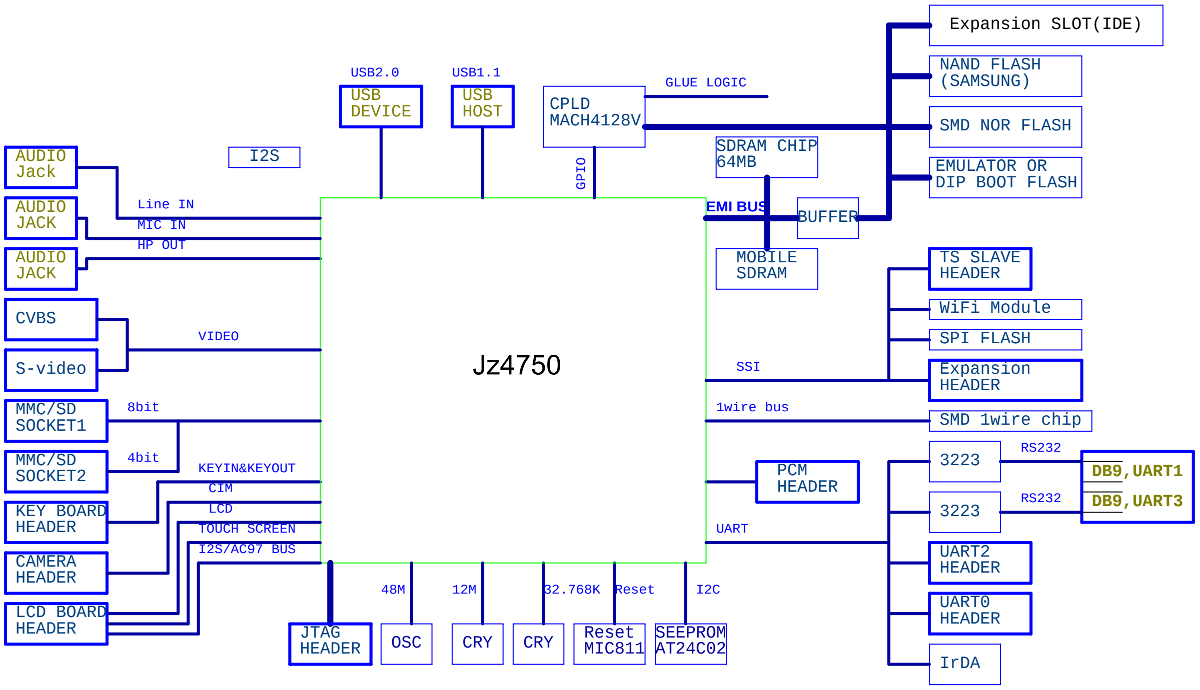
Platform schematics can be obtained and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics remain the same for most platforms. The schematic set provides a reference schematic for each platform component, and common system board options. Additional flexibility is possible through other permutations of these options and components.

The document can help customer span doorstep, design product using existent software and hardware resources. Your advice is the best encourage for us.

1.2 Reference Platform

Figure 1-1 shows the JZ4750 Development Board Architecture.

Figure 1-1 JZ4750 Development Board Architecture



2 Platform Stack-Up and Placement

In this section, an example of a JZ4750 platform component placement and stack-up is presented for a PMP product.

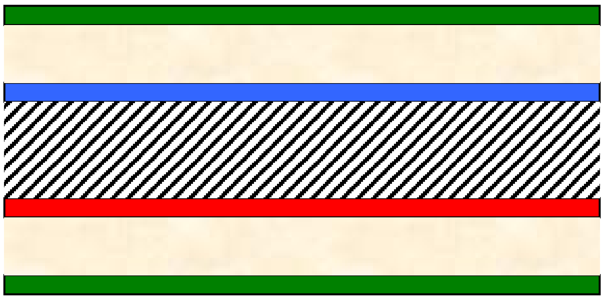
2.1 General Design Considerations

This section describes motherboard layout and routing guidelines for JZ4750 platforms. This section does not describe the function of any bus, or the layout guidelines for an add-in device. If the guidelines listed in this manual are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

The trace impedance typically noted (i.e., 56Ω ± 15%) is the nominal trace impedance for a 4-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time. Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in Figure 2-1

2.2 Nominal 4-Layer Board Stack-Up

The JZ4750 platform requires a board stack-up yielding a target board impedance of 56 Ω ± 15%. Recommendations in this design guide are based on the following a 4-layer board stack-up:



Signal	Layer 1
Prepreg	Layer 2
Ground	Layer 3
Core	Layer 4
Power	Layer 5
Prepreg	Layer 6
Signal	Layer 7
Total Thickness	62 mils.

Figure 2-1 4-layer PCB Stack-Up

Table 2-1 PCB Parameter

Description	Nominal Value	Tolerance	Comments
Board Impedance Z0	56Ω	± 15%	With nominal 4 mil trace width
Dielectric Thickness	4.3 mils	± 0.5 mils	1 x 2116 Pre-Preg
Micro-stripline Er	4.1	± 0.4	@ 100 MHz
Trace Width	4.0 mils	± 0.5 mils	Standard trace
Trace Thickness	2.1 mils	± 0.5 mils	0.5 oz foil + 1.0 oz plate
Soldermask Er	4.0	± 0.5	@ 100 MHz
Soldermask Thickness	1.0 mils	± 0.5 mils	From top of trace

2.3 PCB Technology Considerations

The following recommendation aids in the design of a JZ4750 based platform. Simulations and reference platform are based on the following technology, and we recommend that designers adhere to these guidelines.

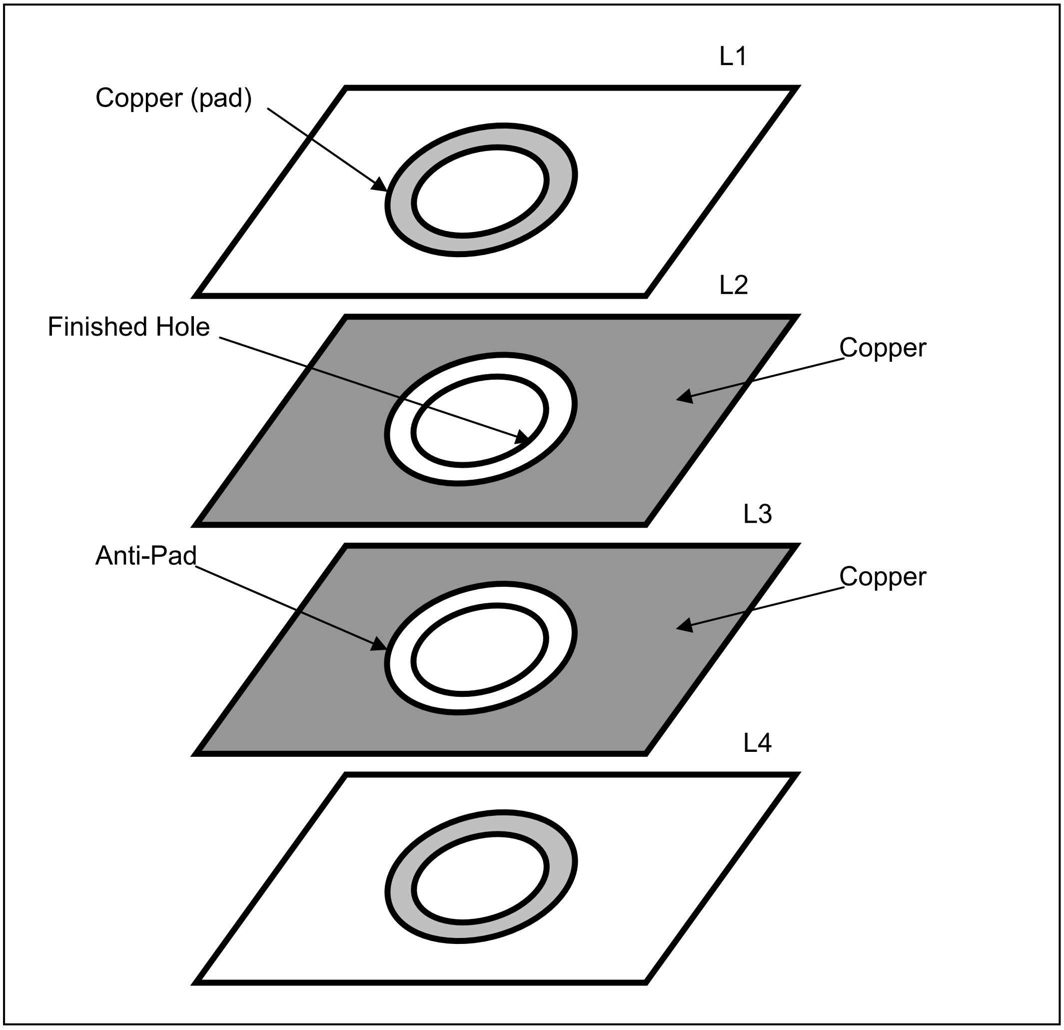


Figure 2-2 PCB Technologies – Stack-Up

Table 2-2 PCB Parameter for Vias

Number of Layers	
Stack Up	4 Layer
Cu Thickness	0.5 oz Outer (before plating); 1oz inner
Final Board Thickness	62 mils (- 5mils / +8mils)
Material	Fiberglass made of FR4
Signal and Power Via Stack	
Via Pad	26 mils
Via Anti-Pad	40 mils
Via Finished Hole	14 mils

3 External Memory Interface Design Guidelines

3.1 Overview

The External Memory Controller (EMC) divides the off-chip memory space and outputs control signals complying with specifications of various types of memory and bus interfaces. It enables the connection of static memory, NAND flash memory, synchronous DRAM, etc., to this processor.

This section is the design guidelines for the external memory interface.

3.2 Static Memory Interface

The static memory controller provides a glueless interface to ROM, Burst ROM, SRAM, NOR Flash and NAND Flash. It supports 4 chips selection CS4~1# and each bank can be configured separately. JZ4750 supports most types of NAND flashes, including SLC and MLC, 8-bit and 16-bit bus width, 512B, 2KB and 4KB page size. It also support boot from NAND flash. The data bus width for each chip select region may be programmed to be 8-bit, 16-bit or 32-bit.

3.2.1 Boot Memory

BOOT_SEL[1:0] pins define the boot time configurations as listed in the following table.

Table 3-1 Boot Configuration

BOOT_ SEL[1]	BOOT_ SEL[0]	Description
0	0	Boot from NOR flash or SPI (SPI0/CE0)
0	1	Boot from NAND flash: 512/2k/4k page size
1	0	Boot from SD card: MSC0
1	1	Boot from USB device

3.2.2 SRAM/Flash Memory Connection

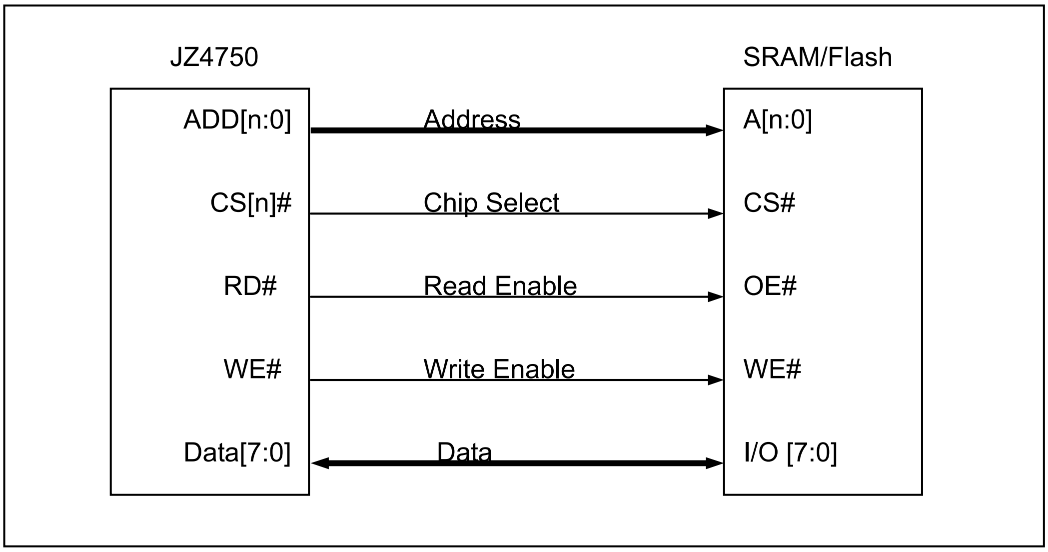


Figure 3-1 8-bit SRAM/Flash Interconnection Example

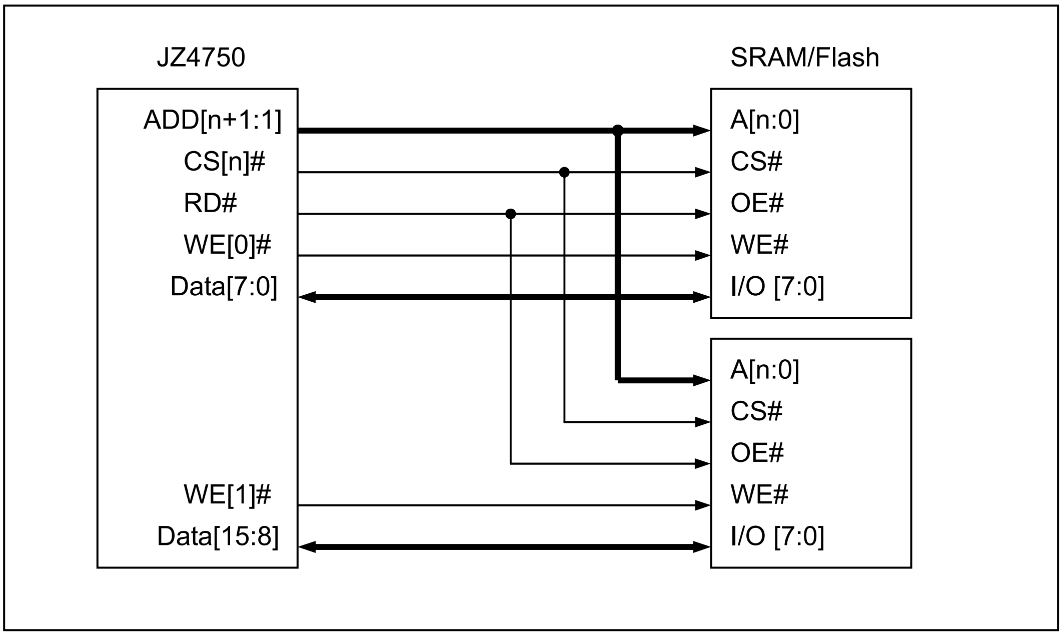


Figure 3-2 16-bit SRAM/Flash Interconnection Example

3.2.3 NAND Flash Connection

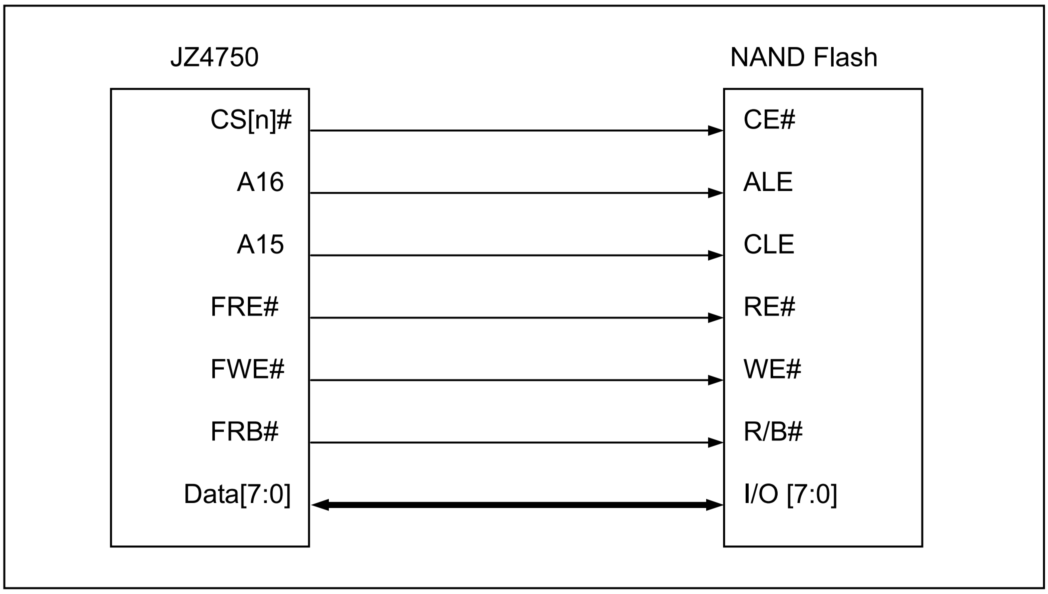


Figure 3-3 8-bit NAND Flash Interconnection Example

3.3 SDRAM

Following figure shows an example of connection of 512K x 16-bit x 2-bank synchronous DRAM.

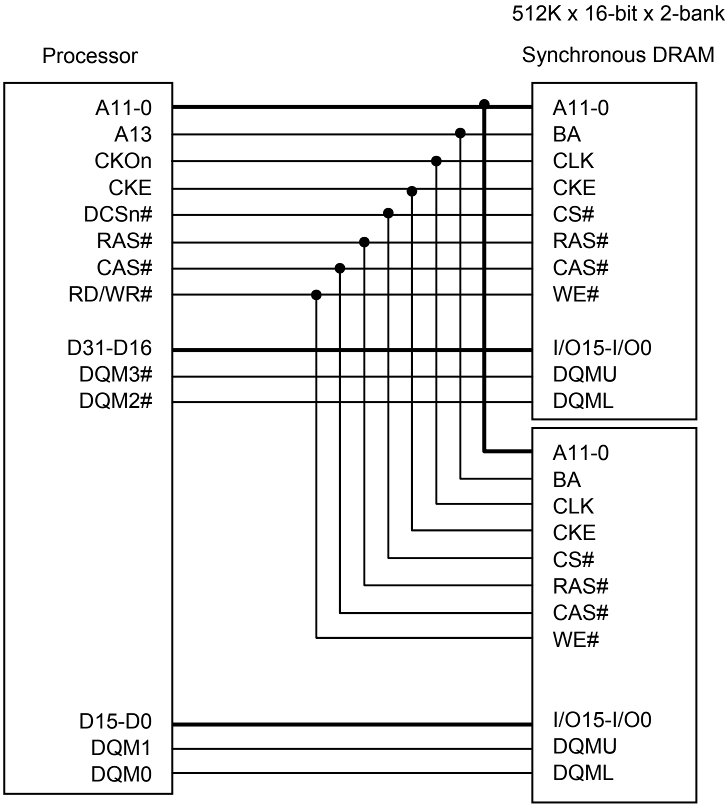


Figure 3-4 Example of Synchronous DRAM Chip Connection (1)

Following figure shows an example of connection of 1M x 16-bit x 4-bank synchronous DRAM.

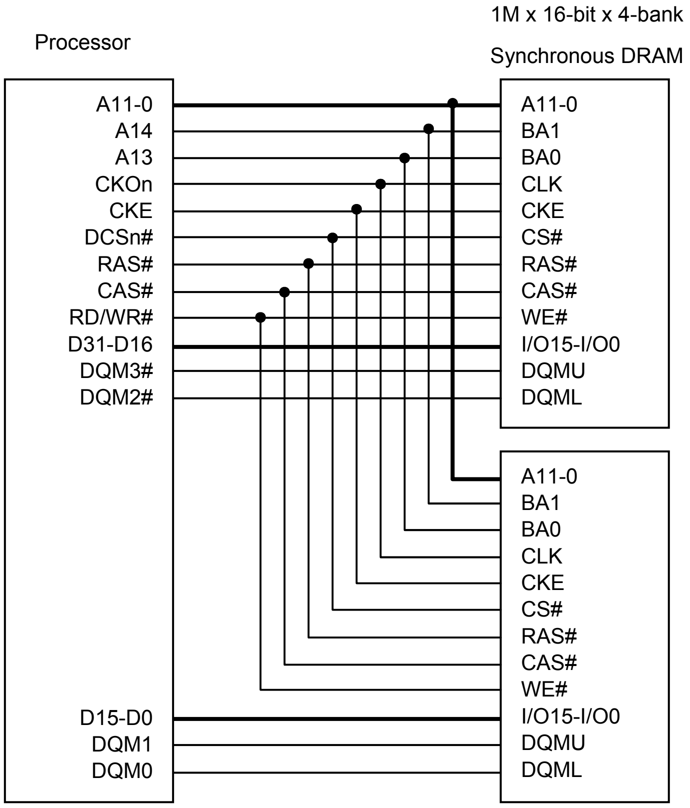


Figure 3-5 Example of Synchronous DRAM Chip Connection (2)

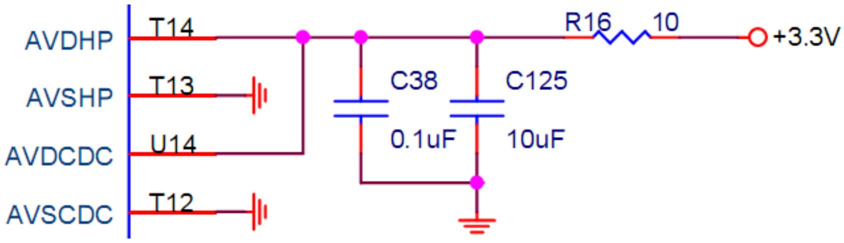
4 Audio Design Guidelines

The JZ4750 has an internal Audio Codec with 24 bits DAC and ADC.

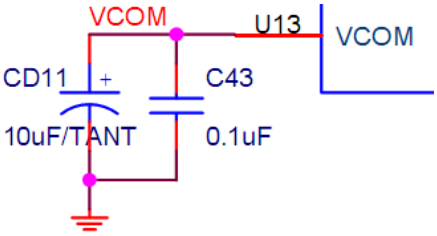
4.1 Audio Power

VDDHP and VDDCDC should be connected to a cleaned +3.3V power.

For a correct working, it is required to connect two decoupling capacitor (10μF and 100nF ceramic) between the pins AVDCDC and AVSCDC.



An electrolytic capacitor more than 10μF tantalum and a 0.1μF ceramic capacitor should be attached from VCOM to AVSCDC to eliminate the effects of high frequency noise.

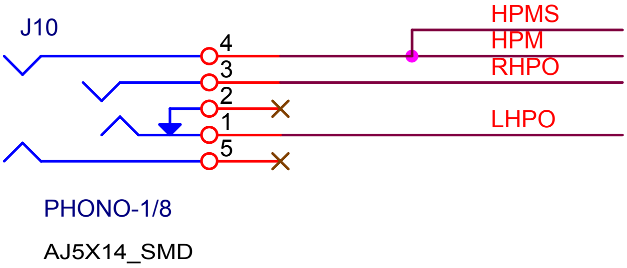


4.2 Headphone Out

The AOHPL and AOHPR pins are applied directly to the loads. The ground of the headphone is connected to AOHPM.

The DC value of the signal AOHPL or AOHPR equals to AVDCDC/2.

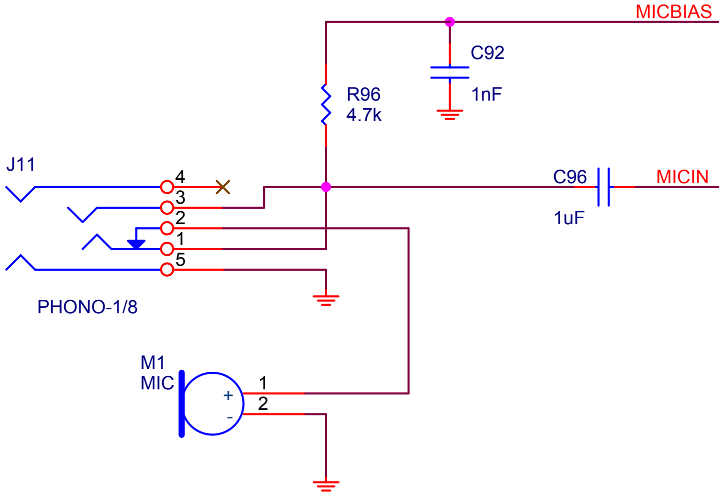
AOHPM and AOHPMS have to be connected together as close as possible of the headphone connector.



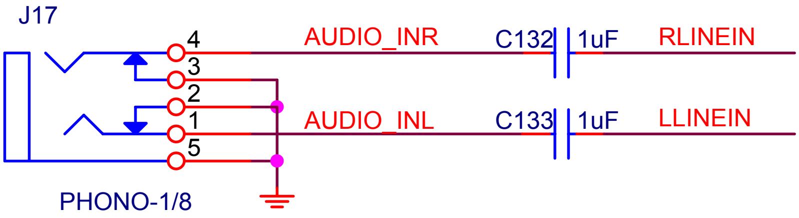
4.3 Mic In

The value of resistor R96 is commonly from 2.2 k Ohm to 4.7 k Ohm.

The 1nf decoupling capacitance removes high frequency noise of the chip.



4.4 Line In



4.5 Layout Guideline

To ensure the maximum performance of the Audio, proper component placement and routing techniques are required. These techniques include properly isolating associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and

voltage reference pins.

- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must not cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.

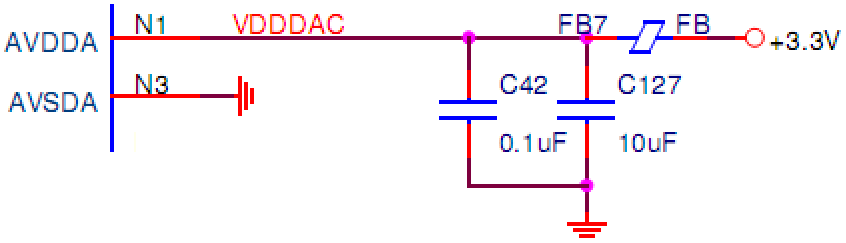
5 Video Design Guidelines

The TV Encoder enables the data for LCD panel showing in TV screen.

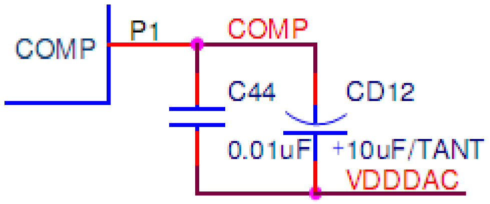
5.1 Video Power

VDDDAC should be connected to a cleaned +3.3V power.

For a correct working, it is required to connect two decoupling capacitor (10μF and 100nF ceramic) between the pins AVDDA and AVSDA.

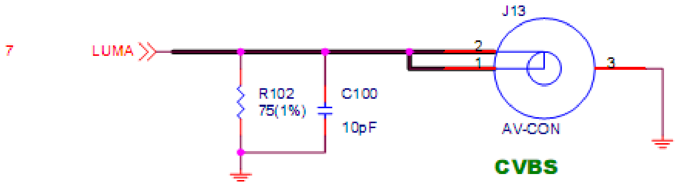


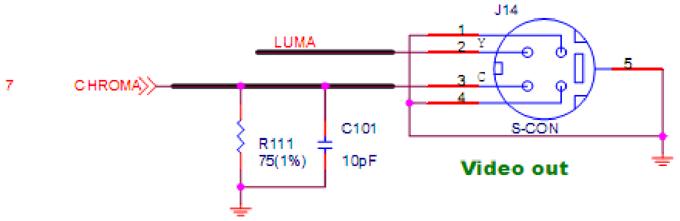
A tantalum capacitor more than 10μF and a 0.01μF ceramic capacitor should be attached from COMP to AVDDA externally



5.2 TV Out

It is required a 75 Ohm 1% pull-down resistors and a 10pF ceramic capacitor for both LUMA and CHROMA.





6 USB Design Guidelines

JZ4750 integrates USB Host Controller (UHC), which is Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible. It supports both low-speed (1.5 Mbps) and full-speed (12 Mbps) USB devices. Two downstream ports are provided.
JZ4750 also integrates USB device controller (UDC), which is USB Revision 2.0-compliant full-speed device.

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both D+/D- data lines.
- 15 Ω series resistors should be placed as close as possible to the JZ4750. These series resistors provide source termination of the reflected signal.
- 47-pF caps must be placed as close as possible to the JZ4750 as well as on the processor side of the series resistors on the USB data lines (D0±, D1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (D0±, D1±). They provide the signal termination required by the USB specification. The stub should be as short as possible.
- The trace impedance for the D0± and D1± signals should be 45 Ω (to ground) for each USB signal D+ or D-. This may be achieved with 9-mil-wide traces on the motherboard based on the stack-up recommended in Figure 5-1. The impedance is 90 Ω between the differential signal pairs D+ and D-, to match the 90 Ω USB twisted-pair cable impedance. Note that the twisted-pair characteristic impedance of 90 Ω is the series impedance of both wires, which results in an individual wire presenting 45Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as ‘critical signals’. (i.e., hand-routing preferred). The D+/D- signal pair should be routed together and not parallel to other signal traces, to minimize cross-talk. Doubling the space from the D+/D- signal pair to adjacent signal traces will help to prevent cross-talk. The D+/D- signal traces should also be the same length, which will minimize the effect of common mode current on EMI.

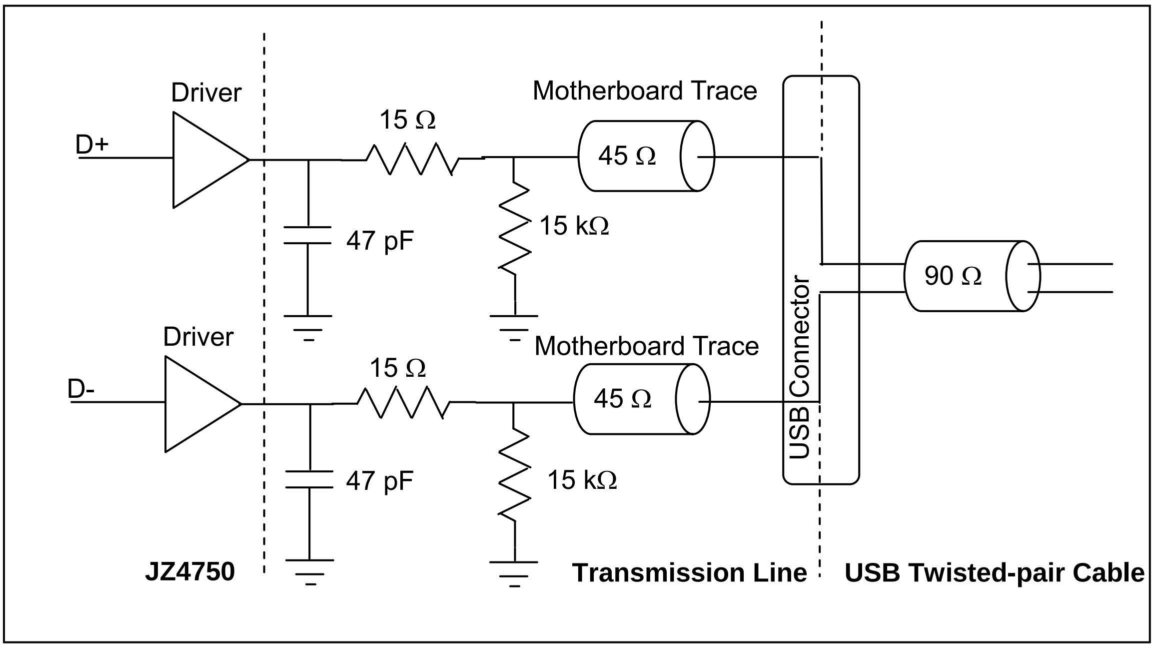


Figure 6-1 Recommend USB Host Schematic

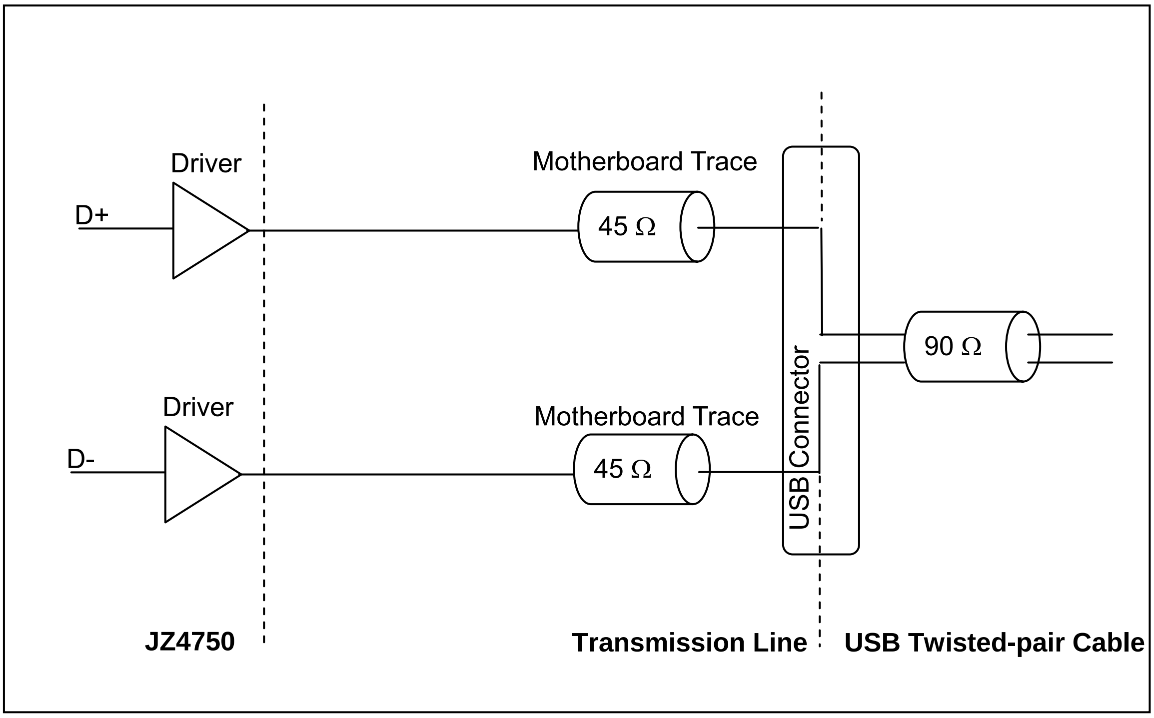


Figure 6-2 Recommend USB Device Schematic

7 LCD

The JZ4750 integrated LCD controller, which has the capabilities to driving the latest industry standard STN and TFT LCD panels. It also supports some special TFT panels used in consuming electronic products. The controller performs the basic memory based frame buffer and palette buffer to LCD panel data transfer through use of a dedicated DMA controller. Temporal dithering (frame rate modulation) is supported for STN LCD panels.
And OSD is also supported for LCD controller. (JZ4750)

Table 7-1 TFT Pin Mapping

JZ4750 Pin	8-bit Serial RGB	16-bit Parallel RGB	18-bit Parallel RGB	24-bit Parallel RGB	Smart LCD Serial	Smart LCD Parallel
LCD_PCLK/SLCD_CLK	CLK	CLK	CLK	CLK	CLK	
LCD_HSYNC/SLCD_RS	HSYNC	HSYNC	HSYNC	HSYNC		RS
LCD_VSYNC/SLCK_CS	VSYNC	VSYNC	VSYNC	VSYNC		CS
LCD_D17			R7	R7		D17
LCD_D16			R6	R6		D16
LCD_D15		R7	R5	R5	Data	D15
LCD_D14		R6	R4	R4		D14
LCD_D13		R5	R3	R3		D13
LCD_D12		R4	R2	R2		D12
LCD_D11		R3	G7	G7		D11
LCD_D10		G7	G6	G6		D10
LCD_D9		G6	G5	G5		D9
LCD_D8		G5	G4	G4		D8
LCD_D7	R7/G7/B7	G4	G3	G3		D7
LCD_D6	R6/G6/B6	G3	G2	G2		D6
LCD_D5	R5/G5/B5	G2	B7	B7		D5
LCD_D4	R4/G4/B4	B7	B6	B6		D4
LCD_D3	R3/G3/B3	B6	B5	B5		D3
LCD_D2	R2/G2/B2	B5	B4	B4		D2
LCD_D1	R1/G1/B1	B4	B3	B3		D1
LCD_D0	R0/G0/B0	B3	B2	B2		D0
LCD_DE	DE	DE	DE	DE		
LCD_PS/LCD_D_G1				G1		
LCD_CLS/LCD_D_R1				R1		
LCD_REV/LCD_D_B1				B1		

LCD_SPL/LCD_D_G0				G0		
UART3_CTS_N/LCD_D_R0				R0		
UART3_RTS_N/LCD_D_B0				B0		

8 Camera

The CIM (Camera Interface Module) of JZ4750 connects to a CMOS or CCD type image sensor. The CIM source the digital image stream through a common parallel digital protocol.

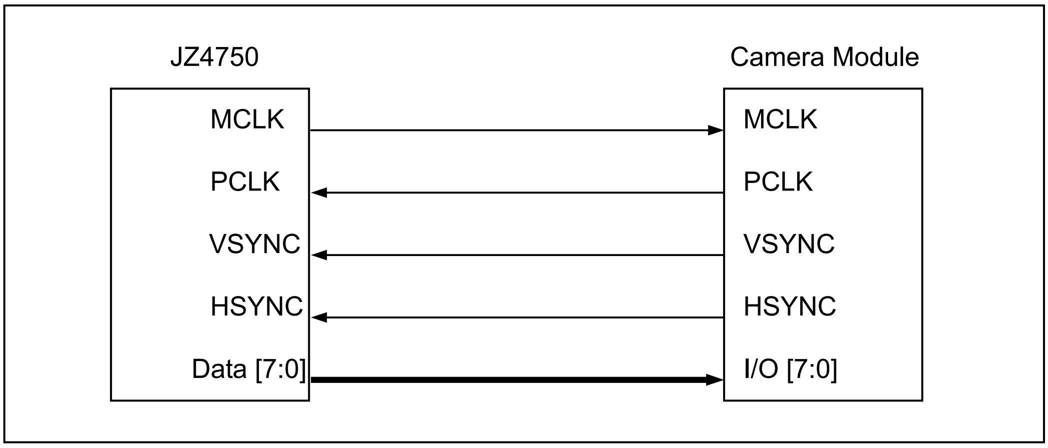


Figure 8-1 Example of Camera Module Interconnection

9 SAR A/D Controller

The A/D in JZ4750 is COMS low-power dissipation 12bit SAR analog to digital converter.

The SAR A/D Controller of JZ4750 can work at three different modes: Touch Screen (measure pen position and pen down pressure), Battery (check the battery power), and SADCIN (external ADC input).

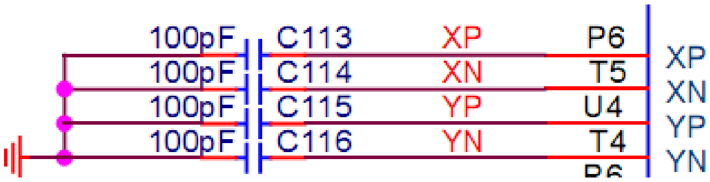
Table 9-1 SADC Pins Description

NAME	I/O	Description
XN	AI	Touch screen analog differential X- position input
YN	AI	Touch screen analog differential Y- position input
XP	AI	Touch screen analog differential X+ position input
YP	AI	Touch screen analog differential Y+ position input
ADIN0 (PBAT)	AI	Analog input for VBAT measurement (0~5V)
ADIN1 (SADCIN)	AI	External SAR-ADC input (0~V_{ADC})

9.1 Touch Screen

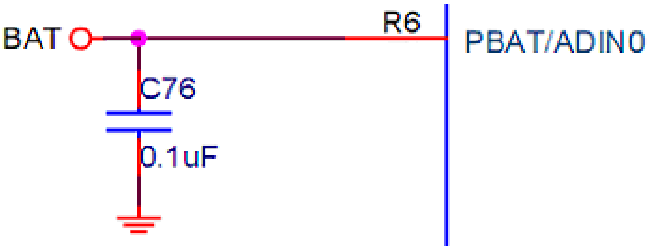
The JZ4750 can only support 4-wire resistive touch screen.

There is needed a decouple capacitor for every channel to avoid the crosstalk from LCD. The value is decided by the touch screen and can be from 100pF to 1000pF.



9.2 Battery Voltage Measurement

The battery voltage measurement can only use the ADIN0 channel. There is needed a decouple capacitor to avoid the crosstalk.



10 Ethernet Design Guidelines

The JZ4750 processor doesn't contain Ethernet media access controller (MAC). So we need an Ethernet controller that is external to the processor. This section describes design guidelines for the LAN on board based JZ4750.

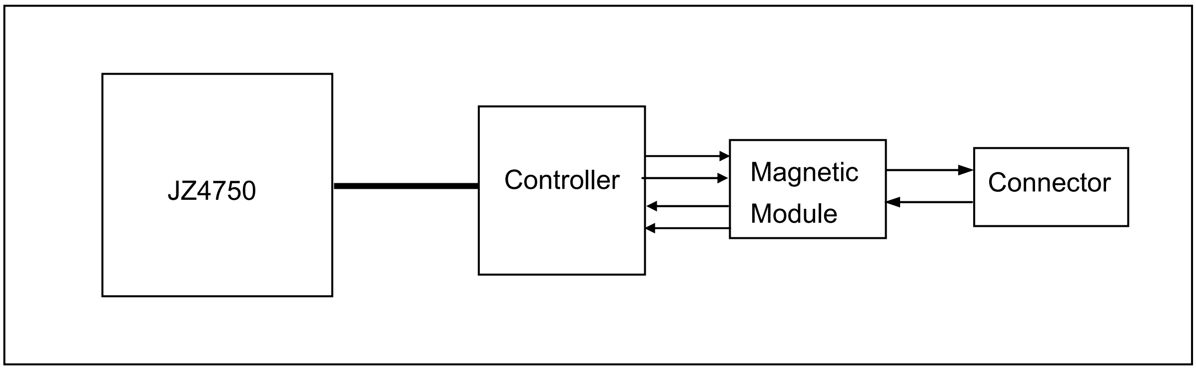


Figure 10-1 LAN On Board Implementation

10.1 JZ4750 Ethernet Controller Connection

JZ4750 Ethernet controller interconnection example is shown as figure 7-2, the Ethernet Controller chip maybe varied for specific OEM design targets. JZ4750 RESETOUT_ drive the RESET# input to reset the CONTROLLER chip when power-up.

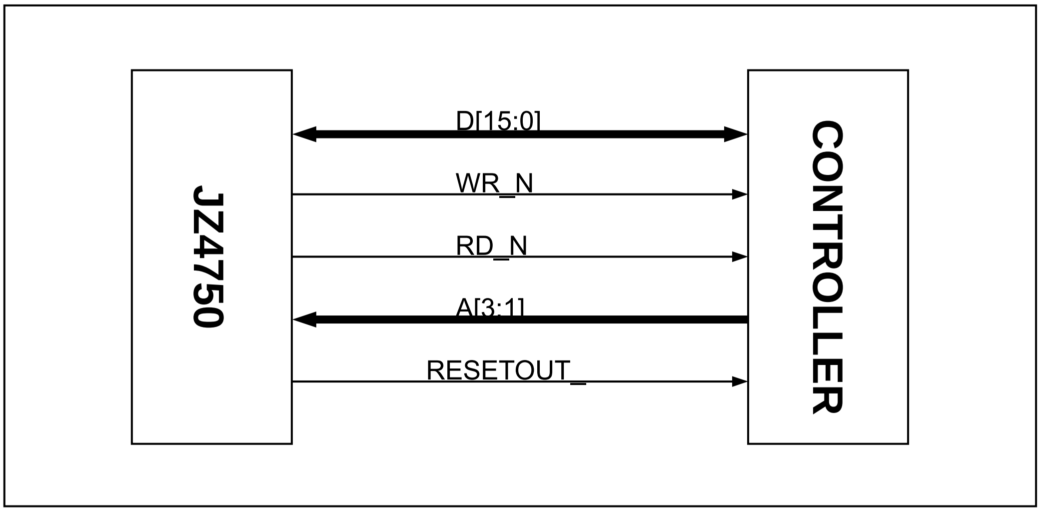


Figure 10-2 Controller Connection

11 RTC

The Real-Time Clock (RTC) unit can be operated in either chip main power is on or the main power is down but the RTC power is still on. In this case, the RTC power domain consumes only a few micro watts power.

The RTC contains a 32768Hz oscillator, a power-on-reset generator, the real time and alarm logic, and the power down and wakeup control logic.

The external WAKEUP_N pin is with up to 2s glitch filter / alarm wakeup.

11.1 RTC Clock

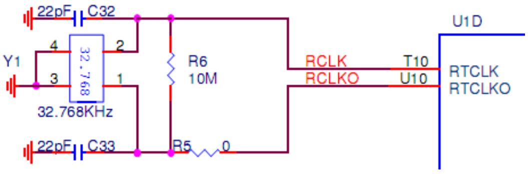


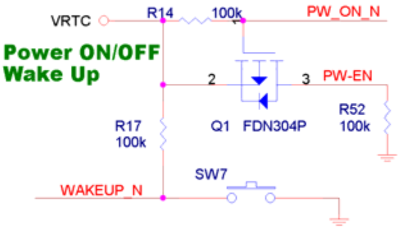
Table 11-1 RTC Clock Routing Summary

Trace Impedance	**Routing Requirements**	**Maximum Trace Length To Crystal**	**Signal Length Matching**	**R1, C1, and C2 Tolerances**	**Signal Referencing**
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R1 = 10M ± 5% C1=C2=33pF±10% The value of C1, C2 and R1 should be referred to the crystal's specification	Ground

11.2 Power Control

The following is the recommended circuit for the system power control.

PW_ON_N is an Open-Drain and active low signal from CPU. If the power circuit enable signal is active low signal, you can use the PW_ON_N directly. If the power circuit enable signal is active high signal, you can use the PW-EN signal. VRTC should be on always.



12 Miscellaneous Peripheral Design Guidelines

12.1 SSI Design Guideline

The SSI is a full-duplex synchronous serial interface and can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and other devices that use serial protocols for transferring data. The SSI supports National's Microwire, Texas Instruments Synchronous Serial Protocol (SSP), and Motorola's Serial Peripheral Interface (SPI) protocol.

The following figures show the connection example:

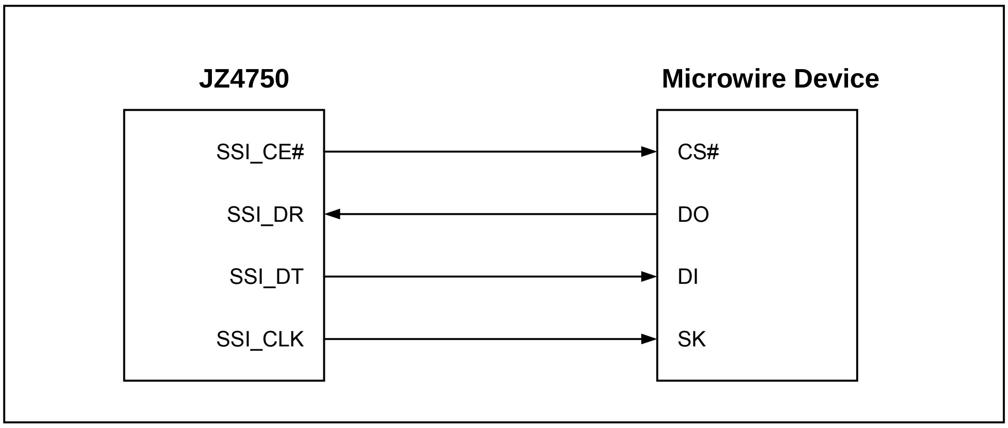


Figure 12-1 Microwire Interconnection

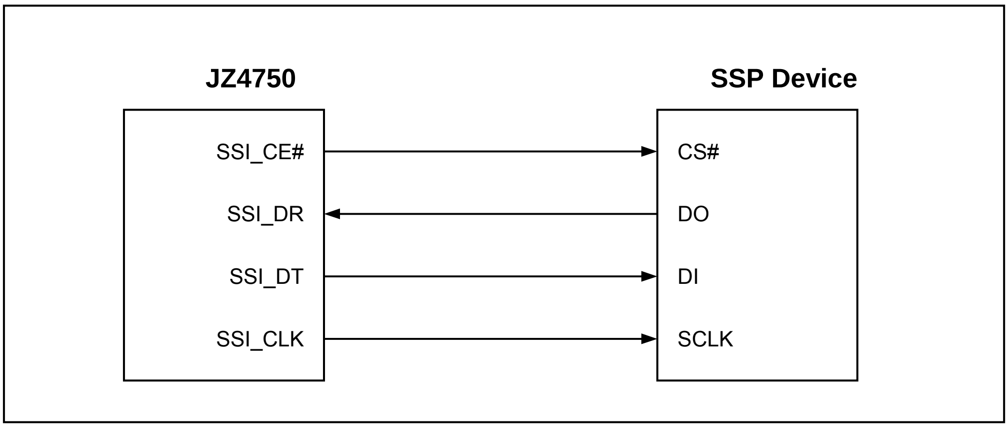


Figure 12-2 SSP Interconnection

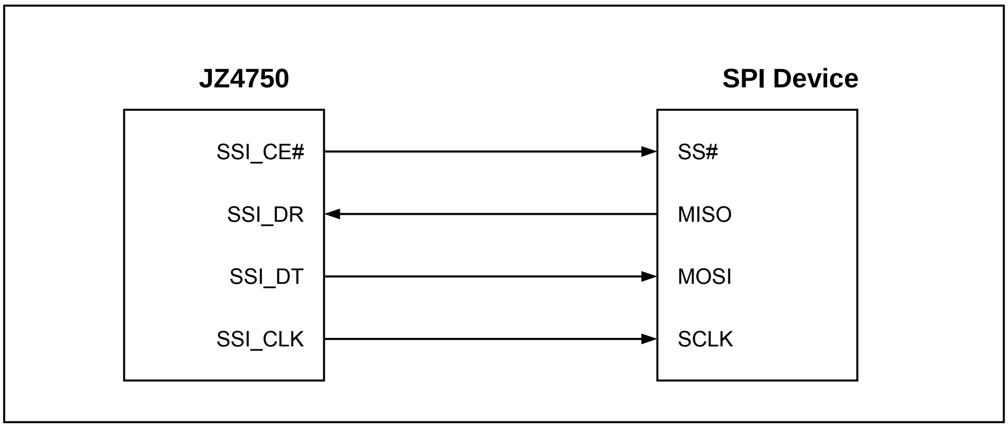


Figure 12-3 SPI Interconnection

12.2 UART/IrDA

The JZ4750 processor has four UARTs: All UARTs use the same programming model. Each of the serial ports can operate in interrupt based mode or DMA-based mode.

The Universal asynchronous receiver/transmitter (UART) is compatible with the 16550 industry standard and can be used as slow infrared asynchronous interface that conforms to the Infrared Data Association (IrDA) serial infrared specification 1.1.

12.2.1 UART Implementation

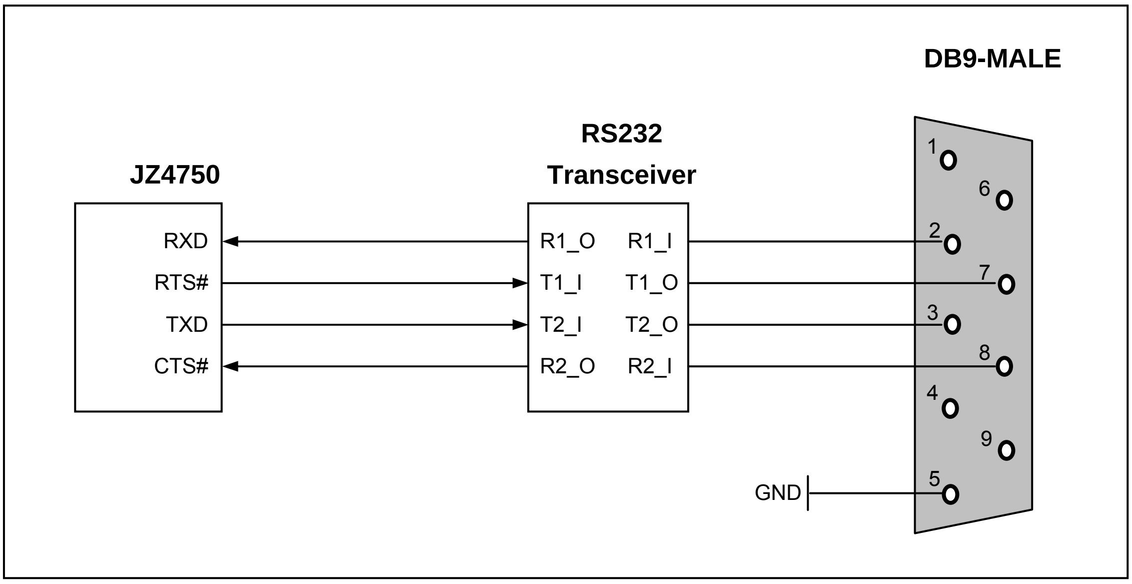


Figure 12-4 RS232 Serial Port Interconnection

12.2.2 IrDA Implementation

The Slow Infrared (SIR) interface is used with the UART to support two-way wireless communication that uses infrared transmission. The SIR provides a transmit encoder and receive decoder to support a physical link that conforms to the IrDA Serial Infrared Specification Version 1.1.

The SIR interface does not contain the actual IR LED driver or the receiver amplifier. The I/O pins attached to the SIR only have digital CMOS level signals. The SIR supports two-way communication, but full duplex communication is not possible because reflections from the transmit LED enter the receiver. The SIR interface supports frequencies up to 115.2 kbps.

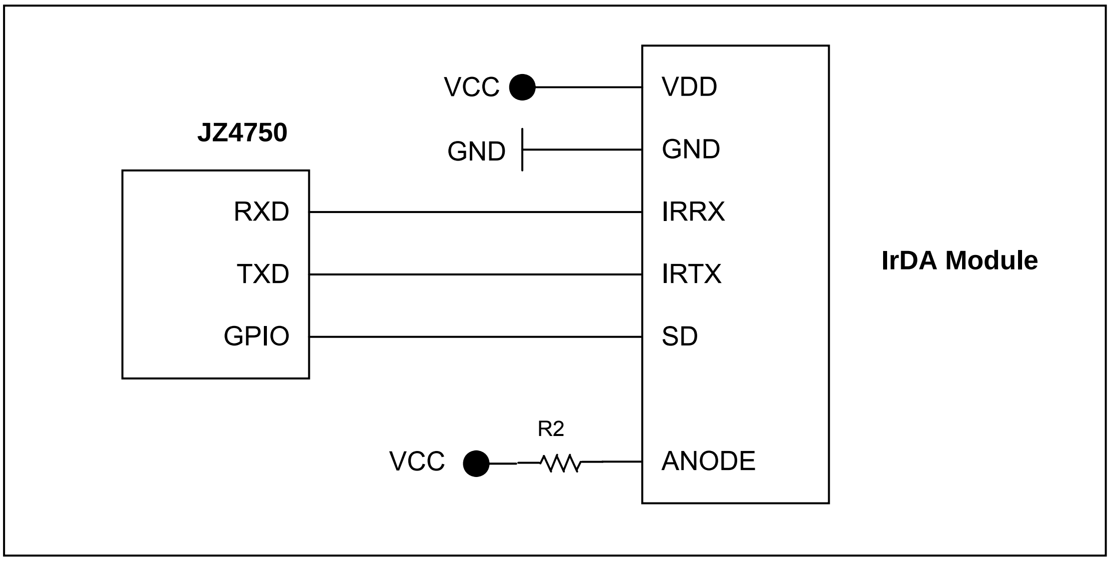


Figure 12-5 IrDA Port Interconnection

12.3 I2C Bus

The I2C bus was created by the Phillips Corporation and is a serial bus with a two-pin interface. The SDA data pin is used for input and output functions and the SCL clock pin is used to control and reference the I2C bus. The I2C bus requires a minimum amount of hardware to relay status and reliability information concerning the processor subsystem to an external device.

JZ4750 support single master mode only, so only slave devices are supported on the I2C bus attached to JZ4750. The I2C module supports I²C standard-mode and F/S-mode up to 400 kHz. The interface example is shown as following figure. The I2C bus serial operation uses an open-drain, wired-AND bus structure, so the pull-up (R1, R2=2.2K) is required on SCL and SDA. Refer to The I2C-Bus Specification for complete details on I2C bus operation.

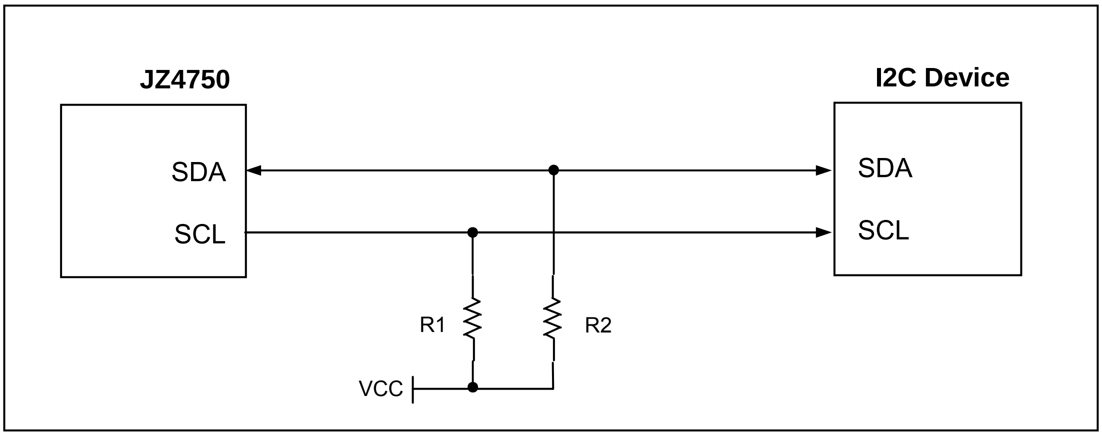


Figure 12-6 I2C Interconnection

12.4 PWM

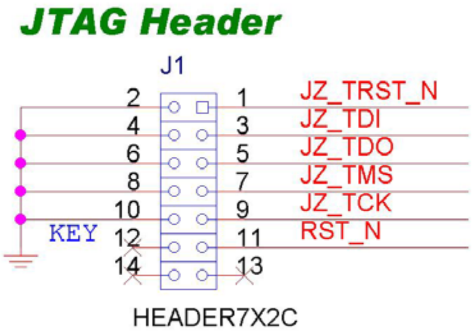
The Pulse Width Modulator (PWM) is used to control the back light inverter or adjust bright or contrast of LCD panel and also can be used to generate tone. PWM consists of a simple free-running counter with two compared registers, each compare register performs a particular task when it matches the count value. The period comparator causes the output pin to be set and the free-running counter to reset when it matches the period value. The width comparator causes the output pin to reset when the counter value matches. JZ4750 contains six pulse width modulators: PWM0 ~ PWM5.

12.5 GPIO

The JZ4750 processor provides 178 multiplexed General Purpose I/O Ports (GPIO) for use in generating and capturing application-specific input and output signals. Each port can be programmed as an output, an input or function port that serves certain peripheral. As input, pull up/down can be enabled/disabled for the port and the port also can be configured as level or edge tripped interrupt source.

12.6 JTAG/Debug Port

JZ4750 has a built-in JTAG/Debug port. All JTAG pins are directly connected. The following figure shows the connection of the JTAG port. Pin 11 RST_N should be connected to system reset circuit. Pin 12 is a KEY. The header should be a 7X2(2.54mm Pitch) male header with coat.



13 Platform Clock Guidelines

The JZ4750 processor contains one PLL driven by the 24-MHz oscillator and a clock generator from which the following are derived:

- CPU clock
- System bus clock
- Peripheral bus clock
- SDRAM bus clock
- Programmable clocks needed by certain peripherals

The following is the recommended circuit for main clock.

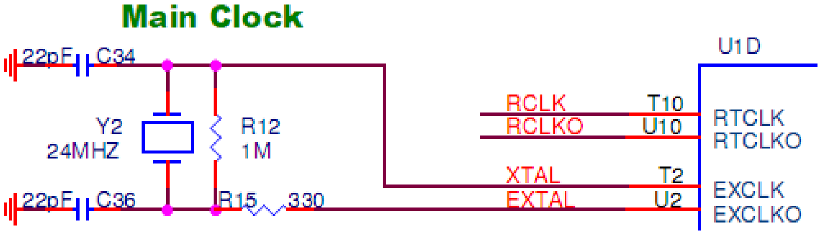
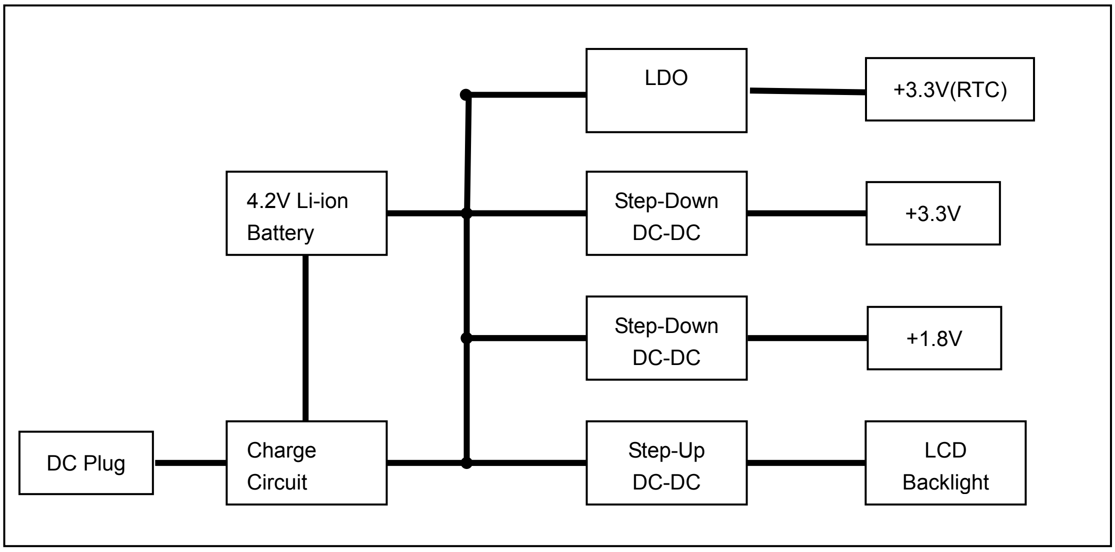


Table 13-1 Main Clock Routing Summary

Trace Impedance	Routing Requirements	Maximum Trace Length To Crystal	Signal Length Matching	R1, R2, C1, and C2 Tolerances	Signal Referencing
45 Ω to 69 Ω, 60 Ω Target	5 mil trace width (results in ~2pF per inch)	1 inch	NA	R1 = 1M ± 5% R2 = 330 ± 5% C1=C2=22pF±10% (Typical) The value of C1, C2 and R1 should be referred to the crystal's specification	Ground

14 Platform Power Guidelines

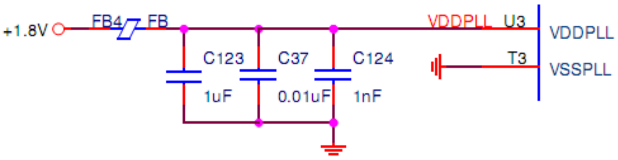
The JZ4750 processor needs two voltages: +3.3V for I/O and +1.8V for core. The following figure is a typical power circuit in the PMP application.



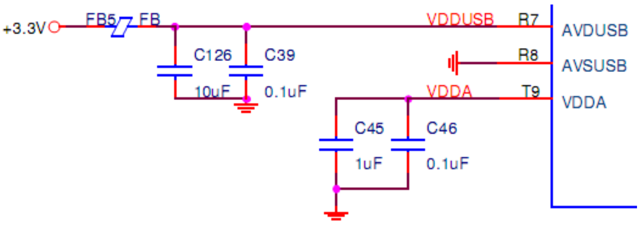
14.1 Power Delivery and Decoupling

The VDDIO (+3.3V) and VCORE (+1.8V) of JZ4750 should be decoupled with 0.1uF capacitor.

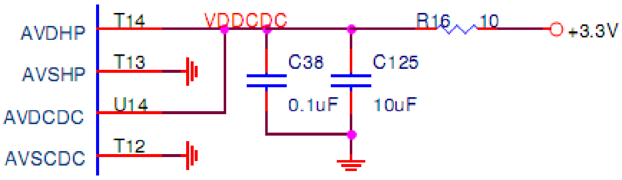
The Power of PLL should be as the following circuit.

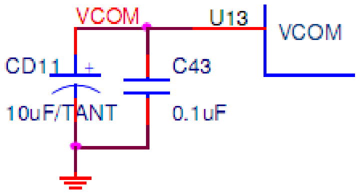


The power of USB should be as the following circuit.

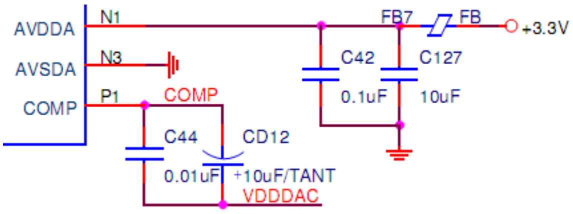


The power of Audio should be as the following circuit.

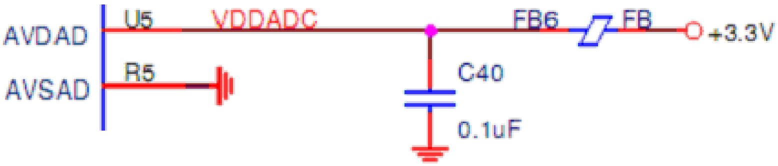




The power of DAC should be as the following circuit.



The power of ADC should be as the following circuit.



The power of RTC should be as the following circuit.

The capacitors should be placed near the Pin of power. The traces from capacitor to the Pin should be short and width.