Jz4740 Version-Mark vs Function

Revision History

Revision	Date	Author	Description
1.0	07-Jul-26	Zhang Jin	Original
1.1	07-Aug-15	Zhang Jin	SDRAM reset bug fix added “3.c)”
1.2	07-Nov-14	Zhang Jin	Add D version

1. Version & Mark

Version		Mark	Description
MPW		070307S0316A	
A0		070618S0621A	First 3 wafers of pilot run
A1		070910S0913A-A	The mark is to be decided. The remain wafers of pilot run
B-C		070927S1004A-B 071019S1025A-C 071019S1026A-CA 071019S1026A-CB 071019S1026A-CD 071019S1026A-CE 071019S1026A-CF 071019S1026A-CG 071019S1026A-CH 071019S1026A-CI 071019S1026A-CJ 071019S1026A-CK 071019S1026A-CL	The mark is to be decided
D			

2. Functions changed from version MPW to Version A0

a) **SSI**: Extend TFIFO and RFIFO from 16-level to 128-level, then update **SSICR1**.**TTRG** & **SSICR1.RTRG** from 2 bit to 4 bit, **SSISR.RFIFO_NUM** & **SSISR.TFIFO_NUM** from 5 bit to 8 bit.

b) **EMC**: remove ECC bug

c) **USB Device 2.0 PHY**: RREF should be connected to a 2.5k resistor and VDDA with a 1uf and a 0.1uf capacitors. Furthermore, PHY’s EOP timing was update so that it can run normally when it is inserted into jz4740 host.

d) **UART**: One UART port (UART1) added. UART1_RxD is multiplexed with UART0_CTS_; UART1_TxD is multiplexed with UART0_RTS_.

e) **DMAC**: remove a bug and add DMA for UART1

f) **CPM**: In spec, add clock divider register (**SSICDR)** for fast SSI clock, you may select 12M or fast SSI clock with **SSICDR.SCS** bit. Add uart1 clock gate in **CLKGR** register.

g) **SADC**:
In spec, Bit31: 30 are added and bit14: 13 are changed in Register **ADCFG**.

Bit31: The XdYdZmZn of the same point measure can be set to same or different.
Bit30, bit14 and bit13: Choose external driver or internal driver when sample.

h) **GPIO**: Interrupt flag is cleared by writing 1 to PDATC in MPW, to PDATS/PFLAGC now. UART1 GPIO added. Level interrupt can't be saved in register in now but can be saved in MPW.

i) **LCDC**: Bit7 is added and bit3:0 is changed in register **LCDCFG**. Bit7 is used to choose 16-bit parallel TFT LCD and 18-bit parallel TFT. Bit3:0-bit to choose the special or normal TFT for 16/18-bit parallel TFT.

LCD and SLCD Pin configure is changed as the following:
Old Pin configure:

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1				SLCD CS	SLCD CLK	SLCD RS			SLCD D [17:0]

New Pin configure:

LCDPIN	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN19	PIN18	PIN17-0
0	LCD PCLK	LCD VSYNC	LCD HSYNC	LCD DE	LCD REV	LCD PS	LCD CLS	LCD SPL	LCD D [17:0]
1	SLCD CLK	SLCD CS	SLCD RS						SLCD D [17:0]

j) **SLCD**: Bug removed . Old design will lose command/data when the freq of clock is to fast. New design will not lose command/data when the freq of clock is to fast.

k) TCU: spec not changed.

l) **AIC/CODEC**: Register: CDCCR1.SW2ON was reset to 1, is reset to 0.

m) **RTC-HIB**:

- HWCR register is changed, remains only one bit field: EALM. All other fields are removed
- A power-off detection circuit is added. When VDDHP is found power down, the chip enters hibernating mode automatically
- RTCCR.AE was not changed during reset, is reset to 0 by PPRST_ and HRST_
- RTCCR.RTCE was reset by PPRST_ only, is reset by both of PPRST_ and HRST_
- WKUP_ pin wakeup was valid in either high or low decided by register setting, is valid only in low
- PWRON_ was normal output pin, is open-drain output pin
- PPRST_ and WKUP_ were normal input pins, are Schmitt trigged input pins

- VDDRTC is changed from 3.3V to 1.8V. The high voltage of input signal PPRST_ and WKUP_ is changed as well (from 3.3V to 1.8V)

3. Functions changed from version A0 to Version A1

a) In A0 version, pins of GPD26, GPD27, GPD28 and GPD30 are output 0 during reset (PPRST_, Hibernating-reset and WDT-reset). In A1 version, these pins are input pull-up during reset

b) In A0 version, PBAT input signal voltage cannot be > VDDADC + 0.3V. In A1 version, PBAT signal voltage can be 5V.

c) In A0 version, the reset is not able to reset SDRAM chips since no proper CKO output. So the chip maybe dead when randomly press PPRST_ pin. In A1, CKO pin is reset to function.

4. Functions changed from version A1 to Version B-C

a) VDDRTC is changed from 1.8V to 3.3V. The high voltage of input signal PPRST_ and WKUP_ is changed as well (from 1.8V to 3.3V)

5. Functions changed from version B-C to Version D

a) ECC of NAND flash bug in Jz4720 is fixed

b) PWM5 can be used in sleep mode in RTCLK. To used it, register set/configure must be done when it chooses PCLK

c) USB1.1 host power/ground is connected to USB2.0 device power supply. So that USB1.1 power/ground pins may not be connected