JZ4725B

Mobile Application Processor

Data Sheet

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Disclaimer

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1 Overview

JZ4725B is a cost effective SOC solution for multimedia rich and mobile devices like video MP3, MP4 and PMP like products.

At the heart of JZ4725B is XBurst CPU core. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption.

The SIMD instruction set implemented by XBurst core, in together with the video post processing unit, provides RMVB, MPEG-1/2/4 decoding capability up to D1 resolution.

The memory interface of JZ4725B supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory and 4-bit/8-bit/12-bit ECC MLC NAND flash memory for cost sensitive applications.

On-chip modules such as LCD controller, audio CODEC, SAR-ADC and I2S controller offer designers a rich suite of peripherals for multimedia application. Other peripherals such as I2C, UART, USB 2.0 device controller, MMC/SD/SDIO host controller and general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

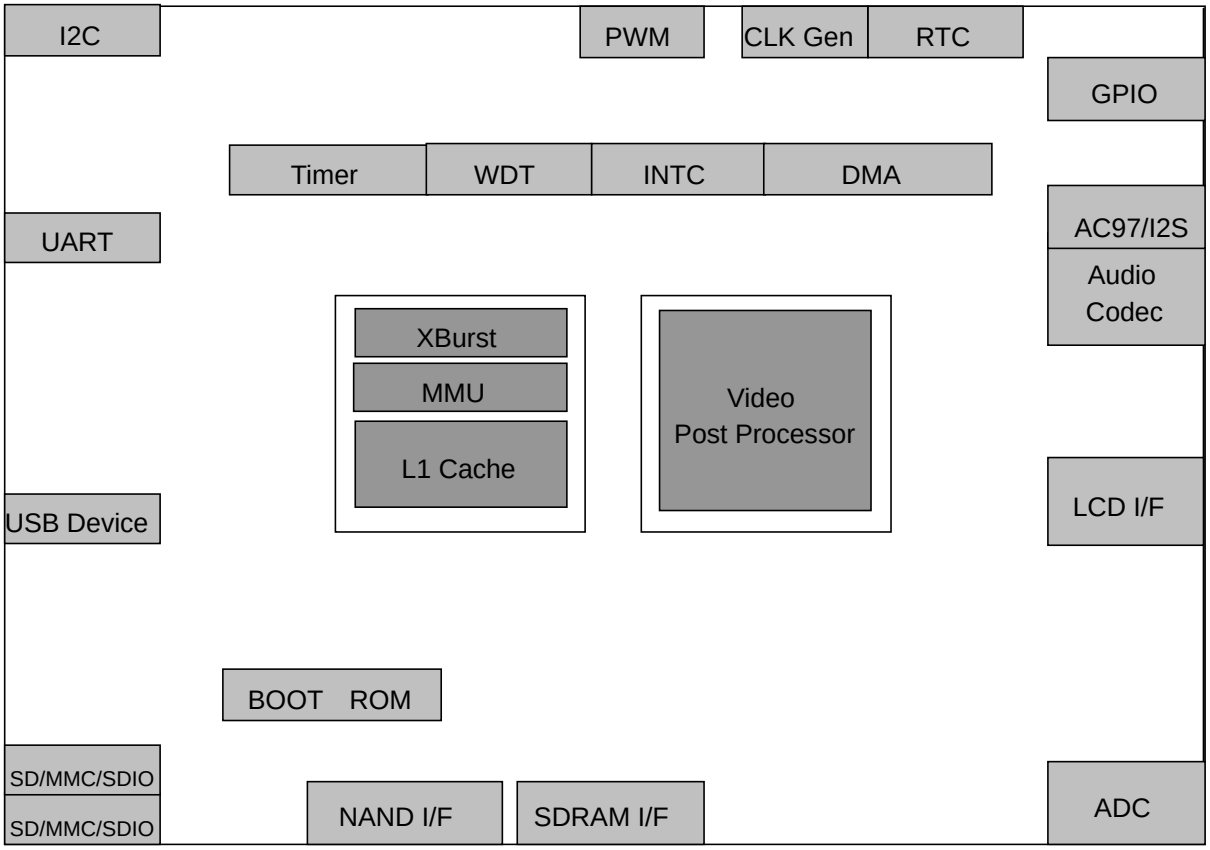


Figure 1-1 JZ4725B Diagram

1.2 Features

1.2.1 CPU Core

- XBurst CPU
  - XBurst® RISC instruction set to support Linux and WinCE
  - XBurst® SIMD instruction set to support multimedia acceleration
  - XBurst® 8-stage pipeline micro-architecture up to 360MHz
- MMU
  - 32-entry dual-pages joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- Cache
  - 16K instruction cache
  - 16K data cache
- Hardware debug support

1.2.2 Memory Sub-systems

- NAND flash interface
  - Support 4-bit/8-bit/12-bit MLC NAND as well as SLC NAND
  - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
  - Support automatic boot up from NAND Flash devices
- Synchronous DRAM interface
  - Standard SDRAM
  - 1 banks with programmable size and base address
  - 16-bit data bus width
  - Multiplexes row/column addresses according to SDRAM capacity
  - Two-bank or four-bank SDRAM is supported
  - Supports auto-refresh and self-refresh functions
  - Supports power-down mode to minimize the power consumption of SDRAM
  - Supports page mode
  - 1 Chip selects
- BCH controller
  - Implement data ECC encoding and decoding
- Direct memory access controller
  - Six independent DMA channels
  - Descriptor supported
  - Transfer data units: 8-bit, 16-bit, 32-bit, 16-byte or 32-byte
  - Transfer requests can be: auto-request within DMA; and on-chip peripheral module request
  - Interrupt on transfer completion or transfer error
  - Supports two transfer modes: single mode or block mode
  - External DMA supported

- The XBurst processor system supports little endian only

1.2.3 AHB Bus Arbiter

- Provide a fair chance for each AHB master to possess the AHB bus
- Fulfill the back-to-back feature of AHB protocol
- Divide two master groups with different privileges supports two arbitrating methods: Round-robin possession for masters in the same group, Preemptive possession for

1.2.4 masters with higher privileges System Devices

- Clock generation and power management
  - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
  - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
  - PLL on/off is programmable by software
  - ICLK, PCLK, SCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
  - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function.
- RTC (Real Time Clock)
  - 32-bit second counter
  - 1Hz from 32768hz
  - Alarm interrupt
  - Independent power
  - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
  - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports
  - Interrupt source and pending registers for software handling
  - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output
  - Provide five separate channels
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Six PWM outputs
- OS timer
  - One channel

- 32-bit counter and 32-bit compare register
- Support interrupt generation when the counter matches the compare register
- Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB
  Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- Watchdog timer
  - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Generate power-on reset

1.2.5 Audio/Display/UI Interfaces

- LCD controller
  - Single-panel display in active mode, and single- or dual-panel displays in passive mode
  - 2, 4, 16 grayscales and up to 4096 colors in STN mode
  - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
  - 24-bit data bus
  - Support 1,2,4,8 pins STN panel, 16bit, 18bit TFT and 8bit I/F TFT
  - Display size up to 1280×1024 pixels
  - 256×16 bits internal palette RAM
  - Support ITU601/656 data format
  - Support smart LCD (SRAM-like interface LCD module)
  - Support delta RGB
  - One single color background and two foreground OSD
- Image post processor
  - Video frame resize
  - Color space conversion: 420/444/422 YUV to RGB convert
- On-chip audio CODEC
  - 24-bit DAC, SNR: 90dB
  - 24-bit ADC, SNR: 85dB
  - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
  - L/R channels line input
  - MIC input
  - L/R channels headphone output amplifier support up to 16ohm load
  - Capacitor-coupled
- AC97/I2S controller
  - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
  - DMA transfer mode support
  - Support variable sample rate mode for AC-link format
  - Power down mode and two wake-up mode support for AC-link format
  - Programmable Interrupt function support
  - Support the on-chip CODEC
  - Support off-chip CODEC
- SADC

- 12-bit, 2Mbps, SNR@500kHz is 61dB, THD@500kHz is -71dB
- Battery voltage input
- 1 generic input channel

1.2.6 On-chip Peripherals

- General-Purpose I/O ports
  - Total 84 GPIOs.
  - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
  - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
  - Each pin can be configured as open-drain when output
  - Each pin can be configured as internal resistor pull-up
- I2C bus interface
  - Only supports single master mode
  - Supports I2C standard-mode and F/S-mode up to 400 kHz
  - Double-buffered for receiver and transmitter
  - Supports general call address and START byte format after START condition
- USB 2.0 device interface
  - Compliant with USB protocol revision 2.0
  - High speed and full speed supported
  - Embedded USB 2.0 PHY
- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Support automatic boot up from MSC0
  - 4-bit data bus on MSC0, 1-bit data bus on MSC1
  - Compliant with “The MultiMediaCard System Specification version 4.2”
  - Compliant with “SD Memory Card Specification version 2.0” and “SDIO Card Specification version 1.0” with 1 command channel and 4 data channels
  - Up to 320 Mbps data rate on MSC0, 80Mbps data rate on MSC1
  - Supports up to 10 cards (including one SD card)
  - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- UART
  - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
  - 32x8bit FIFO for transmit and 32x11bit FIFO for receive data
  - Interrupt support for transmit, receive (data ready or timeout), and line status
  - Supports DMA transfer mode
  - Provide complete serial port signal for modem control functions

- Support slow infrared asynchronous interface (IrDA)
- IrDA function up to 115200bps baudrate
- UART function up to 3.7Mbps baudrate
- Hardware flow control
- Only the TxD (transmit data) pin is available

1.2.7 Bootrom

- 4kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	0.16um CMOS
Power supply voltage	I/O: 3.3 ± 0.3V Core: 1.8 ± 0.2
Package	LQFP 128, 14mm x 14mm x 1.4mm, 0.4mm pitch
Operating frequency	360MHz

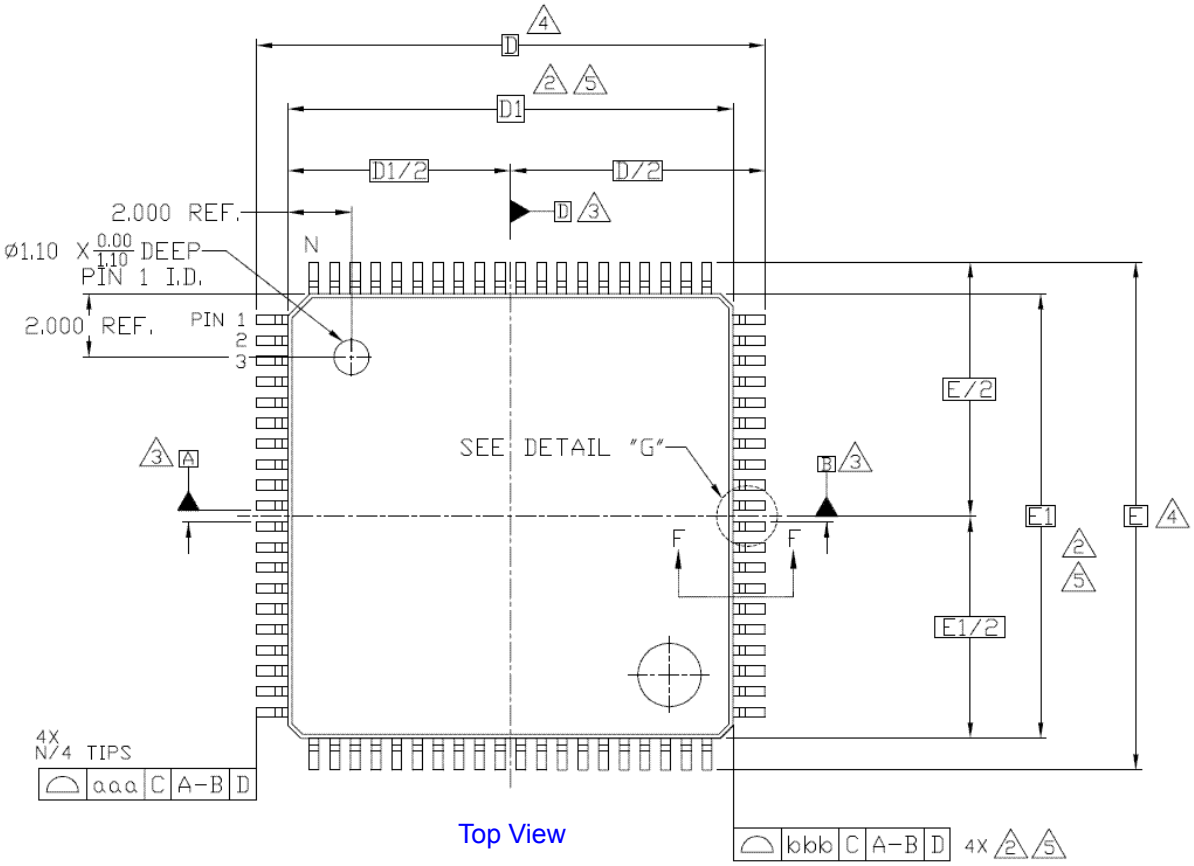
2 Packaging and Pinout Information

2.1 Overview

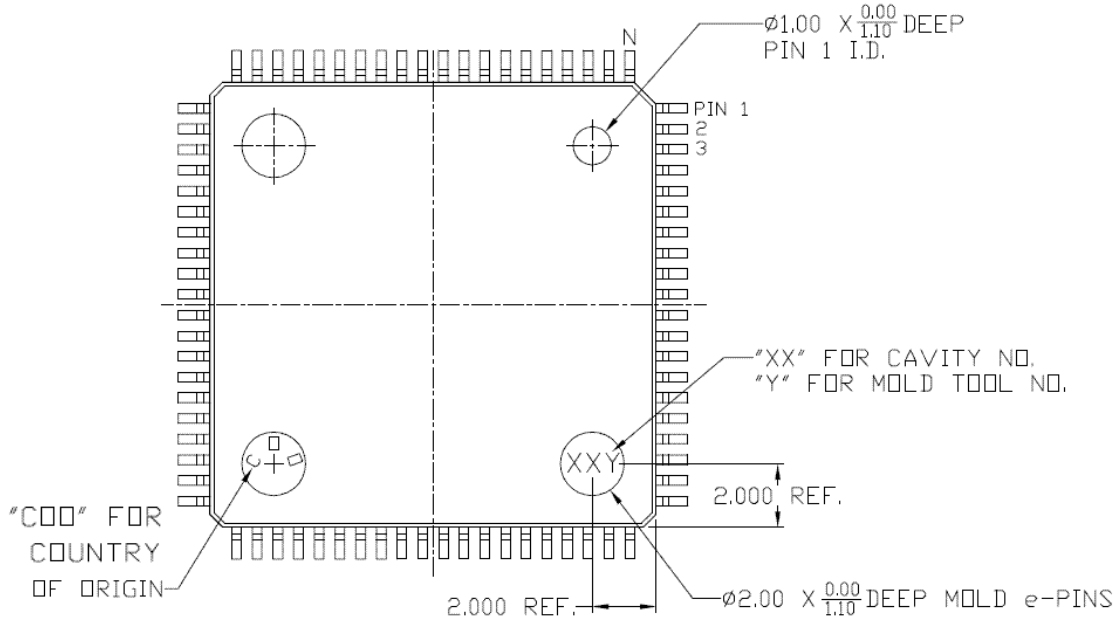
JZ4725B processor is offered in a LQFP128 package, which is 14mm x 14mm x 1.4mm outline 0.4mm pitch, show in “2.2 Package”.

The JZ4725B pin description is listed in Table 2-1 ~ Table 2-12.

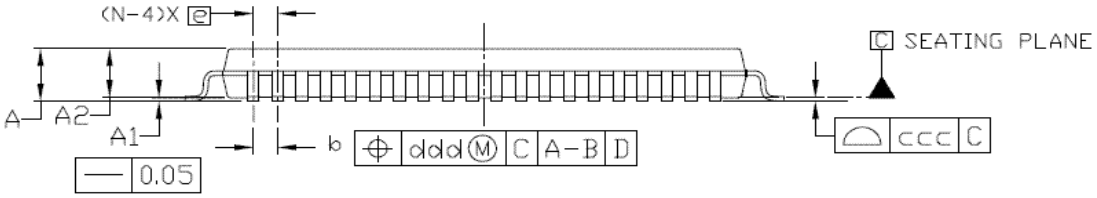
2.2 Package

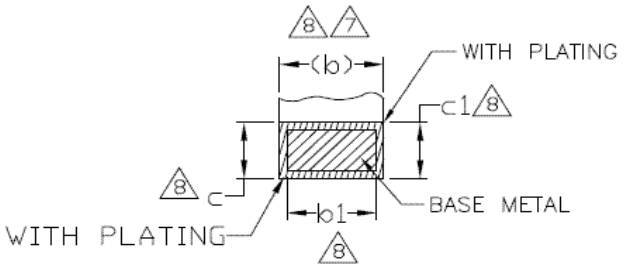


Top View

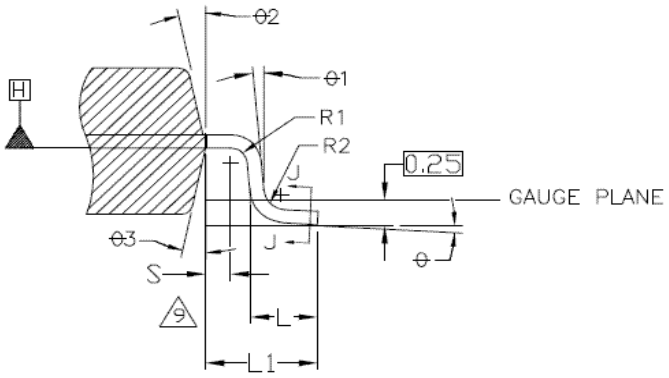


Bottom View

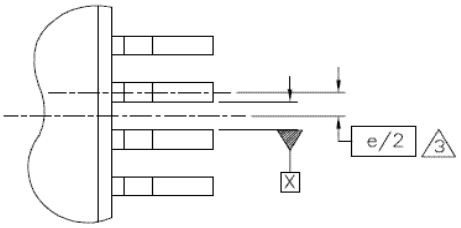




SECTION "J-J"
SCALE: NONE



SECTION "F-F"
SCALE: 3/1



EVEN LEAD SIDES
TOP VIEW

DETAIL "G"
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5-1994.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15 mm.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING DATUM PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 AND 0.5 mm PITCH PACKAGES.
8. THESE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
9. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
10. N IS THE MAXIMUM NUMBER OF LEADS.
11. THIS PRODUCT CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026 ISSUE D, VARIATIONS BEC AND BED..

SYMBOL		JEDEC VARIATIONS			NOTE
		BEC	BED		
b	MIN	0.22	0.17	0.13	
	NOM	0.32	0.22	0.18	
	MAX	0.38	0.27	0.23	
b1	MIN	0.22	0.17	0.13	
	NOM	0.30	0.20	0.16	8
	MAX	0.33	0.23	0.19	8
e		0.65 BSC	0.50 BSC	0.40 BSC	
N		80	100	128	
TOLERANCES OF FORM AND POSITION					
ccc		0.08	0.08	0.08	
ddd		0.13	0.08	0.07	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	--	--	1.60	
A1	0.05	--	0.15	9
A2	1.35	1.40	1.45	
D	16.00 BSC			
D1	14.00 BSC			
E	16.00 BSC			
E1	14.00 BSC			
θ	0°	3.5°	7°	
θ1	0°	5°	--	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
c	0.09	--	0.20	8
c1	0.09	0.127	0.16	8
L	0.45	0.60	0.75	
L1	1.00 REF.			
R1	0.08	--	--	
R2	0.08	--	0.20	
S	0.20	--	--	
TOLERANCES OF FORM AND POSITION				
aaa	0.20			
bbb	0.20			

2.3 Pin Description [1][2]

2.3.1 Pin for parallel interfaces

Table 2-1 EMC SDRAM Pins (39; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0 PA0	IO IO	40	12mA, pullup-pe	D0: SDRAM data bus bit 0, NAND/NOR/SRAM data bus bit 0 PA0: GPIO group A bit 0	VDDIO
D1 PA1	IO IO	41	12mA, pullup-pe	D1: SDRAM data bus bit 1, NAND/NOR/SRAM data bus bit 1 PA1: GPIO group A bit 1	VDDIO
D2 PA2	IO IO	42	12mA, pullup-pe	D2: SDRAM data bus bit 2, NAND/NOR/SRAM data bus bit 2 PA2: GPIO group A bit 2	VDDIO
D3 PA3	IO IO	43	12mA, pullup-pe	D3: SDRAM data bus bit 3, NAND/NOR/SRAM data bus bit 3 PA3: GPIO group A bit 3	VDDIO
D4 PA4	IO IO	44	12mA, pullup-pe	D4: SDRAM data bus bit 4, NAND/NOR/SRAM data bus bit 4 PA4: GPIO group A bit 4	VDDIO
D5 PA5	IO IO	45	12mA, pullup-pe	D5: SDRAM data bus bit 5, NAND/NOR/SRAM data bus bit 5 PA5: GPIO group A bit 5	VDDIO
D6 PA6	IO IO	46	12mA, pullup-pe	D6: SDRAM data bus bit 6, NAND/NOR/SRAM data bus bit 6 PA6: GPIO group A bit 6	VDDIO
D7 PA7	IO IO	47	12mA, pullup-pe	D7: SDRAM data bus bit 7, NAND/NOR/SRAM data bus bit 7 PA7: GPIO group A bit 7	VDDIO
D8 PA8	IO IO	32	12mA, pullup-pe	D8: SDRAM data bus bit 8, NAND/NOR/SRAM data bus bit 8 PA8: GPIO group A bit 8	VDDIO
D9 PA9	IO IO	33	12mA, pullup-pe	D9: SDRAM data bus bit 9, NAND/NOR/SRAM data bus bit 9 PA9: GPIO group A bit 9	VDDIO
D10 PA10	IO IO	34	12mA, pullup-pe	D10: SDRAM data bus bit 10, NAND/NOR/SRAM data bus bit 10 PA10: GPIO group A bit 10	VDDIO
D11 PA11	IO IO	35	12mA, pullup-pe	D11: SDRAM data bus bit 11, NAND/NOR/SRAM data bus bit 11 PA11: GPIO group A bit 11	VDDIO
D12 PA12	IO IO	36	12mA, pullup-pe	D12: SDRAM data bus bit 12, NAND/NOR/SRAM data bus bit 12 PA12: GPIO group A bit 12	VDDIO
D13 PA13	IO IO	37	12mA, pullup-pe	D13: SDRAM data bus bit 13, NAND/NOR/SRAM data bus bit 13 PA13: GPIO group A bit 13	VDDIO
D14 PA14	IO IO	38	12mA, pullup-pe	D14: SDRAM data bus bit 14, NAND/NOR/SRAM data bus bit 14 PA14: GPIO group A bit 14	VDDIO
D15 PA15	IO IO	39	12mA, pullup-pe	D15: SDRAM data bus bit 15, NAND/NOR/SRAM data bus bit 15 PA15: GPIO group A bit 15	VDDIO
A0 PB0	O IO	8	12mA, pullup-pe	A0: SDRAM address bus bit 0, NOR/SRAM address bus bit 0 PB0: GPIO group B bit 0	VDDIO
A1 PB1	O IO	7	12mA, pullup-pe	A1: SDRAM address bus bit 1, NOR/SRAM address bus bit 1 PB1: GPIO group B bit 1	VDDIO
A2 PB2	O IO	6	12mA, pullup-pe	A2: SDRAM address bus bit 2, NOR/SRAM address bus bit 2 PB2: GPIO group B bit 2	VDDIO
A3 PB3	O IO	5	12mA, pullup-pe	A3: SDRAM address bus bit 3, NOR/SRAM address bus bit 3 PB3: GPIO group B bit 3	VDDIO
A4 PB4	O IO	29	12mA, pullup-pe	A4: SDRAM address bus bit 4, NOR/SRAM address bus bit 4 PB4: GPIO group B bit 4	VDDIO
A5 PB5	O IO	28	12mA, pullup-pe	A5: SDRAM address bus bit 5, NOR/SRAM address bus bit 5 PB5: GPIO group B bit 5	VDDIO
A6 PB6	O IO	27	12mA, pullup-pe	A6: SDRAM address bus bit 6, NOR/SRAM address bus bit 6 PB6: GPIO group B bit 6	VDDIO
A7 PB7	O IO	26	12mA, pullup-pe	A7: SDRAM address bus bit 7, NOR/SRAM address bus bit 7 PB7: GPIO group B bit 7	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A8 PB8	O IO	23	12mA, pullup-pe	A8: SDRAM address bus bit 8, NOR/SRAM address bus bit 8 PB8: GPIO group B bit 8	VDDIO
A9 PB9	O IO	22	12mA, pullup-pe	A9: SDRAM address bus bit 9, NOR/SRAM address bus bit 9 PB9: GPIO group B bit 9	VDDIO
A10 PB10	O IO	9	12mA, pullup-pe	A10: SDRAM address bus bit 10, NOR/SRAM address bus bit 10 PB10: GPIO group B bit 10	VDDIO
A11 PB11	O IO	19	12mA, pullup-pe	A11: SDRAM address bus bit 11, NOR/SRAM address bus bit 11 PB11: GPIO group B bit 11	VDDIO
A12 PB12	O IO	18	12mA, pullup-pe	A12: SDRAM address bus bit 12, NOR/SRAM address bus bit 12 PB12: GPIO group B bit 12	VDDIO
A13 PB13	O IO	30	12mA, pullup-pe	A13: SDRAM address bus bit 13, NOR/SRAM address bus bit 13 PB13: GPIO group B bit 13	VDDIO
A14 PB14	O IO	31	12mA, pullup-pe	A14: SDRAM address bus bit 14, NOR/SRAM address bus bit 14 PB14: GPIO group B bit 14	VDDIO
DCS_ PB16	O IO	10	8mA, pullup-pe	DCS_: SDRAM chip select PB16: GPIO group B bit 16	VDDIO
RAS_ PB17	O IO	11	8mA, pullup-pe	RAS_: SDRAM row address strobe PB17: GPIO group B bit 17	VDDIO
CAS_ PB18	O IO	12	8mA, pullup-pe	CAS_: SDRAM column address strobe PB18: GPIO group B bit 18	VDDIO
SDWE_ & BUFD_ PB19	O IO	13	12mA, pullup-pe	SDWE_: SDRAM write enable BUFD_: Select CPU to SRAM chip direction in data bi-direction buffer PB19: GPIO group B bit 19	VDDIO
WE0_ PB20	O IO	14	8mA, pullup-pe	WE0_: SDRAM/NOR/SRAM byte 0 write enable PB20: GPIO group B bit 20	VDDIO
WE1_ PB21	O IO	15	8mA, pullup-pe	WE1_: SDRAM/NOR/SRAM byte 1 write enable PB21: GPIO group B bit 21	VDDIO
CKO PB24	O IO	16	12mA, pullup-pe	CKO: SDRAM clock PB24: GPIO group B bit 24	VDDIO
CKE PB25	O IO	17	8mA, pullup-pe	CKE: SDRAM clock enable PB25: GPIO group B bit 25	VDDIO

Table 2-2 NAND and MSC 0 Pins (8; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A15/CL MSC0_CLK PC8	O O IO	50	4mA, pullup-pe	A15/CL: NOR/SRAM address bit 15, used as NAND flash command latch MSC0_CLK: MSC (MMC/SD) 0 clock output PC8: GPIO group C bit 8	VDDIO
A16/AL MSC0_CM D PC9	O IO IO	49	4mA, pullup-pe	A16/AL: NOR/SRAM address bit 16, used as NAND flash address latch MSC0_CMD: MSC (MMC/SD) 0 command PC9: GPIO group C bit 9	VDDIO
WAIT_ PC20	I IO	54	2mA, pullup-pe	WAIT_: Slow static memory/device wait signal PC20: GPIO group C bit 20, reset to WAIT_	VDDIO
CS1_ PC21	O IO	56	2mA, pullup-pe	CS1_: NAND/NOR/SRAM chip select 1 PC21: GPIO group C bit 21	VDDIO
CS2_ MSC0_D3 PC22	O IO IO	55	4mA, pullup-pe	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 3 PC22: GPIO group C bit 22	VDDIO
PC27/FRB MSC0_D2	IO IO	53	4mA, pullup-pe	PC27/FRB: GPIO group C bit 27, used for NAND FRB (ready/busy) MSC0_D2: MSC (MMC/SD) 0 data bit 2	VDDIO
FRE_ MSC0_D0 PC28	O IO IO	52	4mA, pullup-pe	FRE_: NAND read enable MSC0_D0: MSC (MMC/SD) 0 data bit 0 PC28: GPIO group C bit 28	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
FWE_ MSC0_D1 PC29	O IO IO	51	4mA, pullup-pe	FWE_: NAND write enable MSC0_D1: MSC (MMC/SD) 0 data bit 1 PC29: GPIO group C bit 29	VDDIO

Table 2-3 LCDC Pins (26; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_REV LCD_B1 PD25	O O IO	105	4mA, pullup-pe	LCD_REV: LCD REV output for special TFT LCD_B1: Blue data bit 1, used in 24-bit data bus PD25: GPIO group D bit 25	VDDIO
LCD_B2 PD0	O IO	1	4mA, pullup-pe	LCD_B2: LCD blue data bit 2 PD0: GPIO group D bit 0	VDDIO
LCD_B3 PD1	O IO	128	4mA, pullup-pe	LCD_B3: LCD blue data bit 3 PD1: GPIO group D bit 1	VDDIO
LCD_B4 PD2	O IO	127	4mA, pullup-pe	LCD_B4: LCD blue data bit 4 PD2: GPIO group D bit 2	VDDIO
LCD_B5 PD3	O IO	126	4mA, pullup-pe	LCD_B5: LCD blue data bit 5 PD3: GPIO group D bit 3	VDDIO
LCD_B6 PD4	O IO	124	4mA, pullup-pe	LCD_B6: LCD blue data bit 6 PD4: GPIO group D bit 4	VDDIO
LCD_B7 PD5	O IO	123	4mA, pullup-pe	LCD_B7: LCD blue data bit 7 PD5: GPIO group D bit 5	VDDIO
LCD_SPL LCD_G0 PD23	O O IO	102	4mA, pullup-pe	LCD_SPL: LCD SPL output LCD_G0: Green data bit 0, used in 24-bit data bus PD23: GPIO group D bit 23	VDDIO
LCD_PS LCD_G1 PD24	O O IO	107	4mA, pullup-pe	LCD_PS: LCD PS output for special TFT LCD_G1: Green data bit 1, used in 24-bit data bus PD24: GPIO group D bit 24	VDDIO
LCD_G2 PD6	O IO	122	4mA, pullup-pe	LCD_G2: LCD green data bit 2 PD6: GPIO group D bit 6	VDDIO
LCD_G3 PD7	O IO	121	4mA, pullup-pe	LCD_G3: LCD green data bit 3 PD7: GPIO group D bit 7	VDDIO
LCD_G4 PD8	O IO	120	4mA, pullup-pe	LCD_G4: LCD green data bit 4 PD8: GPIO group D bit 8	VDDIO
LCD_G5 PD9	O IO	119	4mA, pullup-pe	LCD_G5: LCD green data bit 5 PD9: GPIO group D bit 9	VDDIO
LCD_G6 PD10	O IO	118	4mA, pullup-pe	LCD_G6: LCD green data bit 6 PD10: GPIO group D bit 10	VDDIO
LCD_G7 PD11	O IO	117	4mA, pullup-pe	LCD_G7: LCD green data bit 7 PD11: GPIO group D bit 11	VDDIO
LCD_CLS LCD_R1 PD22	O O IO	103	4mA, pullup-pe	LCD_CLS: LCD CLS output LCD_R1: Red data bit 1, used in 24-bit data bus PD22: GPIO group D bit 22	VDDIO
LCD_R2 PD12	O IO	116	4mA, pullup-pe	LCD_R2: LCD red data bit 2 PD12: GPIO group D bit 12	VDDIO
LCD_R3 PD13	O IO	115	4mA, pullup-pe	LCD_R3: LCD red data bit 3 PD13: GPIO group D bit 13	VDDIO
LCD_R4 PD14	O IO	114	4mA, pullup-pe	LCD_R4: LCD red data bit 4 PD14: GPIO group D bit 14	VDDIO
LCD_R5 PD15	O IO	113	4mA, pullup-pe	LCD_R5: LCD red data bit 5 PD15: GPIO group D bit 15	VDDIO
LCD_R6 PD16	O IO	112	4mA, pullup-pe	LCD_R6: LCD red data bit 6 PD16: GPIO group D bit 16	VDDIO
LCD_R7 PD17	O IO	111	4mA, pullup-pe	LCD_R7: LCD red data bit 7 PD17: GPIO group D bit 17	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_PCLK PD18	IO IO	2	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PD18: GPIO group D bit 18	VDDIO
LCD_HSYN PD19	IO IO	109	4mA, pullup-pe	LCD_HSYN: LCD line clock/horizontal sync PD19: GPIO group D bit 19	VDDIO
LCD_VSYN PD20	IO IO	108	4mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PD20: GPIO group D bit 20	VDDIO
LCD_DE PD21	O IO	110	4mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PD21: GPIO group D bit 21	VDDIO

2.3.2 Pin for serial interfaces

Table 2-4 MSC1 Pins (3; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_CLK PD26	O IO	62	4mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output PD26: GPIO group D bit 26	VDDIO
MSC1_CMD PD27	O IO	63	4mA, pullup-pe	MSC1_CMD: MSC (MMC/SD) 1 command PD27: GPIO group D bit 27	VDDIO
MSC1_D0 PD28	IO IO	61	4mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 PD28: GPIO group D bit 28	VDDIO

Table 2-5 UART, I2C and PWM Pins (5; all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 I2C_SDA PC10	O IO IO	60	4mA, pullup-pe	PWM0: PWM 0 output I2C_SDA: I2C serial data PC10: GPIO group C bit 10	VDDIO
PWM1 I2C_SCK PC11	O IO IO	59	4mA, pullup-pe	PWM1: PWM 1 output I2C_SCK: I2C serial clock PC11: GPIO group C bit 11	VDDIO
PWM2 UART_TxD PC12	O O IO	58	2mA, pullup-pe	PWM2: PWM 2 output UART_TxD: UART transmitting data PC12: GPIO group C bit 12	VDDIO
PWM3 UART_RxD PC13	O I IO	57	2mA, pullup-pe	PWM3: PWM 3 output UART_RxD: UART Receiving data PC13: GPIO group C bit 13	VDDIO
PWM5 PC15	O IO	48	2mA, pullup-pe	PWM5: PWM 5 output. It can run in sleep mode in RTCLK clock PC15: GPIO group C bit 15	VDDIO

2.3.3 Pin for system

Table 2-6 System Pins (2, all GPIO shared)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
BOOT_SEL0 PC30	I O	101	2mA, Schmitt	BOOT_SEL0: Boot select bit 0 PC30: GPIO group C bit 30	VDDIO
BOOT_SEL1 PC31	I IO	100	2mA, Schmitt	BOOT_SEL1: Boot select bit 1 PC31: GPIO group C bit 31	VDDIO

2.3.4 Pin for analog interfaces and corresponding power/ground

Table 2-7 Audio CODEC Pins (10)

Pin Names	IO	Loc	Pin Description	Power
AOHPL	AO	90	AOHPL: Left headphone out	AVD_{CDC}
AOHPR	AO	88	AOHPR: Right headphone out	AVD_{CDC}
MICIN	AI	99	MICIN: Microphone input	AVD_{CDC}
AIL	AI	97	AIL: Left line input	AVD_{CDC}
AIR	AI	98	AIR: Right line input	AVD_{CDC}
VCOM	AO	94	VCOM: Voltage Reference Output. An electrolytic capacitor more than 10μF in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise?	AVD_{CDC}
AVDHP	P	95	AVDHP: Headphone amplifier power, 3.3V (VDDAO, double PAD)	-
AVSHP	P	92	AVSHP: Headphone amplifier ground (VSSAO, double PAD)	-
AVDCDC	P	91	AVDCDC: CODEC analog power, 3.3V (AVDDA + VREFP)	-
AVSCDC	P	89	AVSCDC: CODEC analog ground (AVSSA + VREFN)	-

Table 2-8 USB device 2.0 Pins (6)

Pin Names	IO	Loc	Pin Description	Power
DP	AIO	79	DP: USB 2.0 device data plus	AVD_{USB}
DM	AIO	78	DM: USB 2.0 device data minus	AVD_{USB}
RREF	AIO	76	RREF: External Reference for USB 2.0 device. Connect a 10kΩ external reference resistor, with 1% tolerance to analog ground AVSUSB	AVD_{USB}
VDDA	AIO	75	VDDA: For USB 2.0 device. Connect a 0.1μF capacitor to analog ground AVSUSB	AVD_{USB}
AVDUSB	P	77	AVDUSB: USB analog power, 3.3V	-
AVSUSB	P	80	AVSUSB: USB analog ground	-

Table 2-9 SAR ADC Pins (4)

Pin Names	IO	Loc	Pin Description	Power
PBAT/ADIN0	AI	67	ADIN0: Battery voltage input or ADC general purpose input 0	AVD_{AD}
ADIN1	AI	68	ADIN1: ADC general purpose input 1	AVD_{AD}
AVDAD	P	70	AVDAD: ADC analog power, 3.3 V	-
AVSAD	P	69	AVDAD: ADC analog ground	-

Table 2-10 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	64	10~20 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
EXCLKO	AO	65		EXCLKO: OSC output	VDDIO
VDDPLL	P	71		VDDPLL: PLL analog power, 1.8V	-
VSSPLL	P	72		VSSPLL: PLL analog ground	-

Table 2-11 RTC Pins (6, 1 with GPIO input)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	81	32768Hz Oscillator	RTCLK: OSC input	VDD_{RTC}
RTCLKO	AO	82		RTCLKO: OSC output or 32768Hz clock input	VDD_{RTC}
PWRON_	O	86	~2mA, open-drain	PWRON_: Power on/off control of main power, low active	VDD_{RTC}
WKUP_ PB31	I I	85	Schmitt	WKUP_: Wakeup signal after main power down PB31: GPIO group B bit 31, input/interrupt only	VDD_{RTC}
PPRST_	I	84	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD_{RTC}
VDDRTC	P	83		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-

2.3.5 Pin for IO and core power/ground, and NC

Table 2-12 IO/Core power supplies plus NC Pins (10+5)

Pin Names	IO	Loc	Pin Description	Power
VDDIO	P	24 66 104	VDDIO: IO digital power, 3.3V	-
VSS	P	3 20 25 106 125	VSSIO: IO and/or CORE digital ground	-
VDDCORE	P	4 21	VDDCORE: CORE digital power, 1.8V	-
NC		73 74 87 93 96	NC: not connected	-

NOTES:

1 The meaning of phases in IO cell characteristics are:
   a 2/4/8/12mA out: The IO cell's output driving strength is about 2/4/8/12Ma.
   b Pull-up: The IO cell contains a pull-up resistor.
   c Pull-down: The IO cell contains a pull-down resistor.
   d Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
   e Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
   f Schmitt: The IO cell is Schmitt trig input.

2 For any GPIO shared pin except WAIT_/PC20 and CKO/PB24, the reset state is GPIO input with internal pull-up. The WAIT_/PC20 and CKO/PB24 are initialed to WAIT_ and CKO functions with internal pull-up.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDIO power supplies voltage	-0.5	4.6	V
AVDUSB power supplies voltage	-0.3	3.9	V
AVDCDC power supplies voltage	-0.3	4.0	V
AVDHP power supplies voltage	-0.3	4.0	V
AVDAD power supplies voltage	-0.3	4.0	V
VDDRTC power supplies voltage	-0.3	4.0	V
VDDcore power supplies voltage	-0.2	2.2	V
VDDPLL power supplies voltage	-0.5	2.5	V
Input voltage to VDDIO supplied non-supply pins	-0.5	4.6	V
Input voltage to AVDUSB supplied non-supply pins	-0.5	5.0	V
Input voltage to AVDAD supplied non-supply pins except PBAT	-0.5	4.0	V
Input voltage of PBAT	-0.5	6.0	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	4.0	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDIO supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDUSB supplied non-supply pins	-0.5	5.0	V
Output voltage from AVDAD supplied non-supply pins	-0.5	4.0	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	4.0	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	4.0	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{IO}	VDDIO voltage	2.97	3.3	3.63	V
V_{USB}	AVDUSB voltage	3.0	3.3	3.6	V
V_{CDC}	AVDCDC voltage	3.0	3.3	3.6	V
V_{HP}	AVDHP voltage	3.0	3.3	3.6	V
V_{ADC}	AVDAD voltage	3.0	3.3	3.6	V
V_{RTC}	VDDRTC voltage	3.0	3.3	3.6	V
V_{CORE}	VDDcore voltage	1.62	1.8	1.98	V
V_{PLL}	VDDPLL analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH-IO}	Input high voltage	2.0		3.6	V
V_{IL-IO}	Input low voltage	-0.3		0.8	V

Table 3-4 Recommended operating conditions for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{I-UF}	Input voltage range for full speed applications	0		V_{USB}	V
V_{I-UH}	Input voltage range for high speed applications	120		400	mV

Table 3-5 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
$V_{I-PBAT1}$	PBAT input voltage range when measuring low voltage battery	0		2.5	V
$V_{I-PBAT2}$	PBAT input voltage range when measuring high voltage battery	0		5	V
$V_{I-ADIN1}$	ADIN1 input low voltage range	0		V_{ADC}	V

Table 3-6 Recommended operating conditions for AVDCDC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
$V_{ILH-CDC}$	Input voltage range	0		V_{CDC}	V

Table 3-7 Recommended operating conditions for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit

V_{IH-RTC}	Input high voltage	2.0		3.6	V
V_{IL-RTC}	Input low voltage	-0.3		0.8	V

Table 3-8 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-9 DC characteristics for VDDIO supplied pins

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.46	1.59	1.75	V
V_{T+}	Schmitt trig low to high threshold point		1.44	1.50	1.56	V
V_{T-}	Schmitt trig high to low threshold point		0.88	0.94	0.99	V
I_L	Input Leakage Current				±10	μA
I_{OZ-IO}	Tri-State output leakage current				±10	μA
R_{PU}	Pull-up Resistor		50	65	100	kΩ
R_{PD}	Pull-down Resistor		40	56	107	kΩ
C_{IO}	Capacitance of the pins		4	5	10	pF
V_{OL-IO}	Output low voltage @I_{OL-IO}=2, 4, 8, 12mA				0.4	V
V_{OH-IO}	Output high voltage @I_{OH-IO}=2, 4, 8, 12mA		2.4			V
I_{OL-IO}	Low level output current @ V_{OL-IO} = 0.4V for cells of	2mA	2.2	3.7	4.6	mA
		4mA	4.4	7.4	9.2	mA
		8mA	8.9	14.7	18.4	mA
		12mA	13.3	22.1	27.5	mA
I_{OH-IO}	High level output current @ V_{OH-IO} = 2.4V for cells of	2mA	2.5	5.1	7.9	mA
		4mA	5.0	10.2	15.9	mA
		8mA	10.0	20.4	31.7	mA
		12mA	15.0	30.6	47.6	mA

Table 3-10 DC characteristics for USB 2.0 Device DP/DM pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-U20}	Output high voltage	1.5		V_{USB}	V
V_{OL-U20}	Output low voltage	0		0.4	V

Table 3-11 DC characteristics for ADC pins

Symbol	Description	Min	Typical	Max	Unit
V_{OH-ADC}	XN/XP/YN/YP output high voltage	0.9 * V_{ADC}		V_{ADC}	V
V_{OL-ADC}	XN/XP/YN/YP output low voltage	0		0.1 * V_{ADC}	V
R_{BAT}	BAT input resister		9.3		kΩ
R_{PDADC}	Internal pull down resister		10.4		kΩ

Table 3-12 DC characteristics for VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{OH-RTC}	Output high voltage	2.0		3.6	V
V_{OL-RTC}	Output low voltage	-0.3		0.8	V

3.4 Power Consumption Specifications

Power consumption depends on the operating frequency, operating voltage, program used which determines internal and external switching activities, external loading and even environment ambient. The typical power consumption of both dynamic and static for the Jz4740 processor are provided here.

Table 3-13 PLL (VDD_{PLL}) Dynamic Power Consumption

Conditions	PLL out	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL input clock = 12MHz	240MHz	TBD	mA
	360MHz	TBD	mA

Table 3-14 PLL (VDD_{PLL}) Static Power Consumption

Conditions	Typical	Unit
VDDPLL = 1.8V, Temperature = room, PLL is in suspend mode	TBD	uA

Table 3-15 RTC (VDD_{RTC}) Dynamic Power Consumption

Conditions	Typical	Unit
VDDRTC = 3.3V, RTCLK = 32768Hz oscillator, Temperature = room	TBD	uA

Table 3-16 IO (VDD_{IO}) Dynamic Power Consumption

Conditions	SDRAM Clock	Typical	Unit
VDDIO = VDDIOL = 3.3V, VDDcore = 1.8V, Temperature = room, 32-bit SDRAM, CIM is not run, LCD run in 480 x 272 x 60, EXCLK = 12MHz oscillator, CPU clock is 3 times of SDRAM clock, run GCC or media program in Linux	80MHz	TBD	mA
	120MHz	TBD	mA

NOTE: IO dynamic power is greatly depends on the software environment and the hardware (board and other components) environment.

Table 3-17 IO (VDD_{IO}) Static Power Consumption

Conditions	Typical	Unit
VDDIO = VDDIOL = 3.3V, VDDcore = 1.8V, Temperature = room, oscillator stopped, No input floating, the pull-up/down is in same direction as the driving	TBD	uA

Table 3-18 CORE (VDD_{CORE}) Dynamic Power Consumption

Conditions	CPU Clock	Typical	Unit

VDDcore = 1.8V, Temperature = room, 32-bit SDRAM, CIM is not run, LCD run in 480 x 272 x 60, EXCLK = 12MHz oscillator, SDRAM clock is 1/3 of CPU clock, run GCC or media program in Linux	240MHz	TBD	mA
	360MHz	TBD	mA

NOTE: CORE dynamic power is greatly depends on the software environment.

Table 3-19 CORE (VDD_{CORE}) Static Power Consumption

Conditions	Typical	Unit
VDDcore = 1.8V, Temperature = room, EXCLK oscillator stopped, all clocks exception RTCLK are stopped	TBD	uA

Table 3-20 CODEC (AVD_{CDC} + AVD_{HP}) Dynamic Power Consumption

Conditions		Typical	Unit
AVDCDC = AVDHP = 3.3V, Temperature = room, 220uF capacitors, 32Ωheadphone load, 48k sample rate, stereo	Replay all zero samples	TBD	mA
	Replay full scale 1k sine wave	TBD	mA
	Typical replay	TBD	mA
	Typical record	TBD	mA

Table 3-21 CODEC (AVD_{CDC} + AVD_{HP}) Static Power Consumption

Conditions	Typical	Unit
AVDCDC = AVDHP = 3.3V, Temperature = room, CODEC is in suspend mode	TBD	uA

Table 3-22 USB (AVD_{USB}) Dynamic Power Consumption

Conditions	Typical	Unit
TBD	TBD	mA

Table 3-23 USB (AVD_{USB}) Static Power Consumption

Conditions	Typical	Unit
AVDUSB = 3.3V, Temperature = room, USB 2.0 device is in suspend mode	TBD	uA

Table 3-24 ADC (AVD_{AD}) Dynamic Power Consumption

Conditions		Typical	Unit
AVDAD = 3.3V, Temperature = room, Resister between XP and XN, between YP and YN is 440Ω, pen touch in center of the touch screen, measure X, Y, Z values on every measurement	3 measure / 1ms	TBD	mA
	5 measure / 10ms	TBD	mA

Table 3-25 ADC (AVD_{AD}) Static Power Consumption

Conditions	Typical	Unit
AVDAD = 3.3V, Temperature = room, ADC is in suspend mode	TBD	uA

3.5 Oscillator Electrical Specifications

The processor contains two oscillators, each for a specific crystal: a 32.768KHz real time clock oscillator and a 12MHz EXCLK oscillator.

3.6 Power On, Reset and BOOT

3.6.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4725B processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and is detailed in Table 3-26.

On the processor, it is important that the power supplies be powered up in a certain order to avoid high current situations. The required order is:

1 VDDRTC

2 VDDA: AVDCDC, AVDHP

3 All other 3.3V VDDs (VDD33): VDDIO, AVDAD, AVDUSB

4 All 1.8V VDDs (VDD18): VDDCORE, VDDPLL

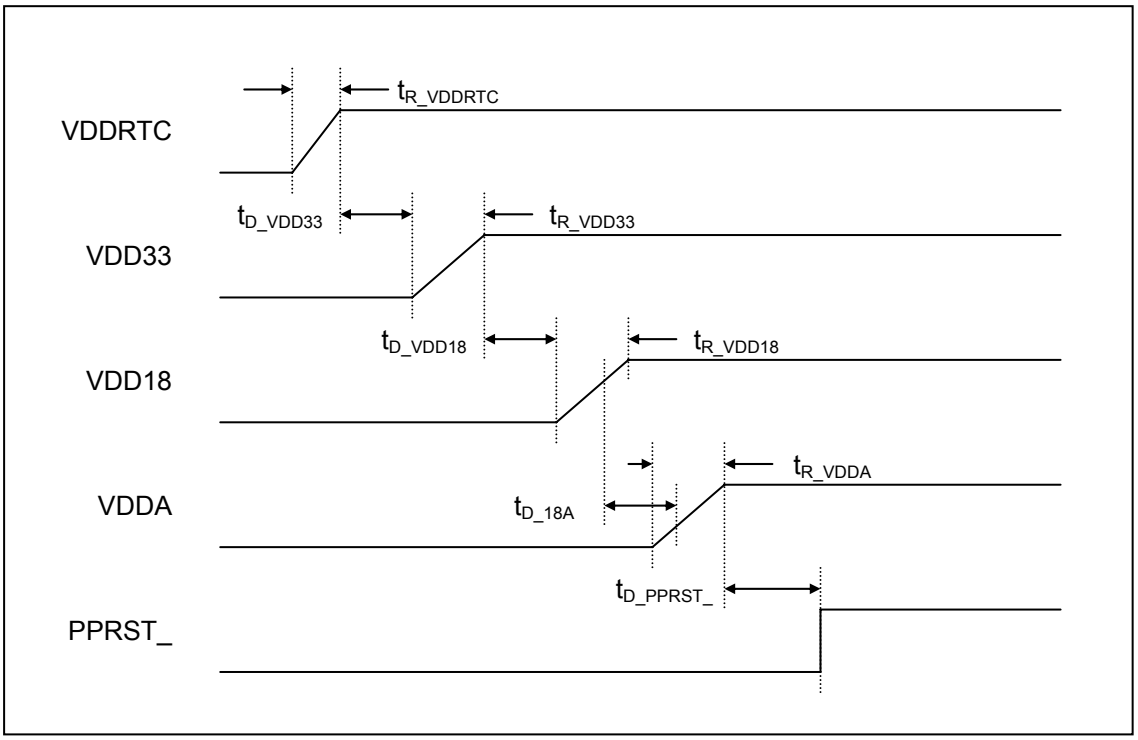


Figure 3-1 Power-On Timing Diagram

Table 3-26 Power-On Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
t_{R_VDDRTC}	VDDRTC rise/stabilization time	0	–	100	ms
t_{D_VDD33}	Delay between VDDRTC stable and VDD33 applies	$-t_{R\_VDDRTC}$	–	10	ms[1]

t_{R_VDD33}	VDD33 rise/stabilization time	0	–	100	ms
t_{D_VDD18}	Delay between VDD33 stable and VDD18 applies	$-t_{R\_VDD33}/2$	–	10	ms[2]
t_{R_VDD18}	VDD18 rise/stabilization time	0	–	100	ms
t_{D_18A}	Delay between VDD18 (actually VDDcore) arriving 1.5V and VDDA arriving 1V	0.01	–	10	ms
t_{R_VDDA}	VDDA rise/stabilization time	0	–	100	ms
$t_{D\_PPRST\_}$	Delay between VDDA stable and PPRST_ deasserted	20	–	–	ms

NOTES:

1 VDD33 can be applied before VDDRTC stable. But the time of VDD33 arriving 50%, 90% voltage level should later than that of VDDRTC arriving the same level.

2 VDD18 can be applied before VDD33 stable. But the time of VDD18 arriving 50%, 90% voltage level should later than that of VDD33 arriving the same level.

3.6.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is a few RTCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 0ms ~ 125ms programable, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins, except WAIT_ pin, are put to GPIO input function with the internal pull-up set to on. The WAIT_ pin is set to wait function with the internal pull-up set to on. The PWRON_ is output 0. The 32768Hz/12MHz oscillators are on. The analog devices, the USB 2.0 PHY, the CODEC DAC/ADC and the SAR-ADCs are put in suspend mode.

3.6.3 BOOT

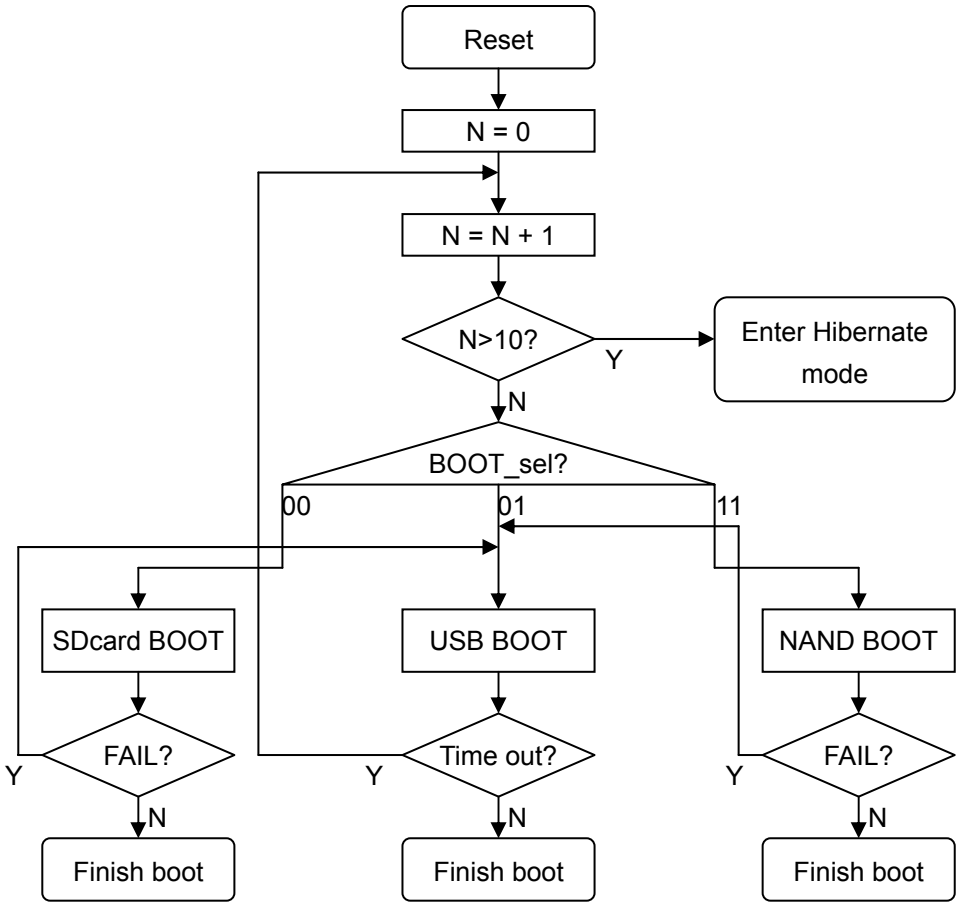
JZ4725B support 3 different boot sources depending on BOOT_SEL0 and BOOT_SEL1 pin values. Table 3-27 lists them.

Table 3-27 Boot from 3 boot sources

BOOT_SEL1	BOOT_SEL0	Boot From
1	1	NAND flash, CS1
0	1	USB2.0 device @EXCLK=12MHz
0	0	SD card: MSC0
1	0	Reserved

The boot procedure is showed in the following flow chart:

- In case of NAND/SDcard boot, if it fails, enter USB boot.
- In case of USB boot, if it cannot connect to USB host within 10 seconds, restart the boot procedure.
- If the procedure has been repeated more than 10 times, enter hibernating mode.



When JZ4725B BOOT from NAND at CS1_ or MSC0, some of the memory interface pins are set to

function pin from the default GPIO pin and are used in executing BOOT ROM instructions. When BOOT from USB, none of any pins are used. Table 3-28 lists the cases.

Table 3-28 Pins are used and are set to function pins during BOOT

Boot Source Condition	GPIO pin state changed from RESET
USB	None
8-bits NAND flash at CS1_	TBD
16-bits NAND flash at CS1_	TBD
MSC0	TBD